

21-26.5GHz Integrated Down converter

GaAs Monolithic Microwave IC in SMD package

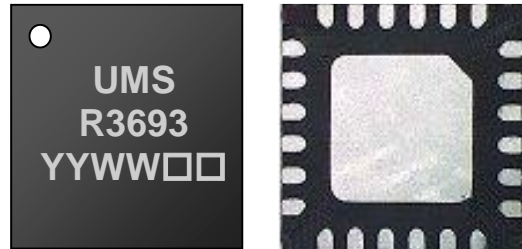
Description

The CHR3693-QDG is a multifunction chip, which integrates a balanced cold FET mixer, a time two multiplier, and a RF self biased LNA.

It is designed for a wide range of applications, typically commercial communication systems.

The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate and air bridges.

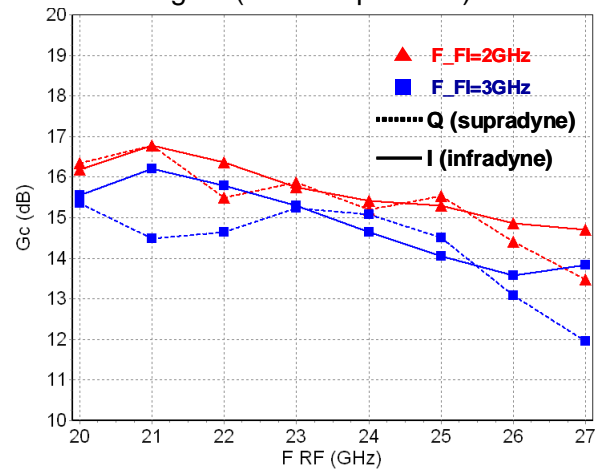
It is supplied in lead-free SMD package.



Main Features

- Broadband performance 21-26.5GHz
- 14dB gain
- -5dBm input IP3
- 18dBc image rejection
- DC bias: $V_d=4.0\text{Volt}$ @ $I_d=160\text{mA}$
- 24LQFN4x4
- MSL Level: 1

Conversion gain (Inf. & Sup. Mode)



Main Electrical Characteristics

$T_{amb.} = +25^{\circ}\text{C}$, $V_{dx}=V_{dl}=4.0\text{V}$, $V_{gx}=-0.9\text{V}$, $V_{gm}=-0.7\text{V}$

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------|--------------------|-----|-----|------|------|
| F_RF | RF frequency range | 21 | | 26.5 | GHz |
| F_LO | LO frequency range | 9 | | 14 | GHz |
| F_IF | IF frequency range | DC | | 3.5 | GHz |
| Gc | Conversion gain | 12 | 14 | | dB |

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

Electrical Characteristics

Tamb.= +25°C, Vdx=Vdl = +4.0V, Vgx=-0.9V, Vgm=-0.7V

| Symbol | Parameter | Min | Typ | Max | Unit |
|---------|---|-----|-----|------|------|
| F_RF | RF frequency range | 21 | | 26.5 | GHz |
| F_LO | LO frequency range | 9 | | 14 | GHz |
| F_IF | IF frequency range | DC | | 3.5 | GHz |
| Gc | Conversion gain | 12 | 14 | | dB |
| NF | Noise Figure for IF>0.1GHz | | 2 | 2.5 | dB |
| P_LO | LO Input power | | 2 | 5 | dBm |
| Img Sup | Image Suppression ⁽¹⁾ | 15 | 18 | | dBc |
| IIP3 | Input IP3 | | -2 | | dBm |
| LO_RL | LO return loss | | -9 | -7 | dB |
| RF_RL | RF return loss (21 to 24GHz) | | -12 | -7 | dB |
| | RF return loss (24 to 26.5GHz) | | -8 | -6 | dB |
| LO/RF | Isolation LO → RF | | 45 | | dBc |
| 2LO/RF | Isolation 2LO → RF | | 35 | | dBc |
| Id | Bias current ⁽²⁾ (Idl + Idx) | 120 | 160 | 200 | mA |

⁽¹⁾ With external I/Q 90° hybrid coupler

⁽²⁾ Typically, Idl= 90mA, Idx=70mA

These values are representative of onboard measurements as defined on the drawing at paragraph "Evaluation mother board".

Absolute Maximum Ratings ⁽¹⁾

Tamb.= +25°C

| Symbol | Parameter | Values | Unit |
|--------|---------------------------------------|--------------|------|
| Vd | Maximum drain bias voltage | 4.5 | V |
| Id | Maximum drain bias current | 230 | mA |
| Vg | Gate bias voltage | -2.0 to +0.4 | V |
| P_RF | Maximum RF input power ⁽²⁾ | 10 | dBm |
| P_LO | Maximum LO input power ⁽²⁾ | 10 | dBm |
| Tch | Maximum channel temperature | 175 | °C |
| Ta | Operating temperature range | -40 to +85 | °C |
| Tstg | Storage temperature range | -55 to +150 | °C |

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage.

⁽²⁾ Duration < 1s.

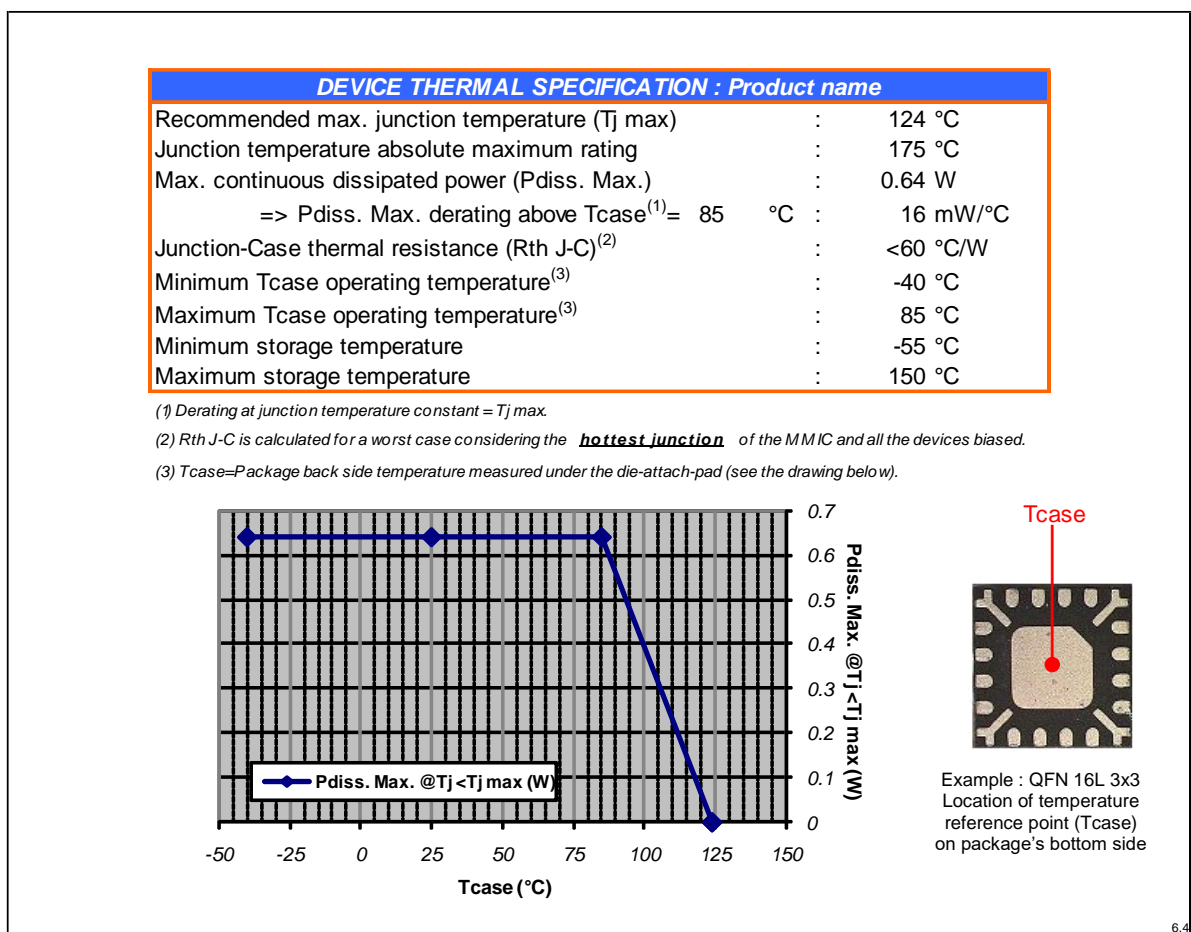
Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).

The temperature is monitored at the package back-side interface (T_{case}) as shown below.

The system maximum temperature must be adjusted in order to guarantee that T_{case} remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

A derating must be applied on the dissipated power if the T_{case} temperature can not be maintained below than the maximum temperature specified (see the curve $P_{diss. Max}$) in order to guarantee the nominal device life time (MTTF).



Typical Board Measurements

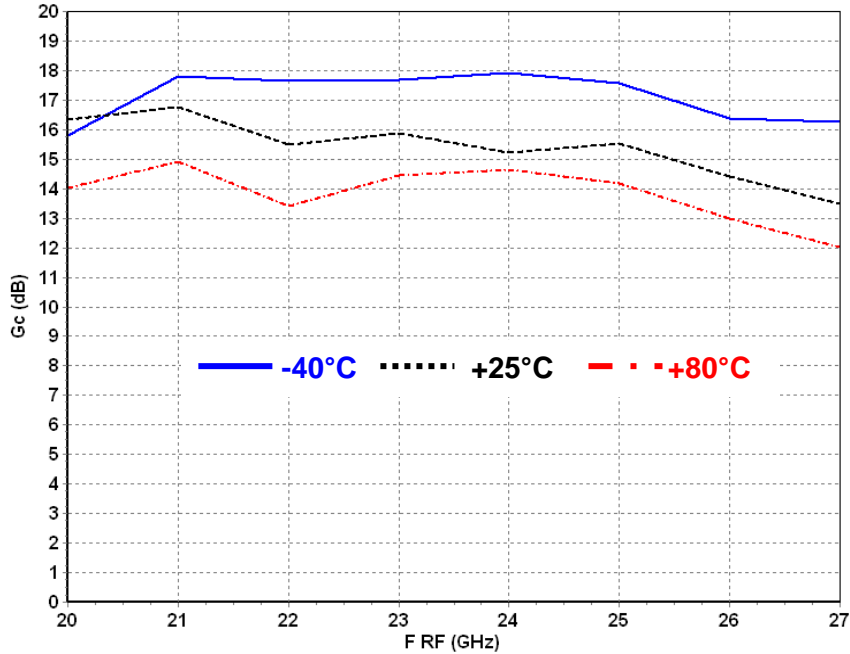
Tamb=25°C, Vdx=Vdl=4V, Typical Vgx=-0.9V & Vgm=-0.7V

P_LO=2dBm, F_IF=2GHz

These values are representative of onboard measurements as defined on the drawing at page 12 (paragraph "Evaluation mother board") (in connector access planes).

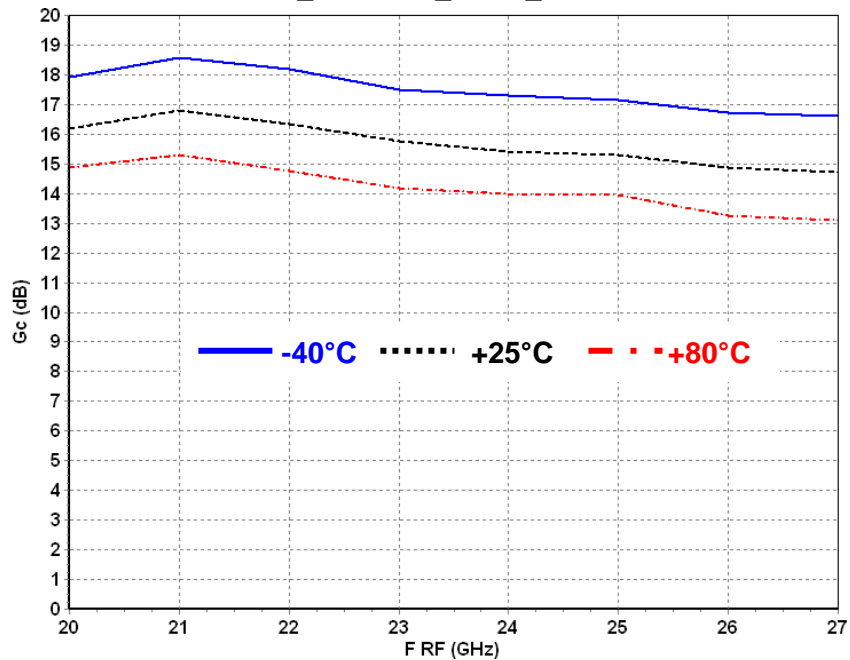
Conversion Gain in infradyne mode versus frequency

$$F_{RF} = 2 \times F_{LO} - F_{IF}$$



Conversion Gain in supradyne mode versus frequency

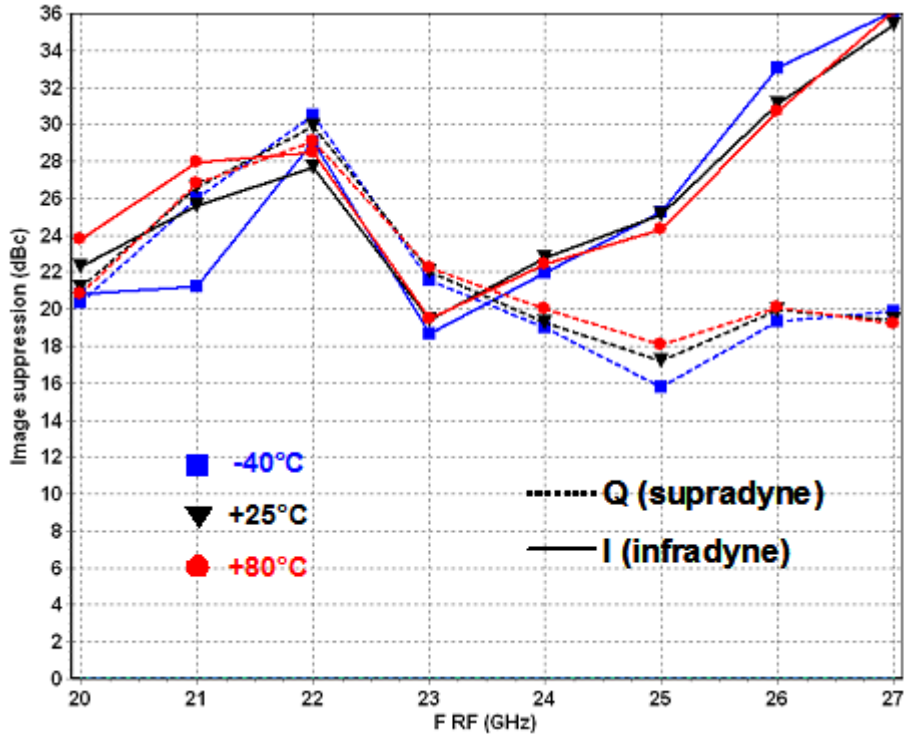
$$F_{RF} = 2 \times F_{LO} + F_{IF}$$



Typical Board Measurements

Tamb=25°C, Vdx=Vdl=4V, Typical Vgx=-0.9V & Vgm=-0.7V
 P_LO=2dBm, F_IF=2GHz

Image Frequency rejection (inf. & sup. Mode) @ -40, +25, +80°C



Typical Board Measurements

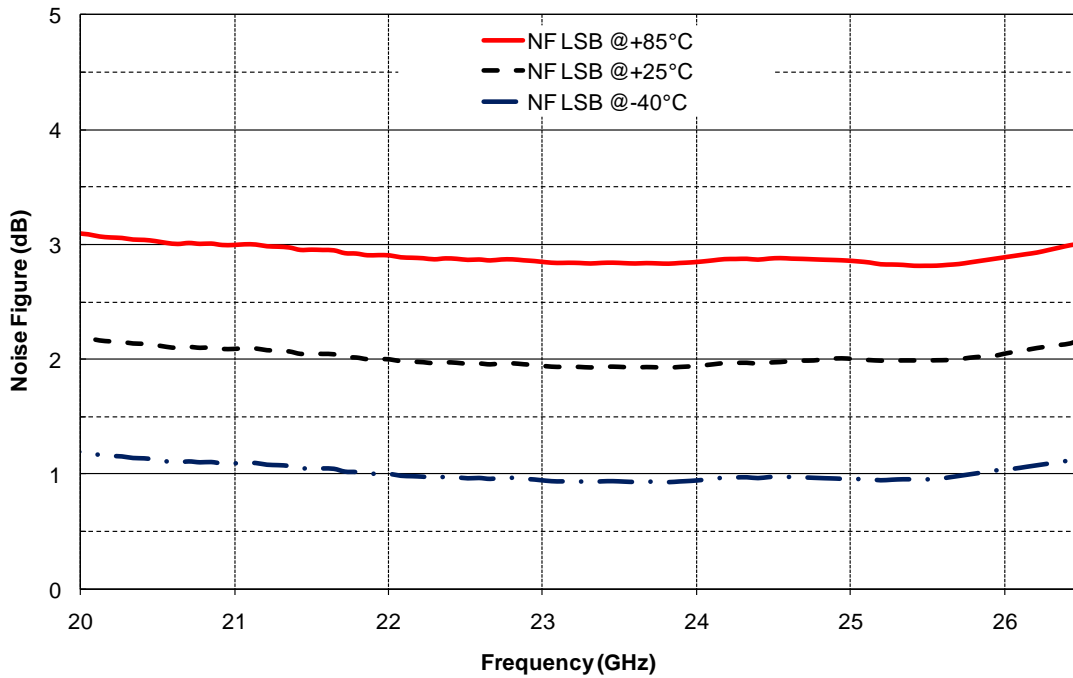
Tamb=25°C, Vdx=Vdl=4V, Typical Vgx=-0.9V & Vgm=-0.7V

P_LO=2dBm, F_IF=2GHz

Board losses have been de-embedded (results in package access planes)

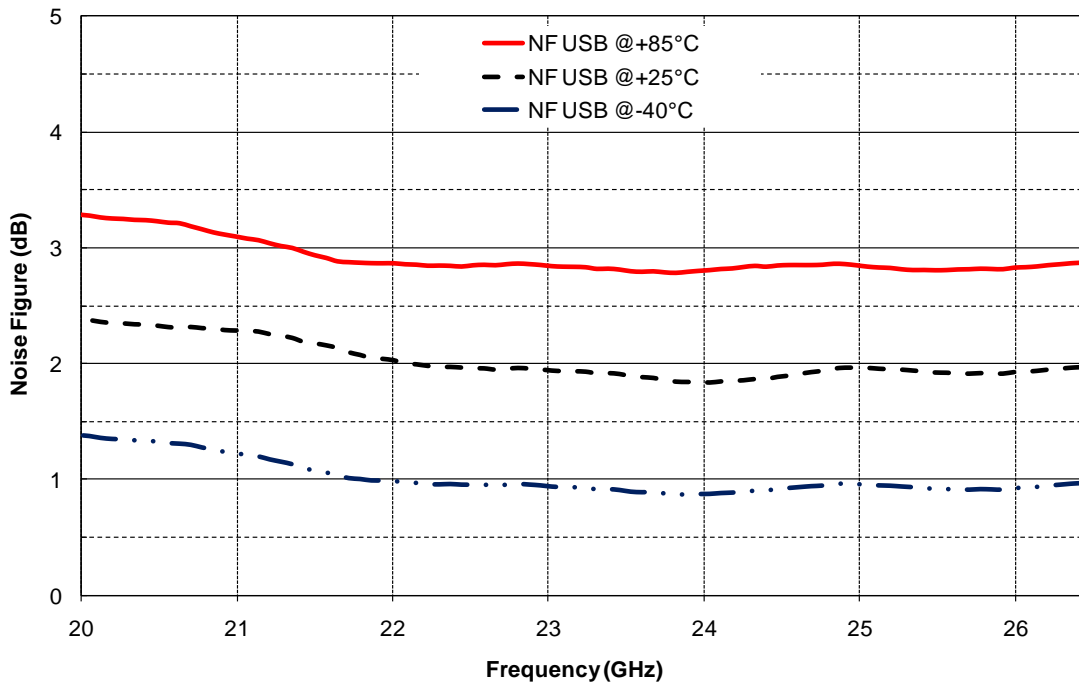
Noise Figure in infradyne mode versus frequency

$$F_{RF} = 2x F_{LO} - F_{IF}$$



Noise Figure in supradyne mode versus frequency

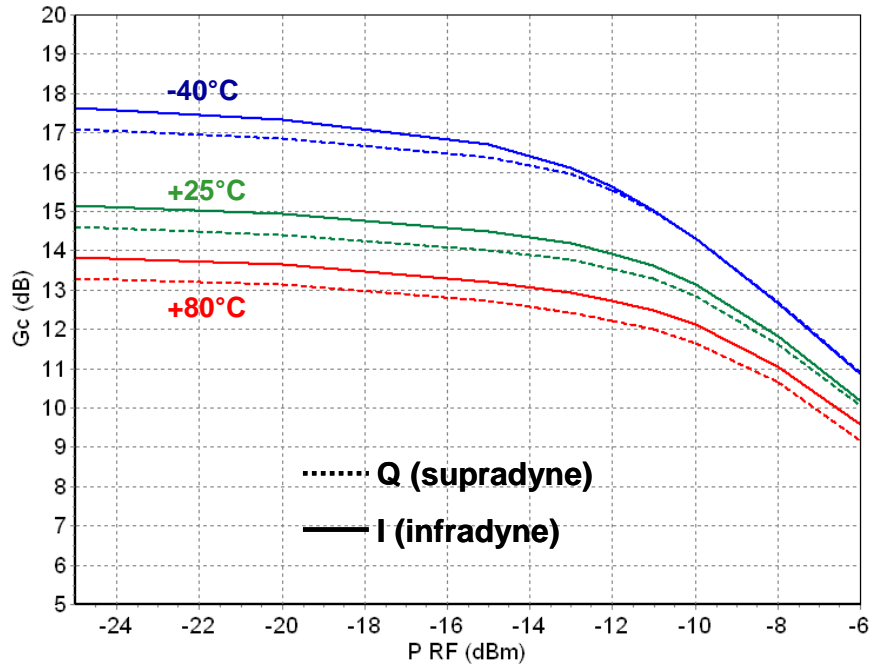
$$F_{RF} = 2x F_{LO} + F_{IF}$$



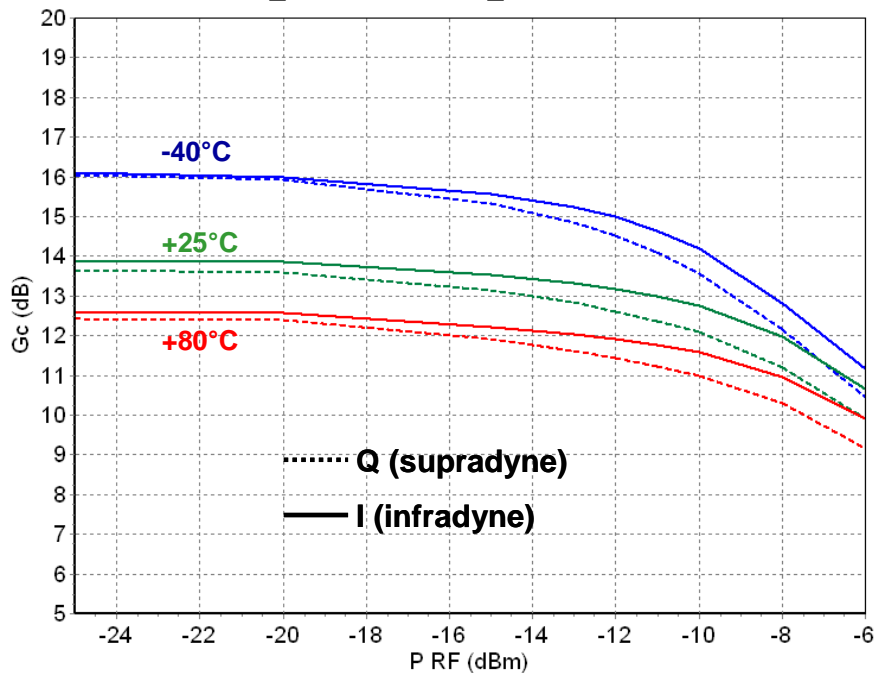
Typical Board Measurements

T_{amb}=25°C, V_{dx}=V_{dI}=4V, Typical V_{gx}=-0.9V & V_{gm}=-0.7V
 P_{LO}=2dBm

Compression versus PRF (infradyne and supradyne modes)
 F_{RF}=21GHz & F_{IF}=3GHz

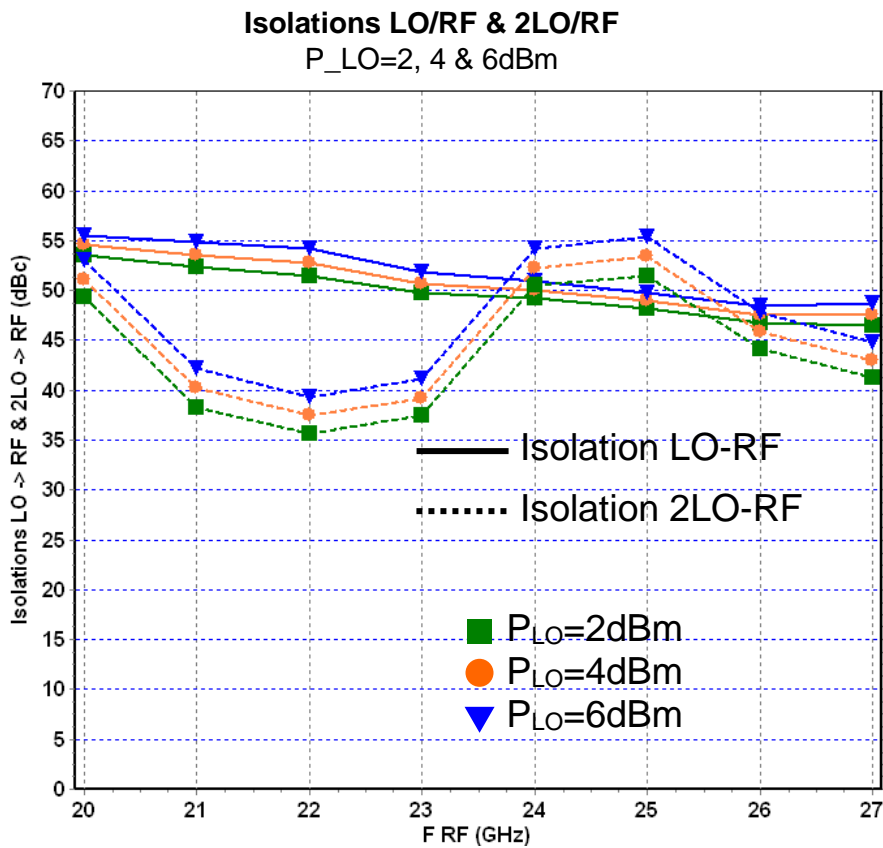
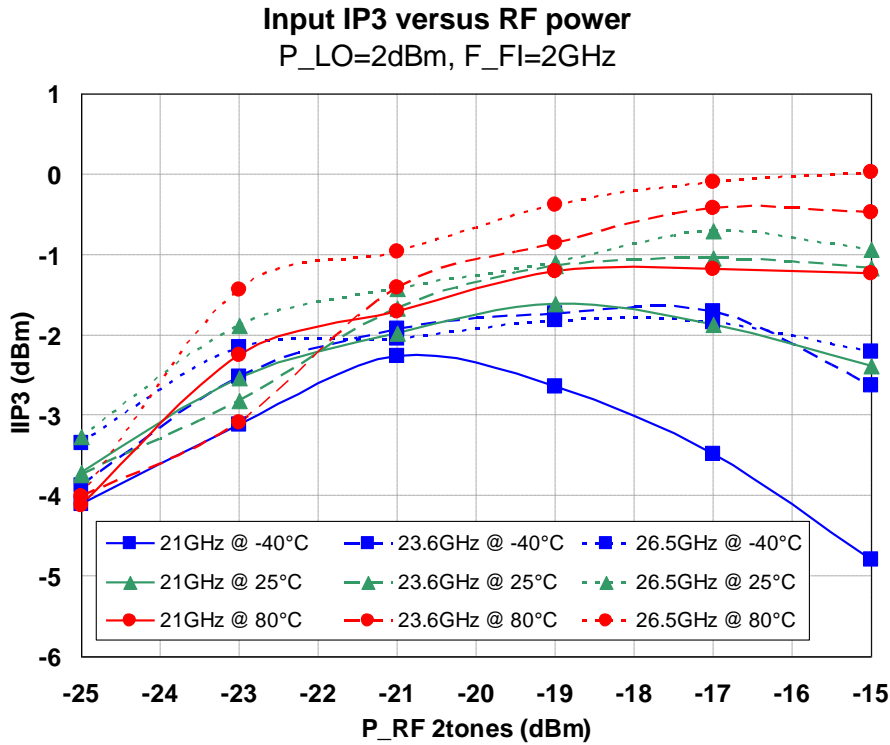


Compression versus PRF (infradyne and supradyne modes)
 F_{RF}=26GHz & F_{IF}=2GHz



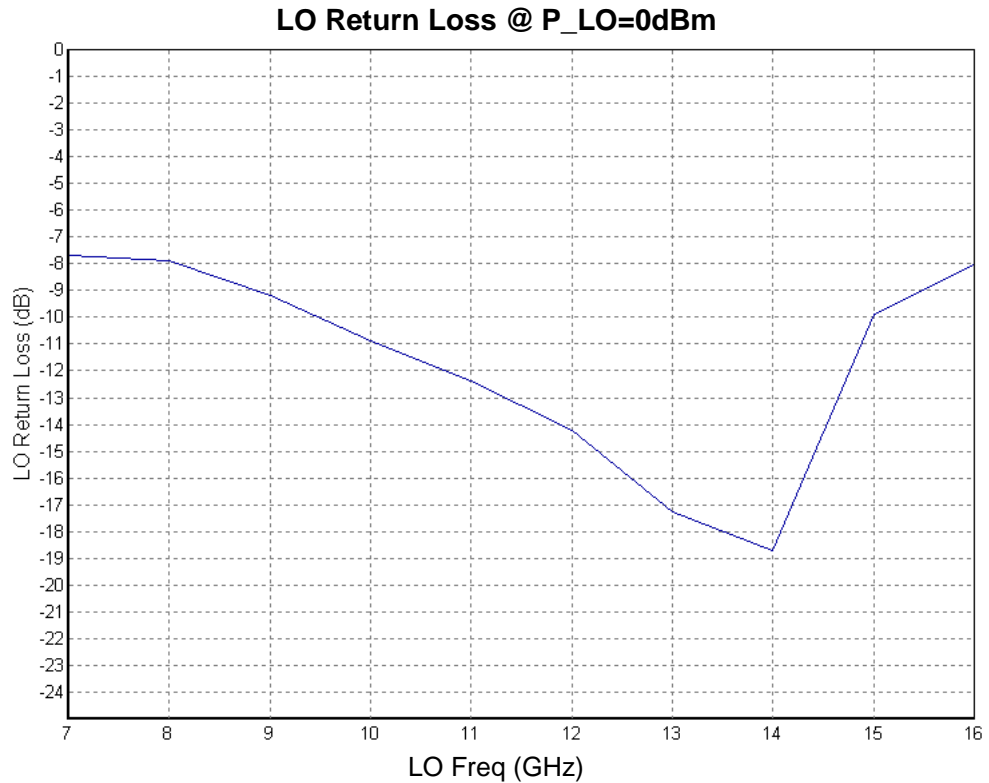
Typical Board Measurements

Tamb=25°C, Vdx=Vdl=4V, Typical Vgx=-0.9V & Vgm=-0.7V

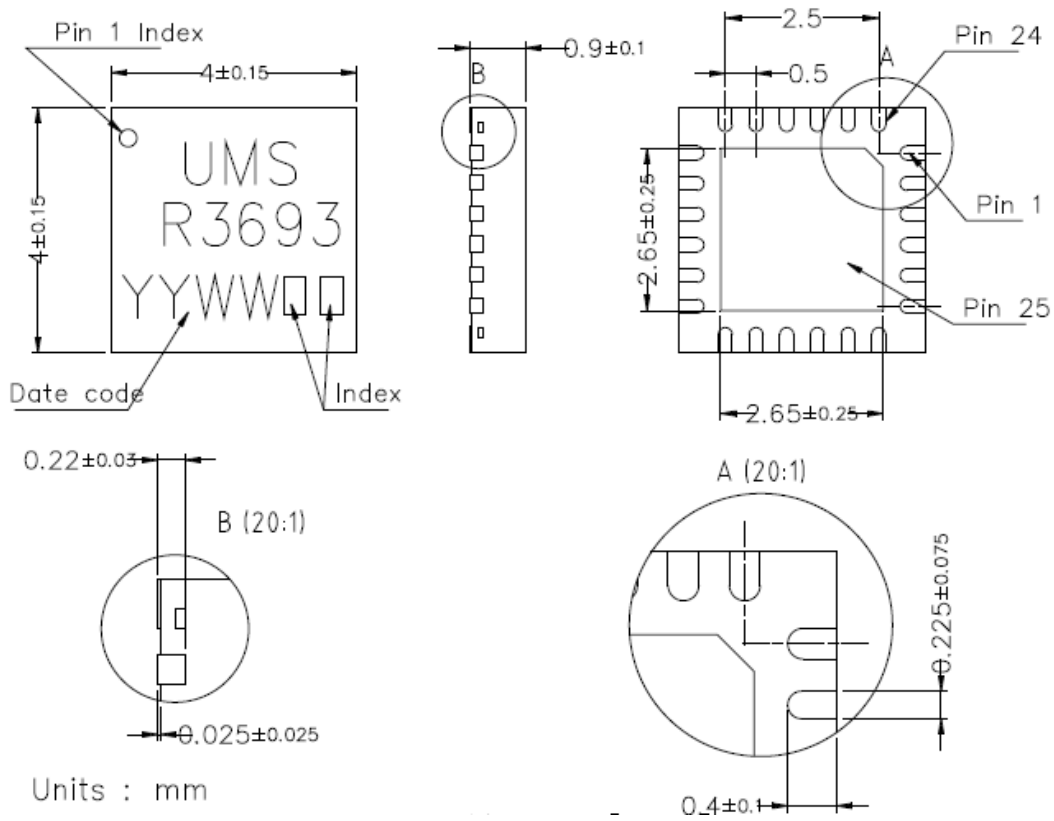


Typical Board Measurements

Tamb=25°C, Vdx=Vdl=4V, Typical Vgx=-0.9V & Vgm=-0.7V



Package outline ⁽¹⁾



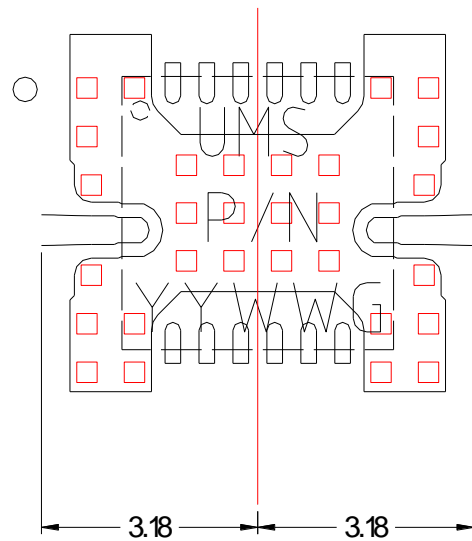
| | | | | |
|---------------------|--------------|-----------------------|------------------------|------------------------|
| Matt tin, Lead Free | (Green) | 1- NC | 9- Vdx | 17- Gnd ⁽²⁾ |
| Units : | mm | 2- Gnd ⁽²⁾ | 10- NC | 18- NC |
| From the standard : | JEDEC MO-220 | 3- Gnd ⁽²⁾ | 11- NC | 19- I-IF out |
| | (VGGD) | 4- RF in | 12- Vgx | 20- Gnd ⁽²⁾ |
| | 25- GND | 5- Gnd ⁽²⁾ | 13- Gnd ⁽²⁾ | 21- Gnd ⁽²⁾ |
| | | 6- Gnd ⁽²⁾ | 14- Gnd ⁽²⁾ | 22- Q-IF out |
| | | 7- Vdl | 15- LO IN | 23- NC |
| | | 8- Vgm | 16- Gnd ⁽²⁾ | 24- NC |

⁽¹⁾ The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<https://www.ums-rf.com>) for exact package dimensions.

⁽²⁾ It is strongly recommended to ground all pins marked "Gnd" through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

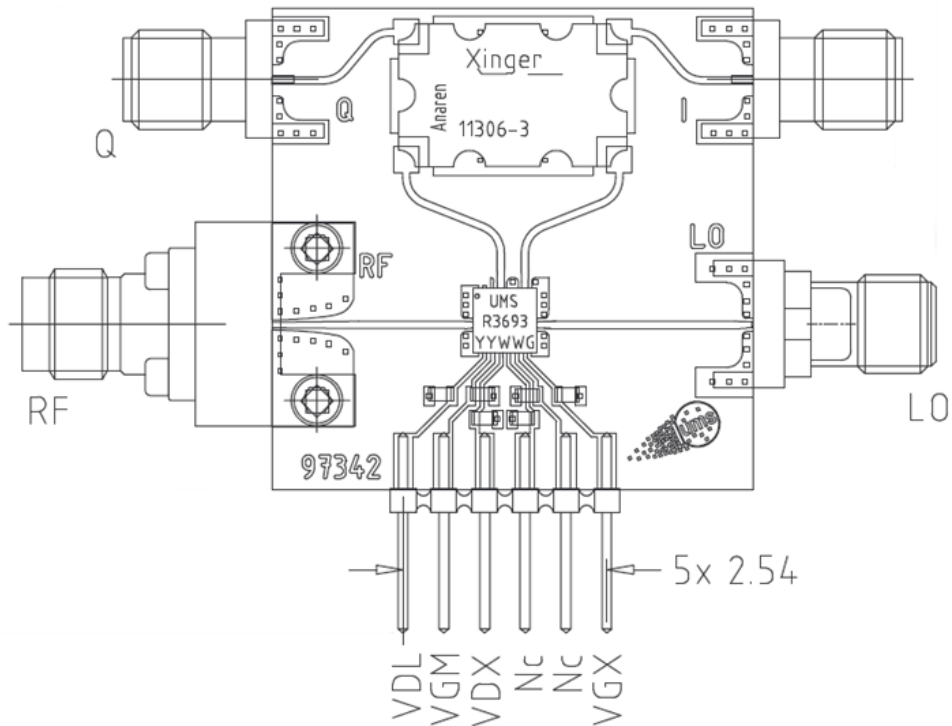
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF \pm 10% are recommended for all DC accesses.
- See application note AN0017 for details.



10nF capacitor 0603

Hybrid coupler 90° (ex. Anaren 11306-3)

Note



Recommended package footprint

Refer to the application note AN0017 available at <https://www.ums-rf.com> for package footprint recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 RoHS compliant package: CHR3693-QDG/XY
Stick: XY = 20 Tape & reel: XY = 21

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Description