

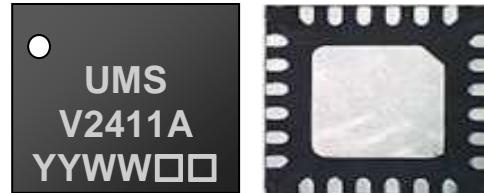
## Fully Integrated HBT K-band VCO GaAs Monolithic Microwave IC in QFN package

### Description

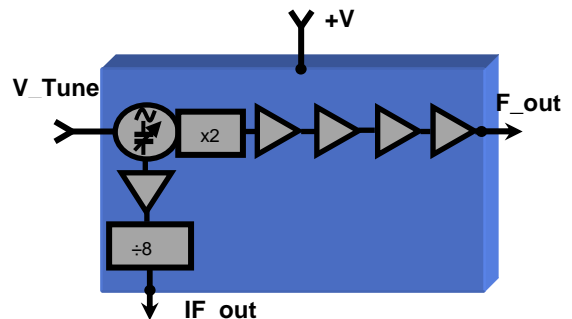
The CHV2411aQDG is a monolithic multifunction for frequency generation. It integrates an X-band “push-push” oscillator with frequency control (VCO) thanks to base-collector diodes, used as varactors, a K-band buffer amplifiers and a divider by 8. The VCO is fully integrated on HBT process. All the active devices are internally self-biased.

The circuit is fully integrated on InGaP HBT process: 2µm emitter length, via holes through the substrate and high Q passive elements.

The chip is delivered in a 24 Leads RoHS compliant QFN4x4 package.

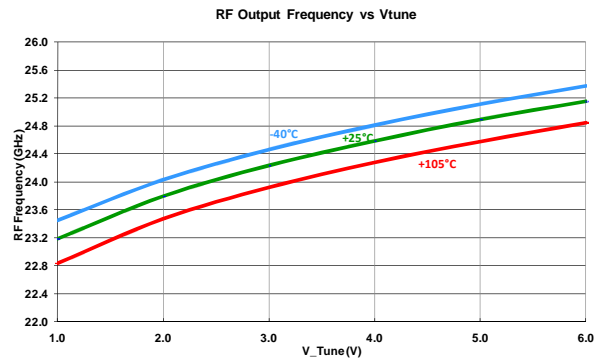


Plastic package



### Main Features

- K-band VCO+K buffers+Prescaler/8
- Fully integrated VCO (no need for external Resonator)
- Low phase noise
- High temperature range
- High frequency stability
- On chip self-biased devices
- Standard SMD package: 24L-QFN4x4



### Main Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
F_out	Specified output frequency range	24.0	24.125	24.25	GHz
Gain	Oscillator frequency		F_out/2		GHz
NF	Output Intermediate frequency		F_out/16		dB
Pout	Output power at F_out	13	16		dBm
PFI	Output power at Intermediate freq. (IF)	-3	0		dBm
PN	SSB Phase Noise @F_out@100KHz		-90	-80	dBc/Hz

ESD Protections: Electrostatic discharge sensitive device observe handling precautions!

## Electrical Characteristics

### VCO & buffer Part

Symbol	Parameters	Min	Typ	Max	Unit
F_out	Output Frequency range (Operating band)	24		24.25	GHz
F_vco	VCO frequency	F_out/2			
V_Tune	Voltage Tuning range	1		6	V
	Tuning sensitivity	250	400	725	MHz/V
	Frequency drift rate		5		MHz/°C
H1	Harmonics 1/2F_out			-20	dBc
H3	Harmonics 3/2 F_out			-40	dBc
H4	Harmonics 2 F_out			-20	dBc
PN	SSB Phase Noise given @ F_out @ 100 KHz		-90	-80	dBc/Hz
	Main Output (RF_Out) VSWR		2:1		
	Pulling into 2:1 VSWR for all phases			8	MHz
	Pushing @ within the V_tune range			250	MHz/V
P_out	Output Power on RF_out port	13	16	19	dBm
	Positive supply current		140	170	mA

### Prescaler Part

Symbol	Parameters	Min	Typ	Max	Unit
IF_out	IF Output Frequency	F_out/16			GHz
	Output Power	-3	0		dBm
	Positive supply current		80	110	mA
	Prescaler Output (IF) VSWR		2:1		

### General

Symbol	Parameters	Min	Typ	Max	Unit
VB,V1,VB1,V2,VB2,VD	Positive supply voltage		5		V
+I (IB1+IB2+I1+I2)	Total Positive supply current		220	280	mA
Top	Operating temperature range	-40		+105	°C

All the parameters are specified between 1V and 6V of Tuning Voltage

### Absolute Maximum Ratings <sup>(1)</sup>

Symbol	Parameters	Values	Unit
V_tune	Positive Tuning voltage	10	V
+V	Positive supply voltage	6	V
+ID	Positive supply current (Prescaler)	120	mA
+IB1 / +IB2	Positive supply current (buffers 2 & 3)	50 / 55	mA
+I1 / +I2	Positive supply current (VCO+ buffer 1)	35 / 50	mA
+IB	Positive supply current (prescaler's buffer)	15	mA
Top	Operating temperature range (2)	-40 to +105	°C
TcaseMax	Absolute maximum rating Tcase temperature (2)	115	°C
Tstg	Storage temperature range	-55 to +125	°C

<sup>(1)</sup> Operation of this device above anyone of these parameters may cause permanent damage.  
Duration < 1s

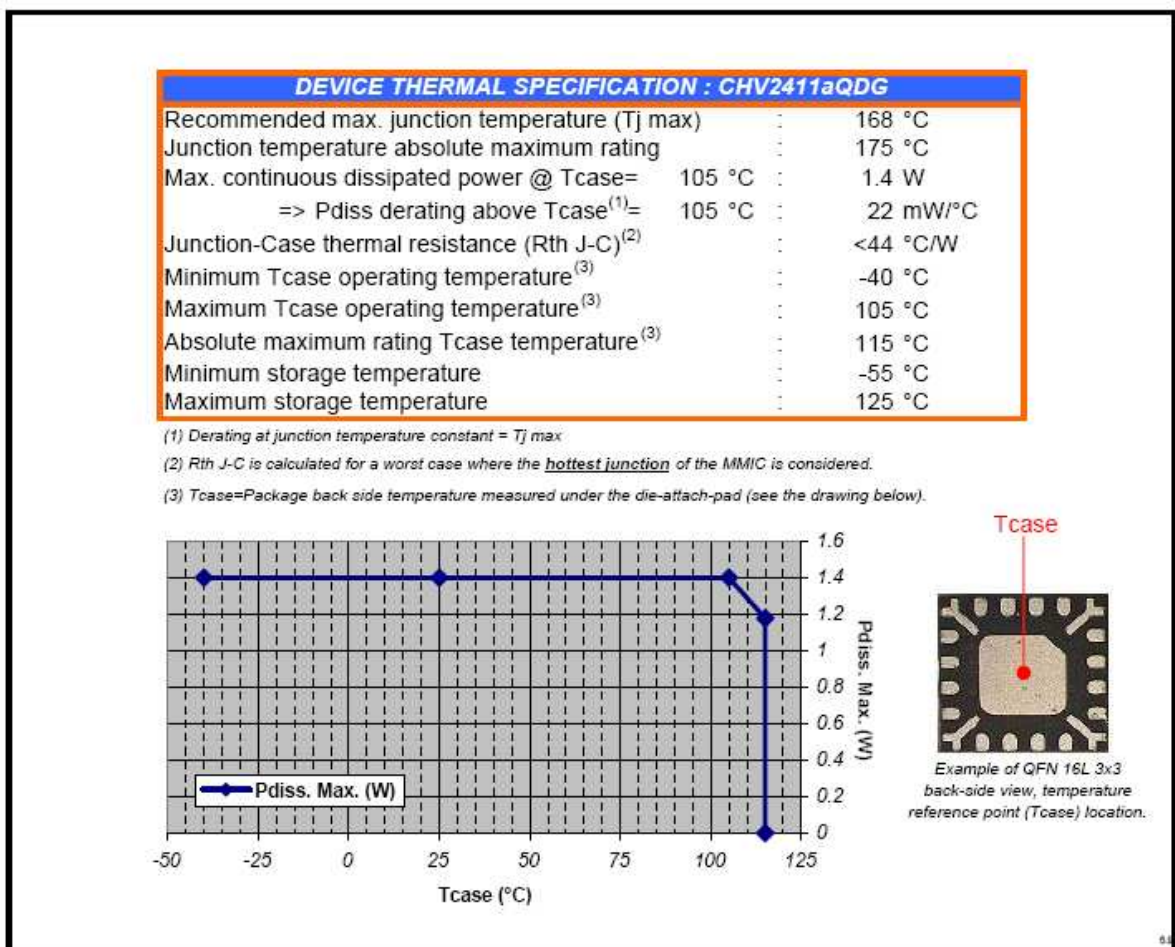
<sup>(2)</sup> Temperature of the back side of the QFN package

## Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).

The temperature is monitored at the package back-side interface ( $T_{case}$ ) as shown below. The system maximum temperature must be adjusted in order to guarantee that  $T_{case}$  remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

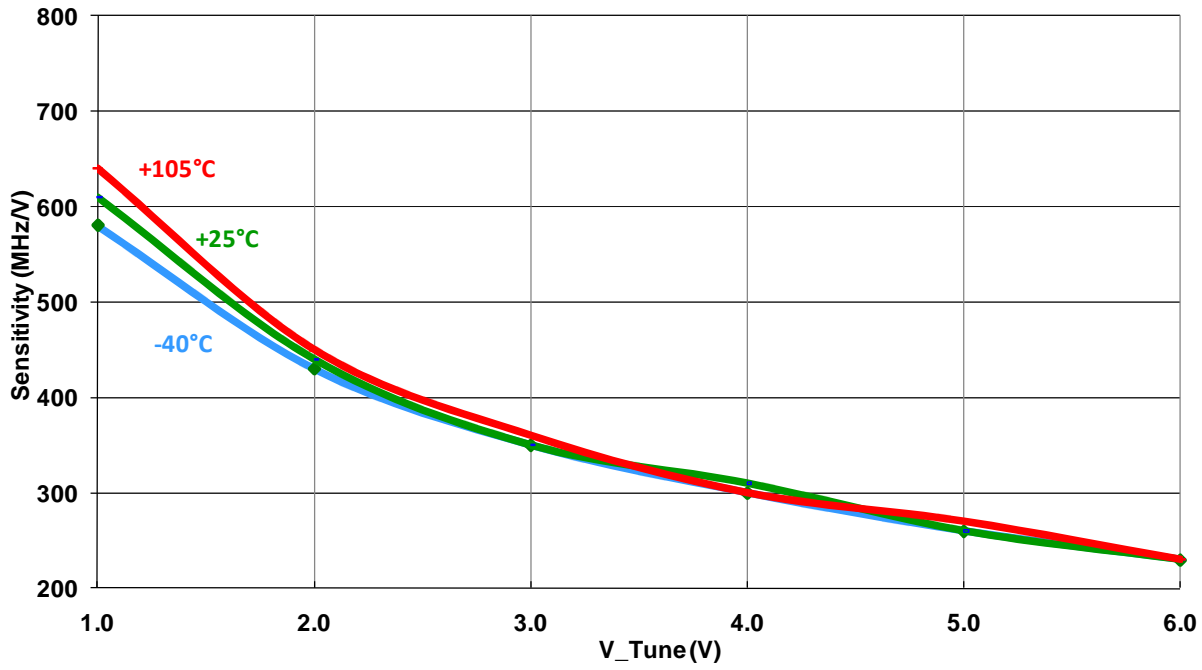
A derating must be applied on the dissipated power if the  $T_{case}$  temperature can not be maintained below than the maximum temperature specified (see the curve  $P_{diss. Max}$ ) in order to guarantee the nominal device life time (MTTF).



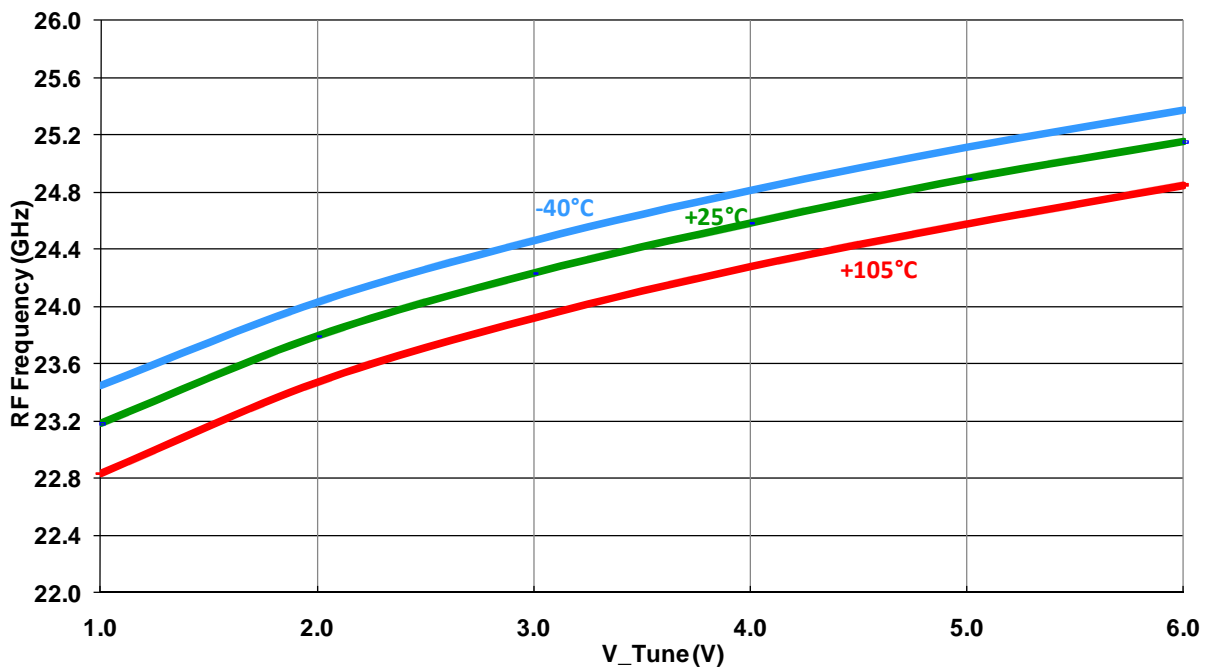
## Typical QFN Measurements on board 95791 (at QFN accesses)

Note: The temperature mentioned below is taken at the back side of the QFN package

### Sensitivity versus Vtune

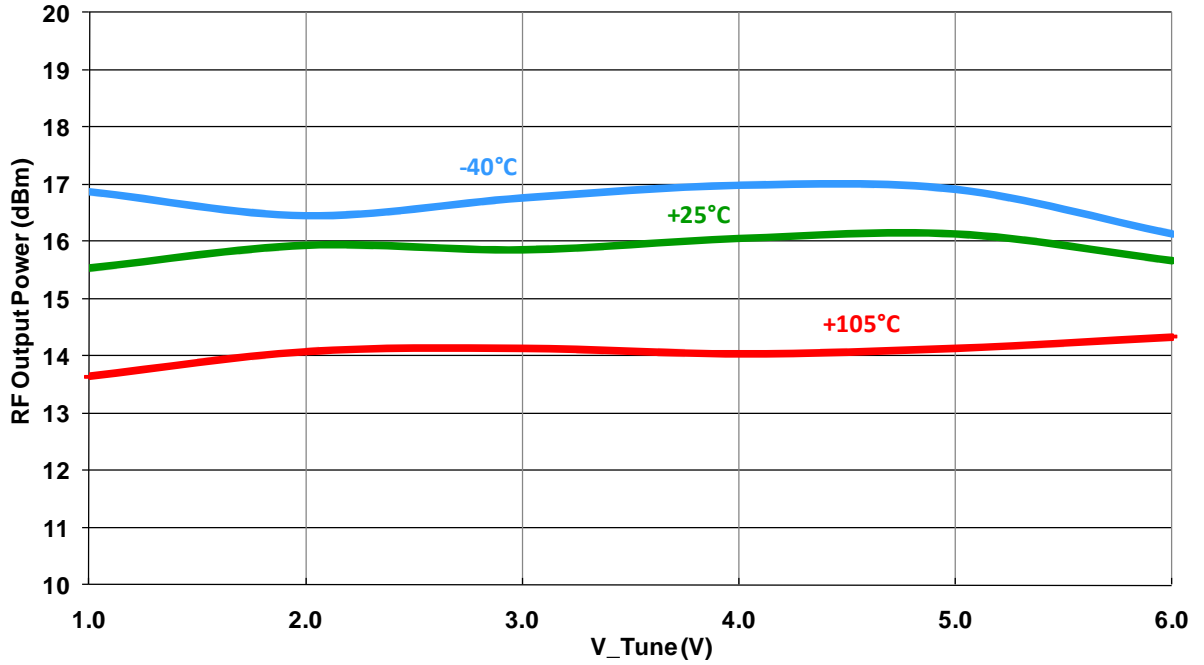


### RF Output Frequency versus Vtune

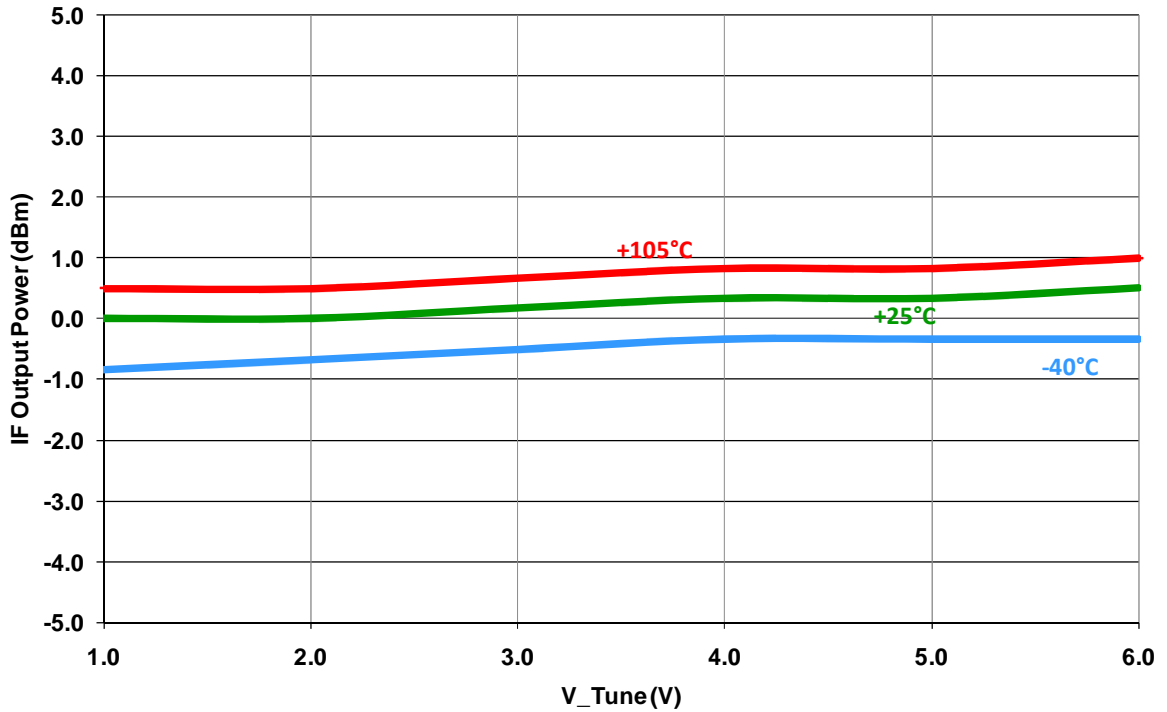


Typical Measured Performances

RF Output Power versus Vtune

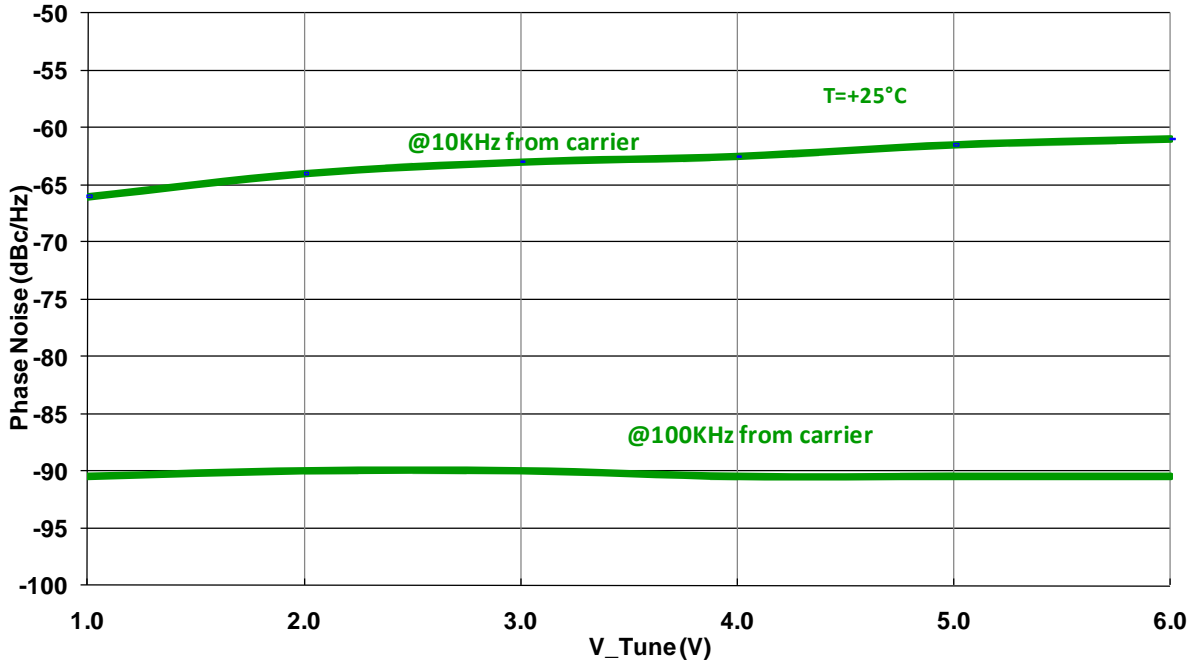


IF Output Power versus Vtune

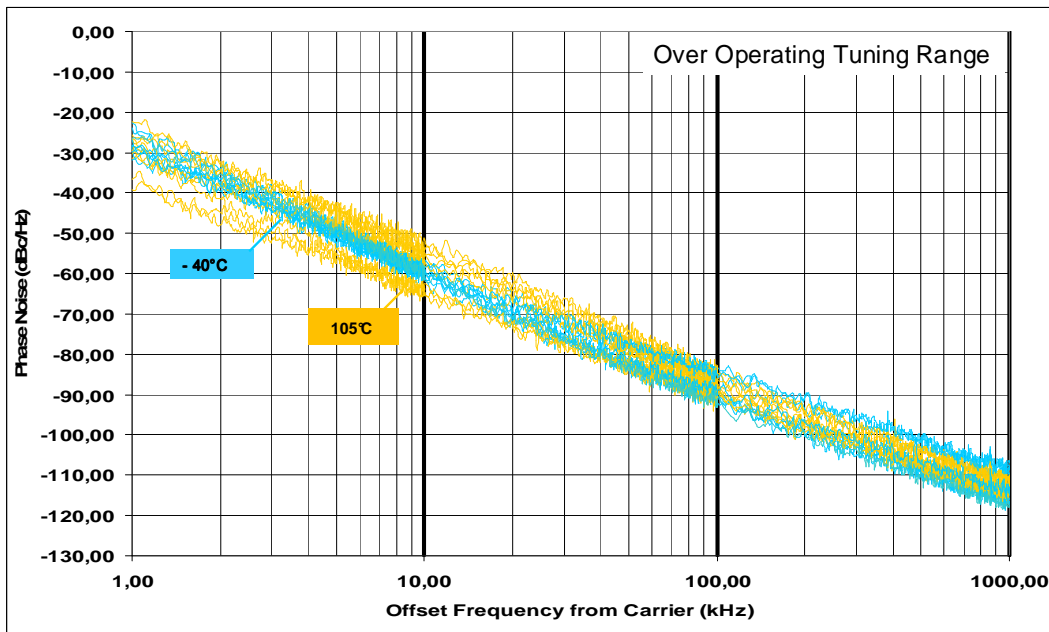


## Typical Measured Performances 25°C

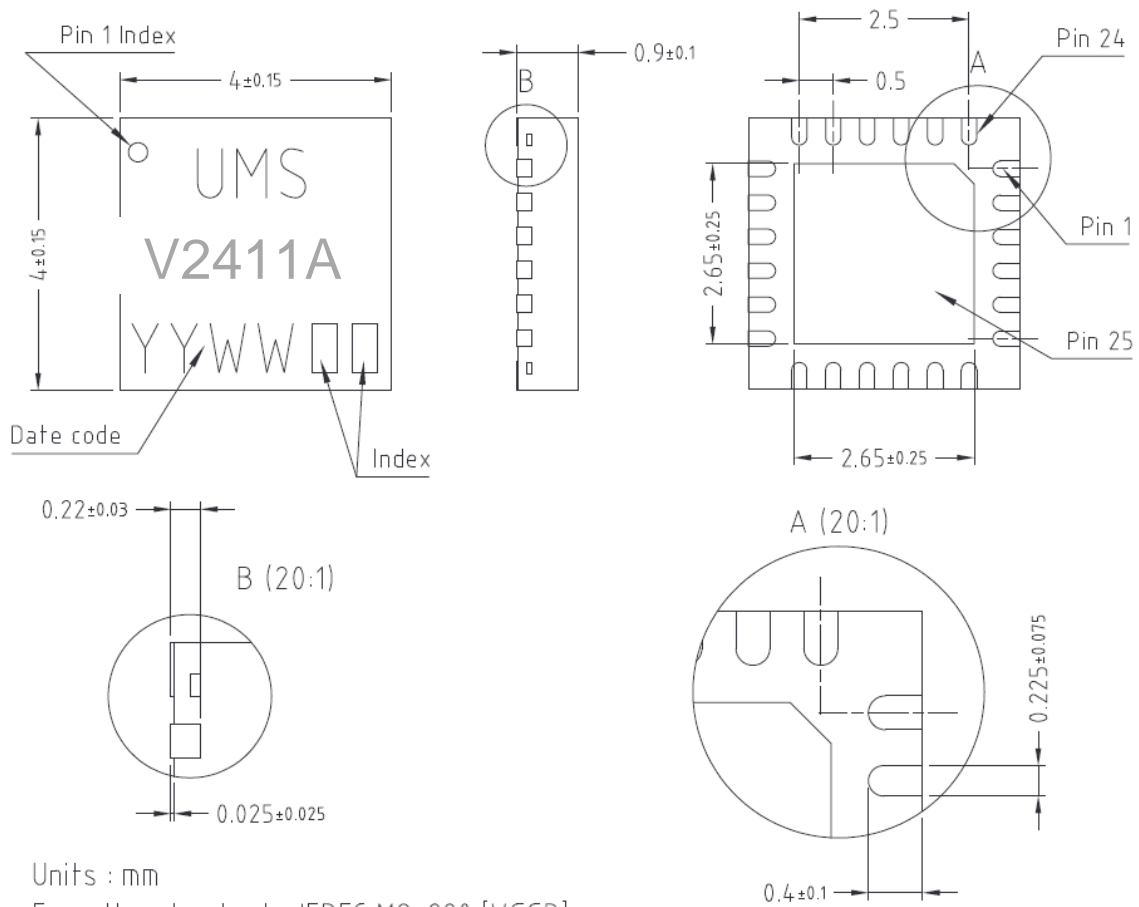
### Phase Noise versus Vtune



### Phase Noise versus Offset frequency Phase Noise vs Offset frequency from carrier



**Package outline <sup>(1)</sup>**



Units : mm

From the standard : JEDEC MO-220 [VGGD]

Matt tin, Lead free (Green)

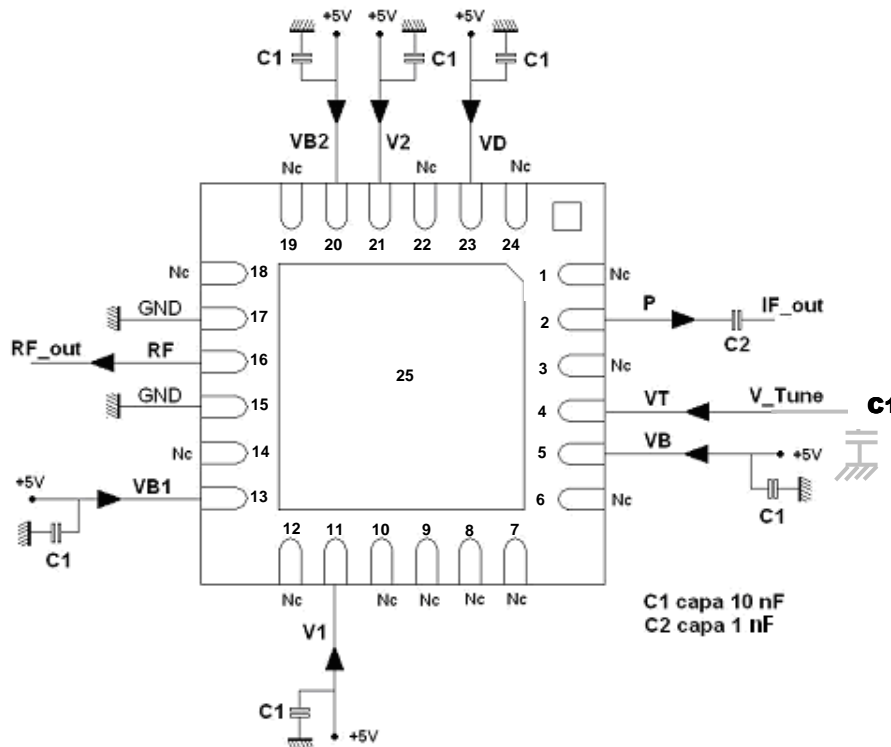
Matt tin, Lead Free (Green)	1- Nc	13- VB1
Units mm	2- P	14- Nc
From the standard JEDEC MO-220 (VGGD)	3- Nc	15- Gnd
	4- VT	16- RF
25- GND	5- VB	17- Gnd
	6- Nc	18- Nc
	7- Nc	19- Nc
	8- Nc	20- VB2
	9- Nc	21- V2
	10- Nc	22- Nc
	11- V1	23- VD
	12- Nc	24- Nc

<sup>(1)</sup>The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 available at <http://www.ums-gaas.com> for exact package dimensions.

## QFN Pin-out description

Pin number	Pin name	Symbol Name	Description
15,17	GND		Ground
2	P	IF_out	IF output at 1.5 GHz
4	VT	V_Tune	Frequency Tuning Port
5,11,13,20,21,23	VB, V1, VB1, VB2, V2, VD	+V	Positive supply voltage
5	VB		Positive supply voltage of 12 GHz prescalar's buffer
11,21	V1,V2		Positive supply voltage of the VCO core+1 <sup>st</sup> stage of the 24GHZ buffers
13	VB1		Positive supply voltage of the 2 <sup>nd</sup> & 3 <sup>rd</sup> stages of the 24GHZ buffers
20	VB2		Positive supply voltage of the 4 <sup>th</sup> stages of the 24GHZ buffers
16	RF	RF_out	RF output at 24 GHz
2	P	F_out/16	Prescalar output at 1.5 GHz
1,3,6,7,8,9,10,12,14, 18, 19,22,24	Nc		Not connected

### External Components and bias configuration (recommended)

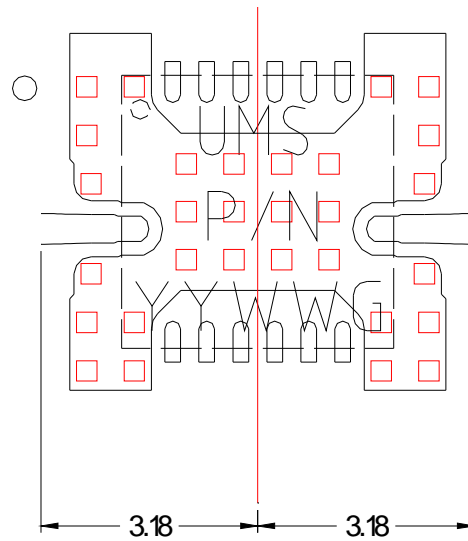


**Important:** Need for a capacitor on the prescalar output port as a DC block (C2).



## Definition of the Sij reference planes

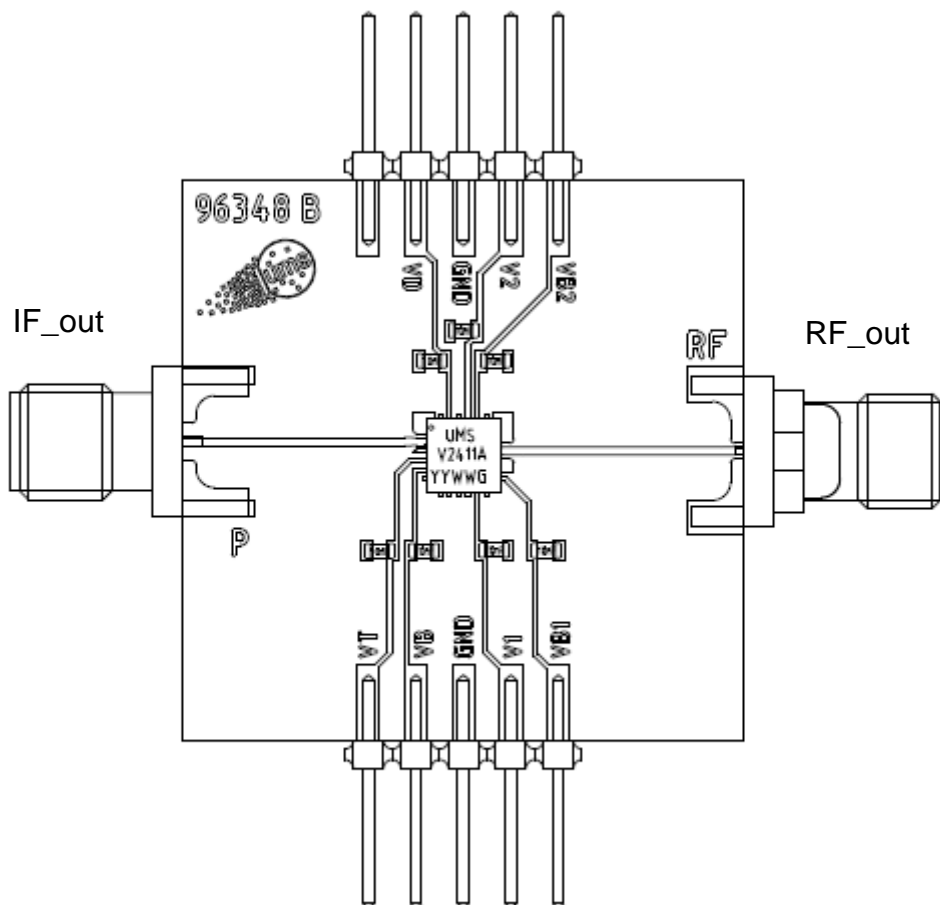
The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation motherboard".



## Evaluation mother board:

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF  $\pm$ 10% are recommended for all DC accesses.
- See application note AN0017 for details.

Recommended Test Fixture (Ref. 96348 B) for measurements over Temperature Range



- 7 capacitors 0603 (1 $\mu$ F)

**Recommended package footprint**

Refer to the application note AN0017 available at <http://www.ums-gaas.com> for package footprint recommendations.

**SMD mounting procedure**

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

**Recommended environmental management**

Refer to the application note AN0019 available at <http://www.ums-gaas.com> for environmental data on UMS package products.

**Recommended ESD management**

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

## Notes

## Ordering Information

QFN 4x4 RoHS compliant package: CHV2411aQDG/XY  
Stick: XY = 20      Tape & reel: XY = 21

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