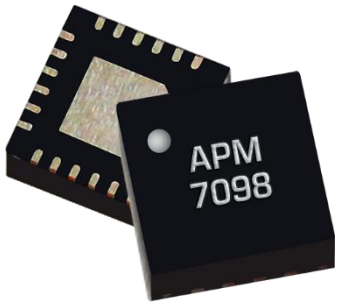
0.1-22 GHz Surface Mount Low Phase Noise Amplifier APM-7098SM



1. Device Overview

1.1 General Description

The APM-7098SM is a broadband low phase noise LO driver amplifier designed to provide a saturated +23 dBm output power with low DC power consumption. This amplifier uses GaAs HBT technology for low phase noise, and is optimized to provide enough power to drive the LO port of an S-diode mixer from 100 MHz to 20 GHz or of an H or L-diode mixer from 100 MHz to 30 GHz. This amplifier can be operated with a variety of bias conditions for both low and high-power applications. The APM-7098SM is packaged in a compact 4 mm QFN for surface mount integration on circuit board-based systems.

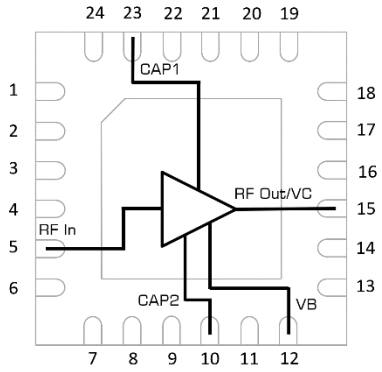
1.2 Features

- -165 dBc/Hz phase noise at 10 kHz offset frequency
- +23 dBm output power
- Low DC power consumption
- Positive-only biasing
- No sequencing required
- Unconditionally stable

1.3 Applications

- Mobile test and measurement equipment
- Radar and satellite communications
- 5G Transceivers
- Driver amplifier for S, H, and L – diode mixers
- NLTL Driver
- Suitable as a T3 mixer driver

1.4 Functional Block Diagram



1.5 Part Ordering Options[1]

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
APM-7098SM	4x4 mm Surface Mount	QFN	**RoHS**	Active	EAR99
EVAL-APM-7098SM	Connectorized Evaluation Fixture	EVAL	**RoHS**	Active	EAR99

[1] Refer to our website for a list of definitions for terminology presented in this table.

Table of Contents

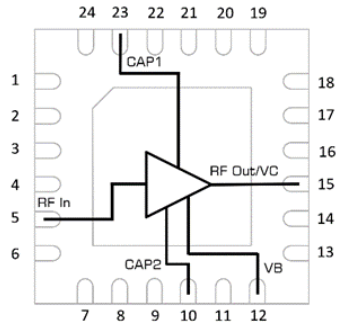
Revision History

Revision Code	Revision Date	Comment
-	September 2020	Datasheet Initial Release
A	January 2021	Updated Thermal Resistance and Max Input Power Spec, updated Min Spec table

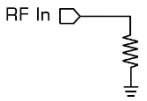
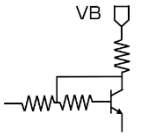
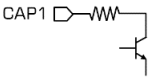
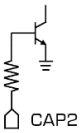
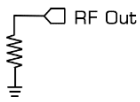
2. APM-7098SM Port Configurations and Functions

2.1 APM-7098SM Port Diagram

A port diagram of the APM-7098SM is shown below.



2.2 APM-7098SM Port Functions

Port	Function	Description	Equivalent Circuit for Package
5	RF Input	This is the RF input port of the device, and is RF matched to 50 Ω. This port is DC-coupled, and requires a blocking capacitor.	
12	Current Mirror Bias Port	Port 12 is the DC voltage bias pad for the current mirror that controls the collector current supplied to the amplifier. See section 3.6 for performance at different bias conditions.	
23	Off-Chip Cap Port 1	Port 23 allows the user to attach additional off chip bypass capacitance to provide adequate low frequency AC grounding termination to the input matching network. The value should be at least 100nF.	
10	Off-Chip Cap Port 2	Port 10 allows the user to attach additional off chip bypass capacitance to provide adequate low frequency AC grounding termination to the input matching network. The value should be at least 100nF.	
15	RF Output and Collector Supply Port	This is the amplifier's RF Output and positive VC supply voltage pin. It is RF matched to 50 Ω and is DC coupled. Must have less than 7:1 VSWR when operating.	
GND	Ground	IC backside must be connected to a DC/RF ground with high thermal and electrical conductivity.	

3. Specifications

3.1 Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may become inoperable or have a reduced lifetime.

Parameter	Maximum Rating	Units
Power Supply (Collector) Voltage (VC)	9	V
Power Supply (Collector) Current (Ic)	150	mA
Bias (Current Mirror) Voltage (VB)	9	V
RF Input Power	+16	dBm
Output Load VSWR	7:1	-
Operating Temperature	-40 to +85	°C
Storage Temperature	-65 to +150	°C
θ_{JC}, Junction to Ambient Thermal Resistance	63	°C/W
Max Junction Temperature for MTTF> 1E6 hours	125	°C
Max Power Dissipation for MTTF of 1E6 hours at 85°C Baseplate Temperature	630	mW

3.2 Package Information

Parameter	Details	Rating
ESD	Human Body Model (HBM), per MIL-STD-750, Method 1020	TBD
Weight	EVAL-APM-7098SM	43.6g

3.3 Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the electrical specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

	Min	Nominal	Max[2]	Units
T_A, Ambient Temperature	-40	+25	+85	°C
Positive DC Voltage (VC)	+5	+8	+9	V
Quiescent DC Current (Ic)	26	44	65	mA
DC Current with RF Input (Ic)	-	-	150	mA
Positive DC Current Mirror Voltage (VB)	+5	+7	+9	V
Input Power for Saturation	+7	+10	+16	dBm

3.4 Sequencing Requirements

There is no sequencing required to power up or power down the amplifier.

Amplifier must have an output load connected when operating.

[2] Maximum recommended operating current conditions without RF input applied. Please see typical performance plots on page 9 for relationship between RF input power and DC current draw.

3.5 Electrical Specifications

The electrical specifications apply at T_A=+25 °C in a 50 Ω system.

QFNs are 100% RF tested.

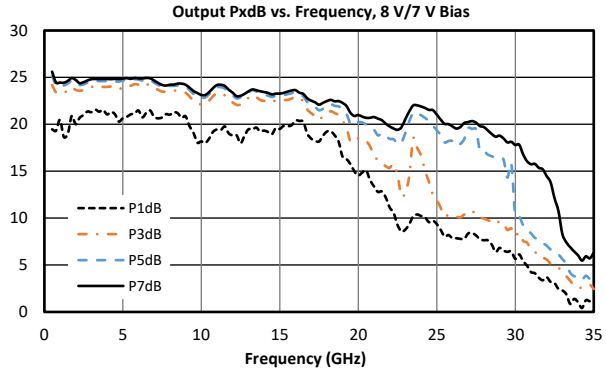
Parameter	Test Conditions	Frequency	Min	Typical	Units
Saturated Output Power[3]	8 V/7 V bias	100 MHz – 15 GHz	+17	+23	dBm
		15 GHz – 22 GHz		+12	
Small Signal Gain	8 V/7 V bias, -25 dBm Input Power	100 MHz – 15 GHz	+11	+15	dB
		15 GHz – 22 GHz		+10	
Input Return Loss		100 MHz – 22 GHz		11	
Output Return Loss		100 MHz – 22 GHz		10	
Noise Figure		100 MHz – 22 GHz		4.8	
Reverse Isolation		100 MHz – 22 GHz		38	
Collector Current[4], Ic	8 V/6 V	-		33	mA
	8 V/7 V	-		42	
Current Mirror Current, Ib	8 V/6 V	-		3	
	8 V/7 V	-		4	
Input IP3 (IIP3)	8 V/7 V bias, -20 dBm Input Power	100 MHz – 22 GHz		+8	dBm
Output IP3 (OIP3)		100 MHz – 22 GHz		+22	
Output P_{1dB}	8 V/7 V bias	100 MHz – 22 GHz		+19	
Input Power for Saturation	8 V/7 V bias	100 MHz – 22 GHz		+10	dBm
Phase Noise @ 10 kHz Offset	8 V/7 V bias, +10 dBm Input power	1 GHz		-165	dBc/Hz

[3] Saturated output power specification defined using the EVAL-APM-7098SM P_{7dB} compression curve shown in section 3.6

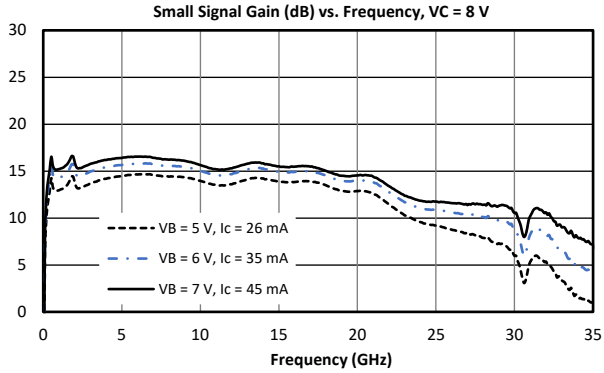
[4] Bias conditions for Ic and Ib tested with no RF input power. See section 3.6 for DC current vs. RF power. Bias conditions presented as VC/VB.

3.6 APM-7098SM Typical Performance Plots[5]

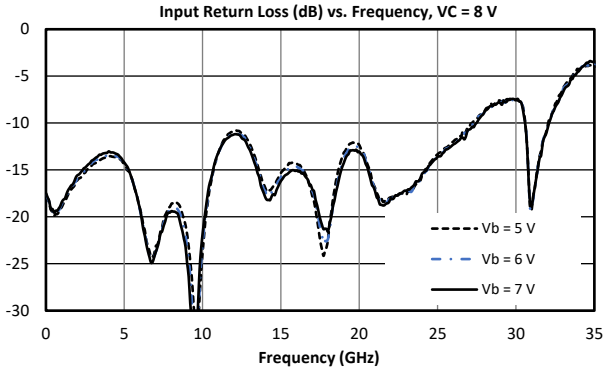
Output PxdB vs. Frequency, 8 V/7 V Bias



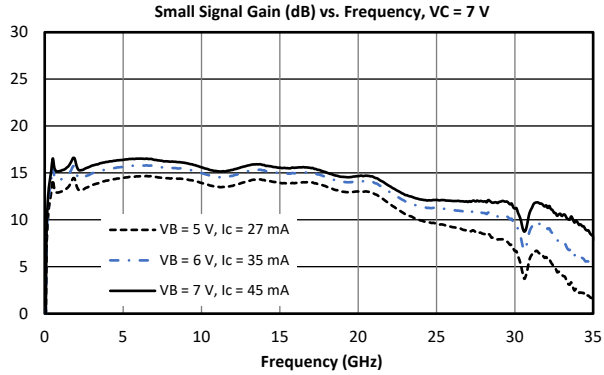
Small Signal Gain (dB) vs. Frequency, VC = 8 V



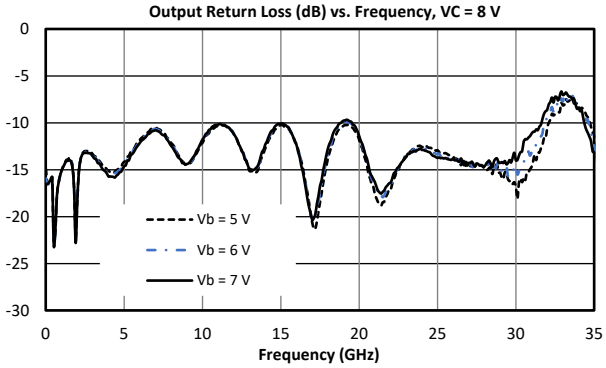
Input Return Loss (dB) vs. Frequency, VC = 8 V



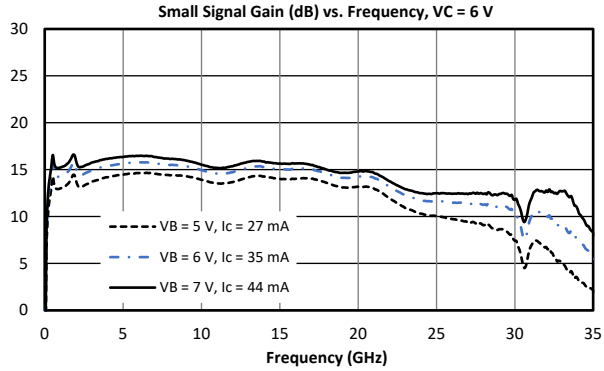
Small Signal Gain (dB) vs. Frequency, VC = 7 V



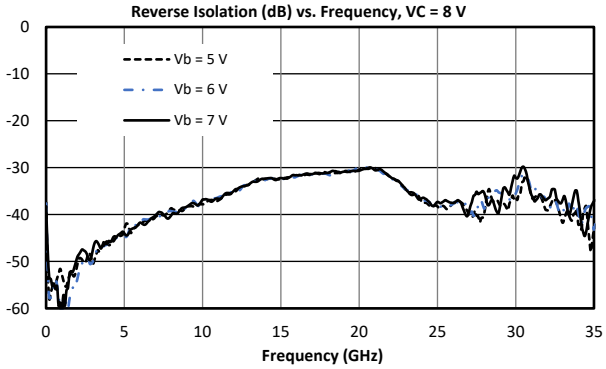
Output Return Loss (dB) vs. Frequency, VC = 8 V



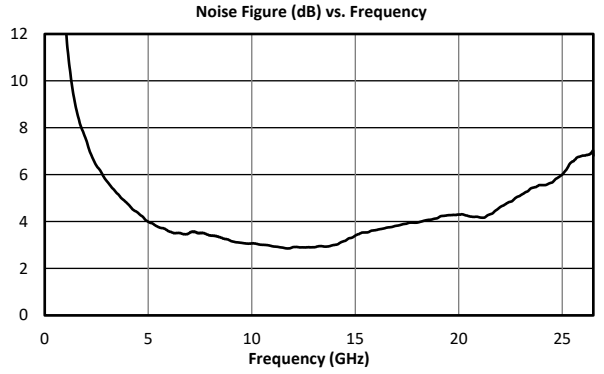
Small Signal Gain (dB) vs. Frequency, VC = 6 V



Reverse Isolation (dB) vs. Frequency, VC = 8 V

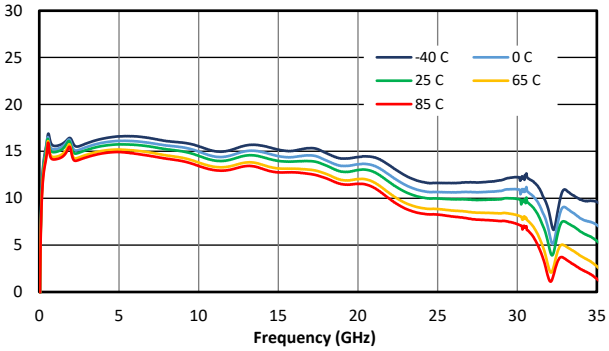


Noise Figure (dB) vs. Frequency

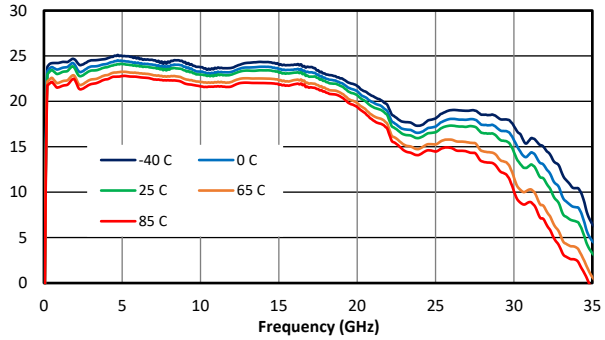


[5] APM-7098SM measurements taken in EVAL-APM-7098SM evaluation board.

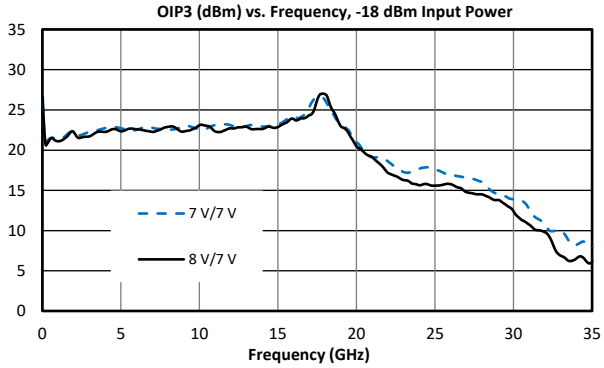
Small Signal Gain (dB) Over Temperature vs. Frequency, 8 V/7 V Bias



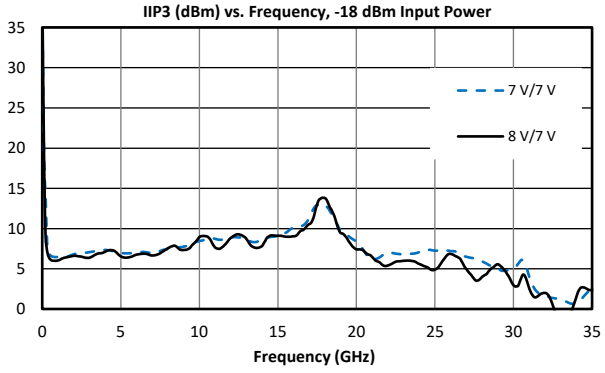
Saturated Output Power over Temperature vs. Frequency, 8 V/7 V



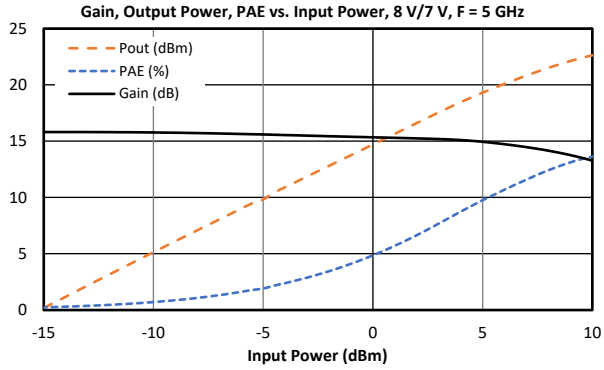
OIP3 (dBm) vs. Frequency, -18 dBm Input Power



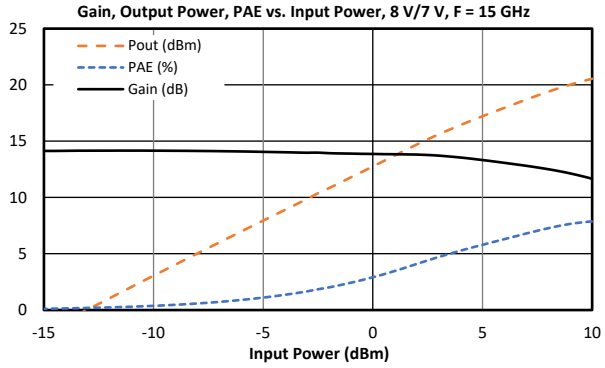
IIP3 (dBm) vs. Frequency, -18 dBm Input Power



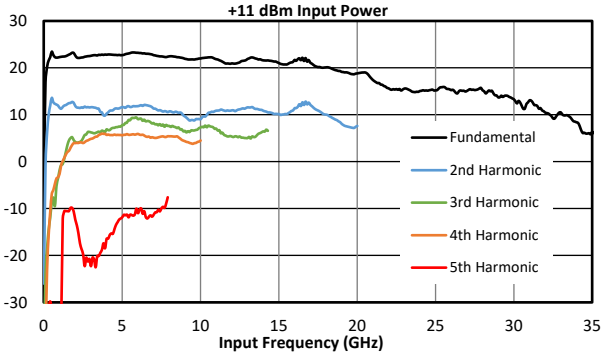
Gain, Output Power, PAE vs. Input Power, 8 V/7 V, F = 5 GHz

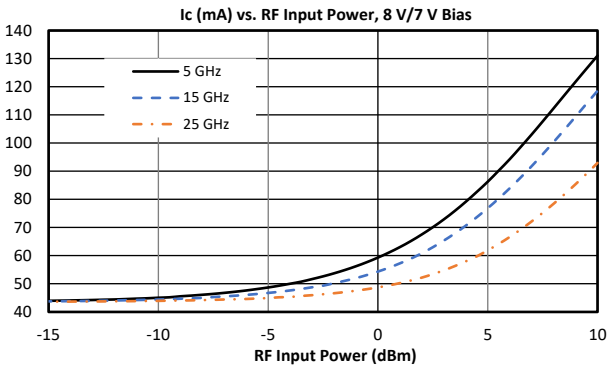


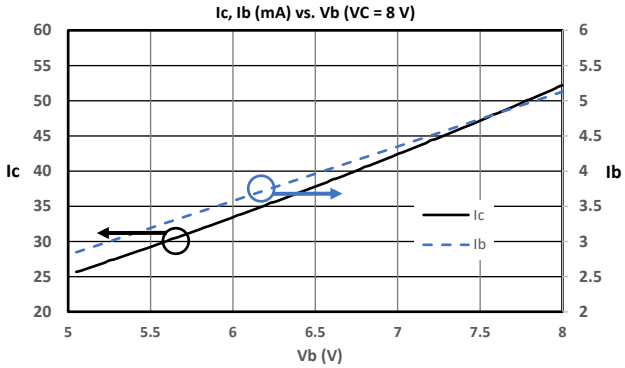
Gain, Output Power, PAE vs. Input Power, 8 V/7 V, F = 15 GHz



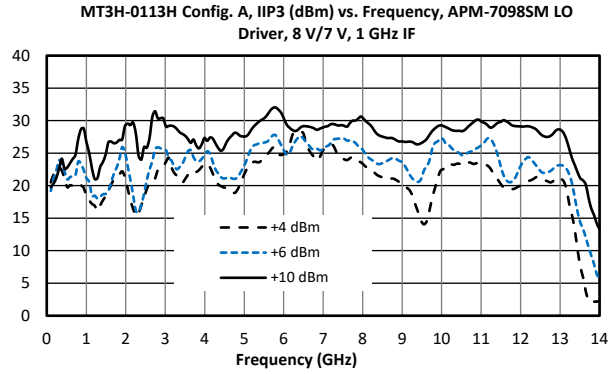
Harmonic Response (dBm) vs. Input Freq. 8 V/7 V Bias, +11 dBm Input Power

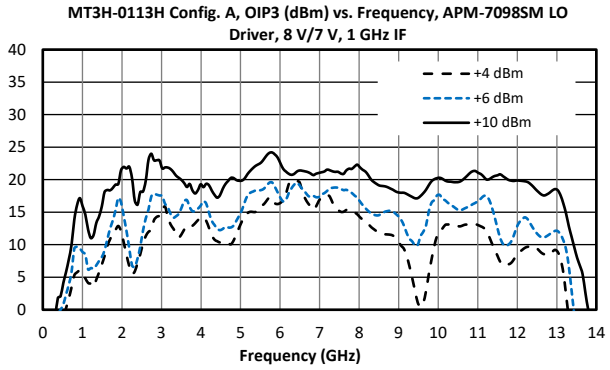


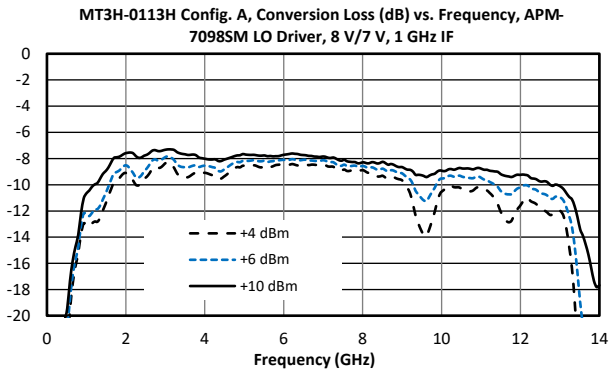




3.7 Typical Performance Plots of Marki MT3H-0113H Driven With APM-7098SM

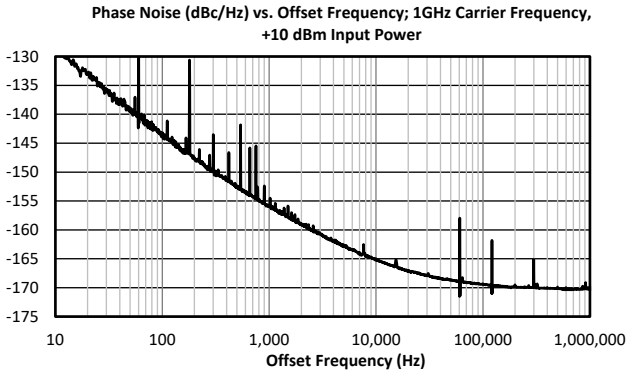




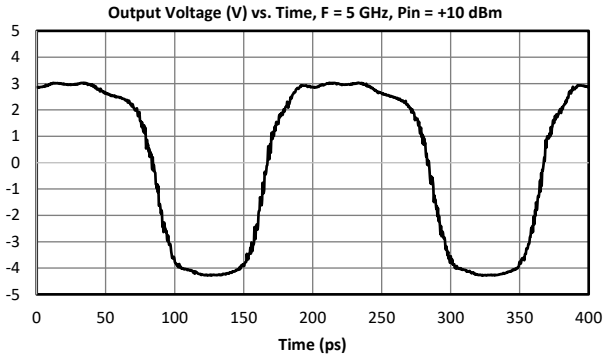


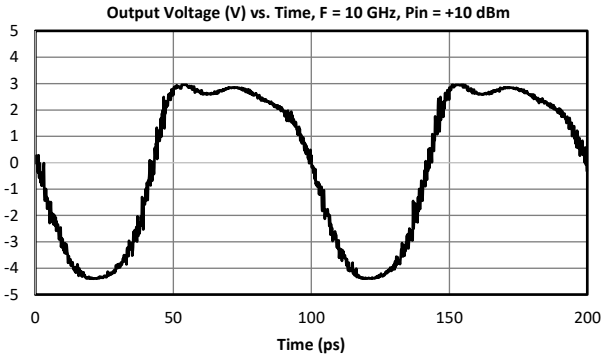
3.8 Connectorized Module APM-7098PA Performance Plots[6]

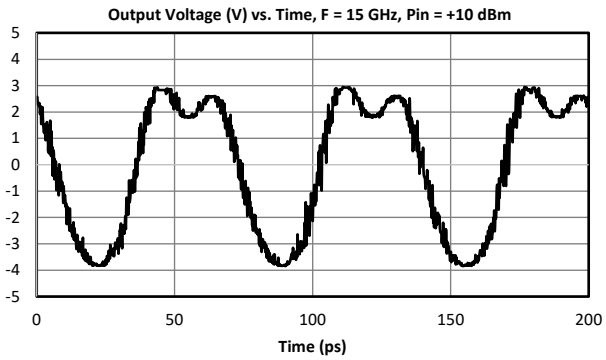
3.8.1 Phase Noise Plot



3.8.2 Time Domain Plots[7] [8]





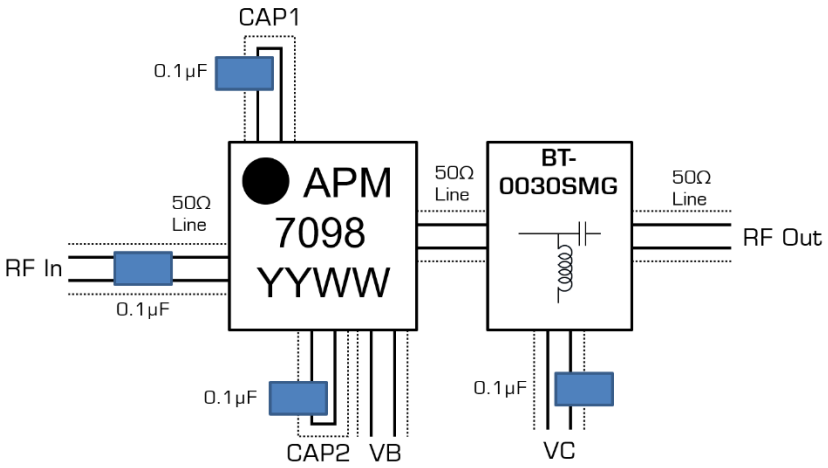


[6] Surface mount module APM-7098SM performance can be expected to be similar to connectorized module performance.
[7] Fast rise time is desirable for linear T3 mixer operation.
[8] Data taken using APM7098PA module

4. Application Information

4.1 APM-7098SM Application Circuit

Below is the recommended application circuit for the APM-7098SM.



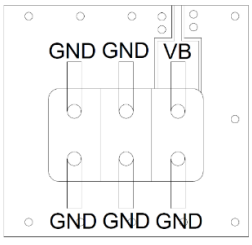
RF input and output should be soldered to 50 Ω traces. A suggested capacitor for the bypass and blocking capacitors would be 0402 0.1 uF 16 V surface mount capacitors.

4.2 Bypass Capacitors

The bypass capacitors on ports CAP1 and CAP2 provide AC ground to the internal circuits on the chip. These should not be DC coupled to prevent disruption of the internal biasing circuits, or outright damage to the chip. The value of these be at least 100nF to provide adequate AC grounding. An additional 100 nF bypass capacitor in series with a 20 Ω resistor should be added to the VC line to stabilize the amplifier and prevent power supply feedback to other parts on the board.

4.3 Evaluation Board Header Pinout

On the EVAL-APM-7098SM, there is a header for biasing the VB port. Only one pin is connected to VB, all other pins are soldered directly to the top side ground plane.

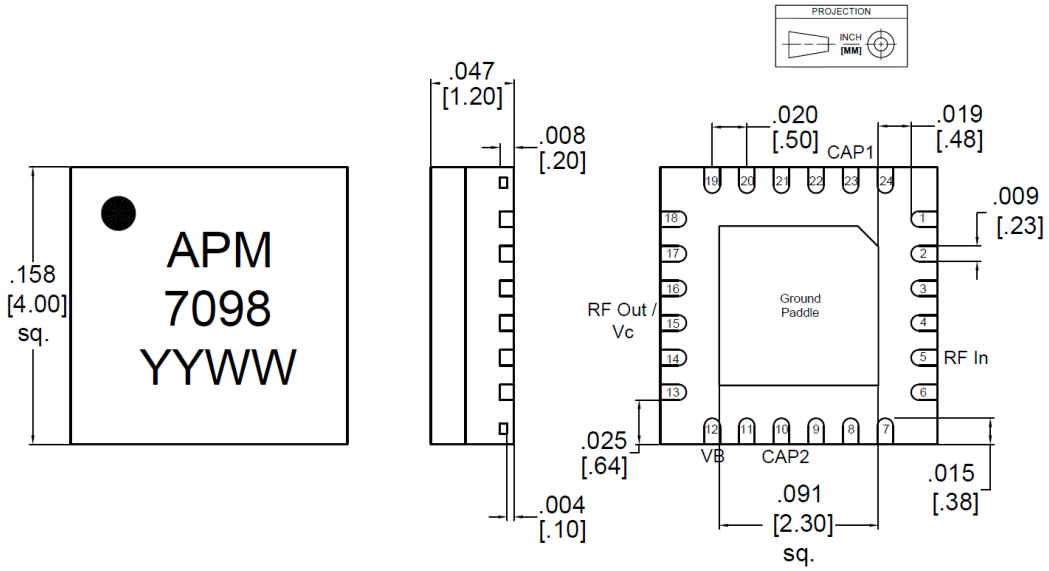


4.4 Harmonic Generation

The APM-7098's harmonic generation can be controlled by adjusting the supply and bias voltages. Decreasing the base voltage VB will increase the even harmonic generation and odd harmonic suppression. To increase the odd harmonic generation and even harmonic suppression, decrease the collector voltage VC. The optimal bias condition for even harmonic generation is VC = 8 V and VB = 5 V, while the optimal bias condition for odd harmonic generation is VC = 5 V and VB = 8 V.

5. Mechanical Data

5.1 APM-7098SM Package Outline Drawing



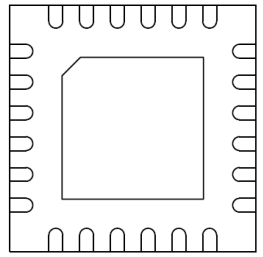
Pad #	Function
1	N/C
2	N/C
3	N/C
4	N/C
5	RF In
6	N/C
7	N/C
8	N/C
9	N/C
10	CAP2
11	N/C
12	VB
13	N/C
14	N/C
15	RF Out / VC
16	N/C
17	N/C
18	N/C
19	N/C
20	N/C
21	N/C
22	N/C
23	CAP1
24	N/C

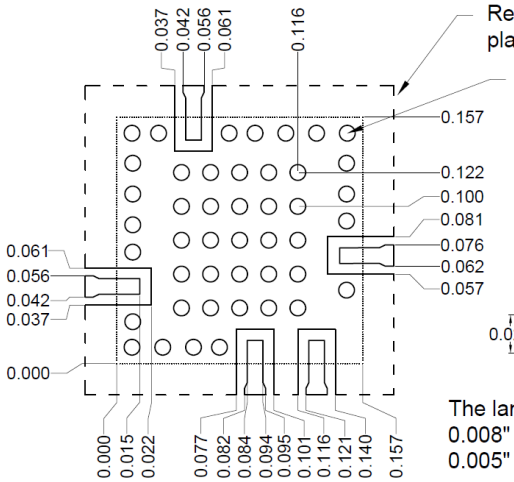
Notes:

1. Substrate Material is Plastic.
2. I/O Leads and Die Paddle are 0.05 microns Au over 0.02 microns Pd over 0.5 microns Ni.
3. All unconnected pins should be connected to PCB RF ground.

5.2 APM-7098SM Landing Pattern

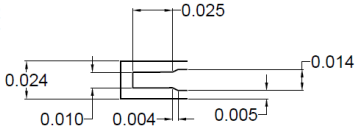
QFN 4mm Sample Drawing
X-Ray view





Recommended to have the ground plane flooded.

Ø0.010 Plated thru via. Recommended conductive or non-conductive fill, 50 PL. Vias can be added or reduced at PCB designer discretion.



The landing pattern is to be used on Rogers4003, 0.008" thick. Grounded coplanar wave guide with 0.005" slot,3 PL.

5.3 EVAL-APM-7098SM Outline