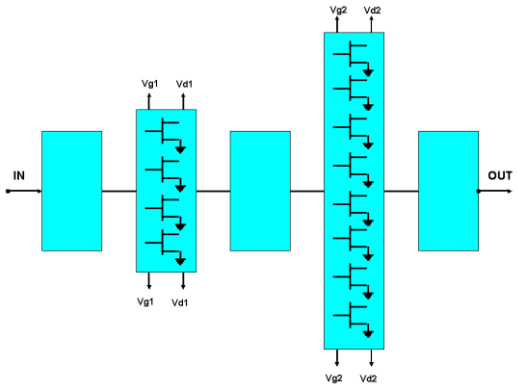
2-8GHz High Power Amplifier

GaAs Monolithic Microwave IC

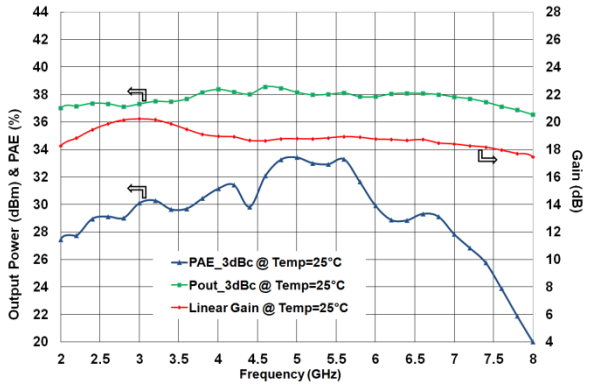
Description

The CHA6015-99F is a HPA that provides typically 37.5dBm output power on the frequency band 2-8GHz. The circuit is dedicated to defence applications and also well suited for a wide range of microwave applications and systems.
The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.



Main Features

- Broadband performances: 2-8GHz
- Linear Gain: 18.5dB
- Pout at 3dB compression : 37.5dBm
- PAE at 3dB compression : 29%
- DC bias: Vd=7Volt@Id=2A
- Chip size: 4.68x6.53x0.07mm



Main Electrical Characteristics

Tamb.= +25°C, Vd = 7V, Id (Quiescent) = 2A, CW

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	2		8	GHz
Gain	Linear Gain		18.5		dB
P_{3dB}	Output Power @3dB gain compression		37.5		dBm
PAE_{3dB}	Power Added Efficiency @ 3dB gain compression		29		%

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Electrical Characteristics

Tamb.= +25°C, Vd = +7V , Id (Quiescent)=2A, CW

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency	2		8	GHz
G	Small signal gain		18.5		dB
RLin	Input Return Loss (1)		6		dB
RLout	Output Return Loss		12		dB
P_{1dB}	Ouput power @ 1dBcomp		36.5		dBm
P_{3dB}	Output power @ 3dBcomp		37.5		dBm
PAE_{3dB}	Power Added Efficiency @ 3dBcomp		29		%
Id_{3dB}	Supply drain current @ 3dBcomp		2.8		A
Vd1, Vd2	Drain supply voltage		7		V
Id	Supply quiescent current (2)		2		A
Vg	Gate supply voltage		-0.45		V

(1) HPA designed to be used in balanced configuration.
(2) Parameter can be adjusted by tuning of Vg.

Note: These values are representative of measurements in test fixture with an equivalent RF wire bonding of 0.25nH on each RF port.

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Cmp	Compression level	6	dB
Pin_max	Maximum peak input power overdrive	27	dBm
Vd	Supply voltage (2)	9.5	V
Id	Supply quiescent current	3	A
Id_sat	Supply current in saturation	4	A
Vg	Supply voltage	0	V
Tj	Maximum junction temperature (3)	175	°C
Ta	Operational temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Without RF input power.

(3) At backside temperature of 85°C, Rth_ equivalent of the die is 4°C/W.

The Rth_equivalent is extrapolated, taking into account the full DC power and the channel temperature increase on the worst transistor.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
Vd1	5,15	Drain supply voltage stage 1	7	V
Vd2	9,11	Drain supply voltage stage 2	7	V
Vg1	3,17	Gate supply voltage stage 1 (1)	-0.45	V
Vg2	6,14	Gate supply voltage stage 2 (1)	-0.45	V

(1) Vg1=Vg2 to be adjusted to settle the total quiescent current ID to 2A

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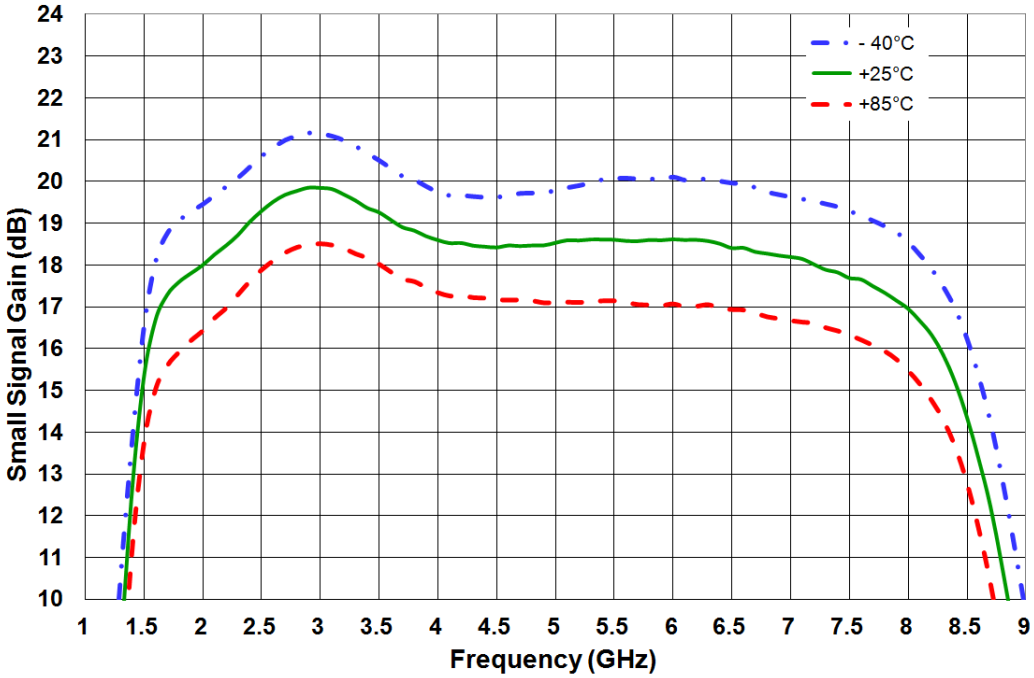
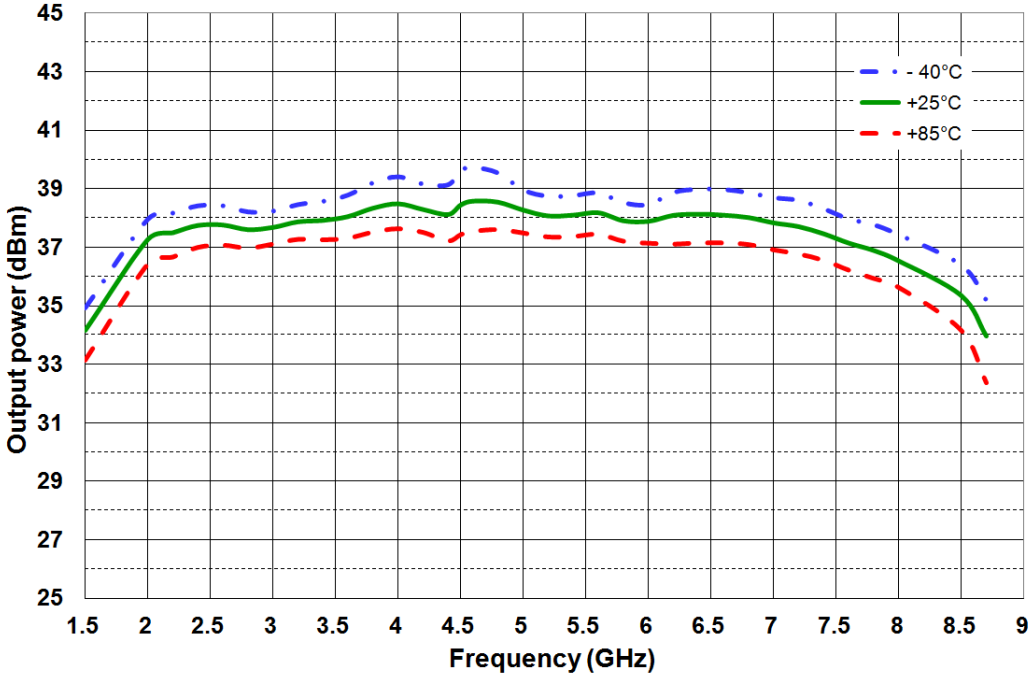
Typical Board Measurements

Vd =7V, Id (Quiescent) =2A, CW

Linear Gain versus frequency



Output power versus frequency
for input power=23dBm at -40°C / 25°C / 85°C



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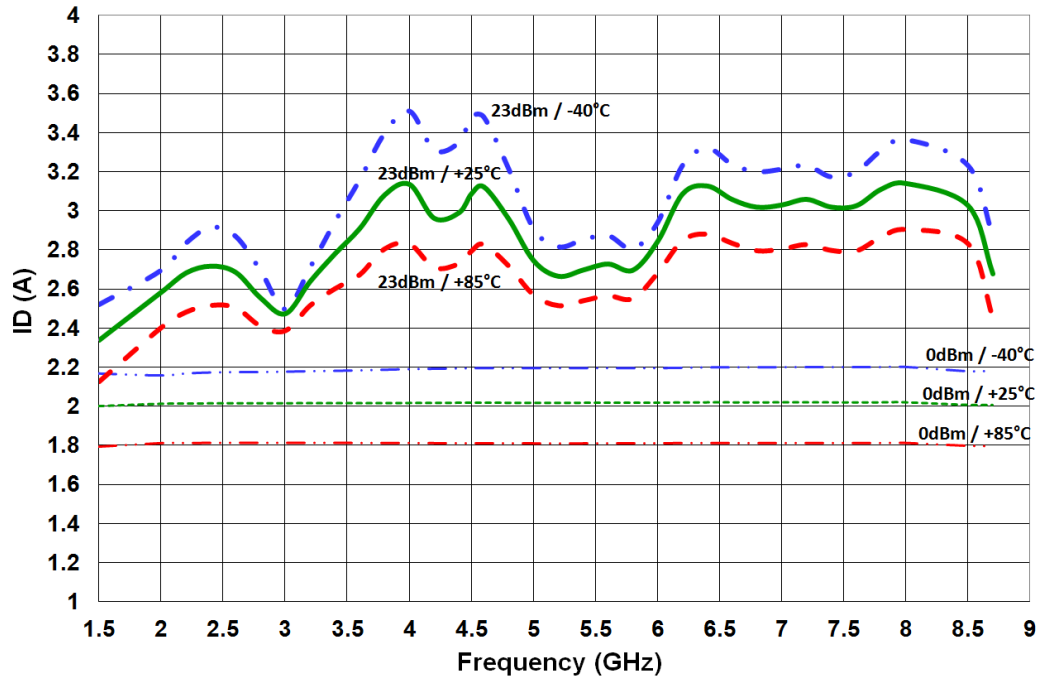
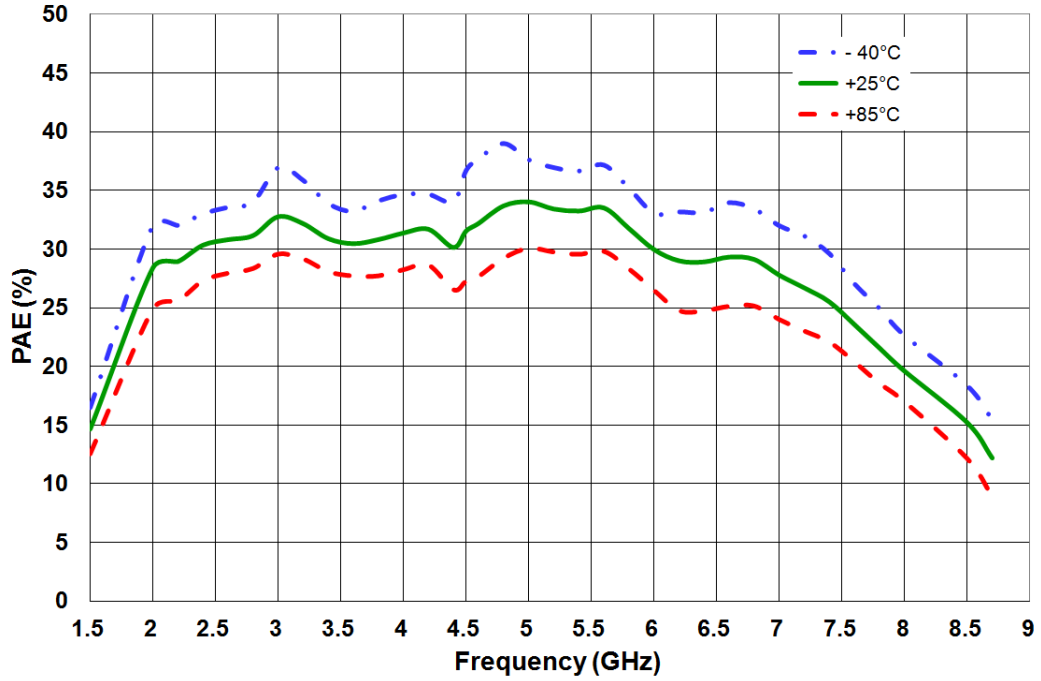
Typical Board Measurements

Vd =7V, Id (Quiescent) =2A, CW

Drain current versus frequency
for input power=0dBm and 23dBm at -40°C / 25°C / 85°C



Power added efficiency versus frequency
for input power=23dBm at -40°C / 25°C / 85°C



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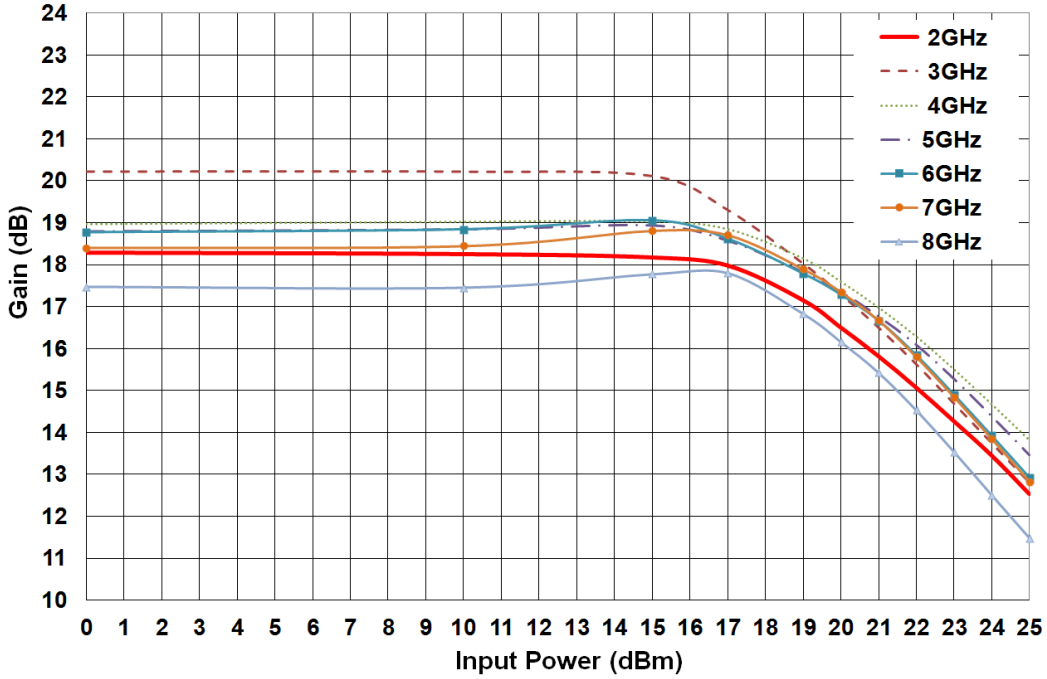
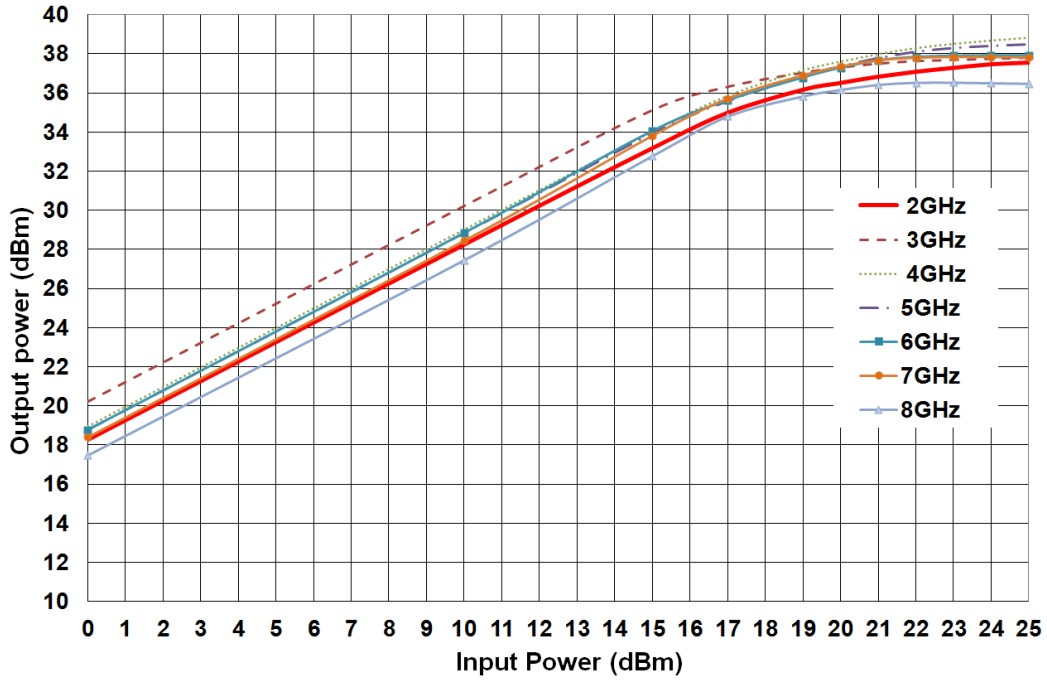
Typical Board Measurements

Vd =7V, Id (Quiescent) =2A, CW

Gain versus input power at 25°C



Output power versus input power at 25°C



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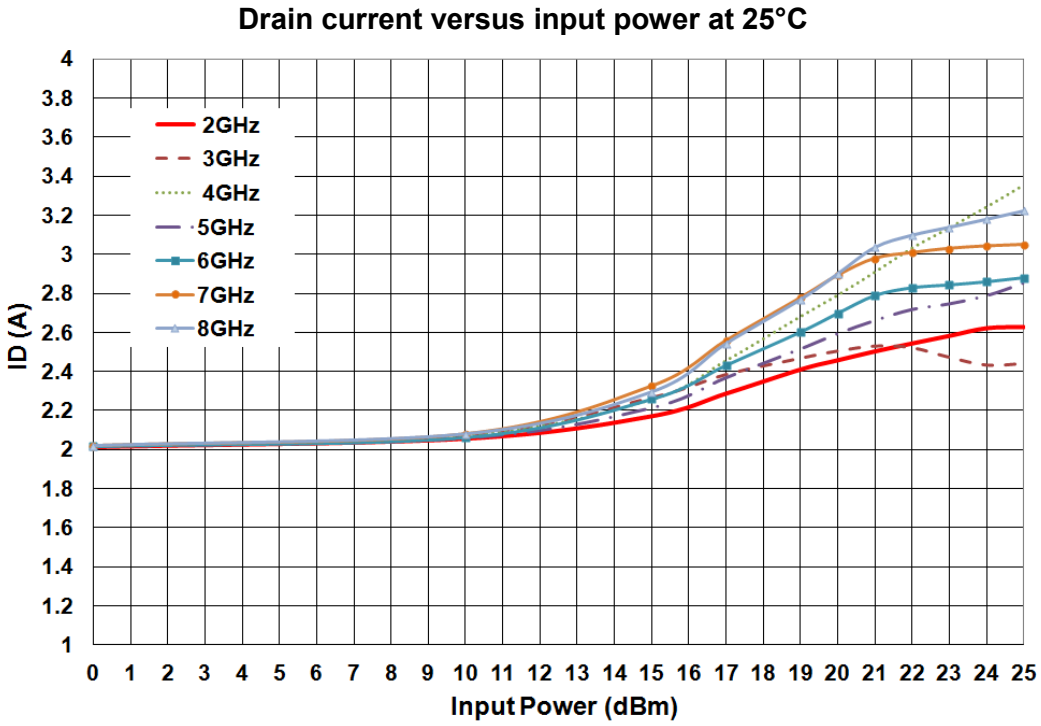
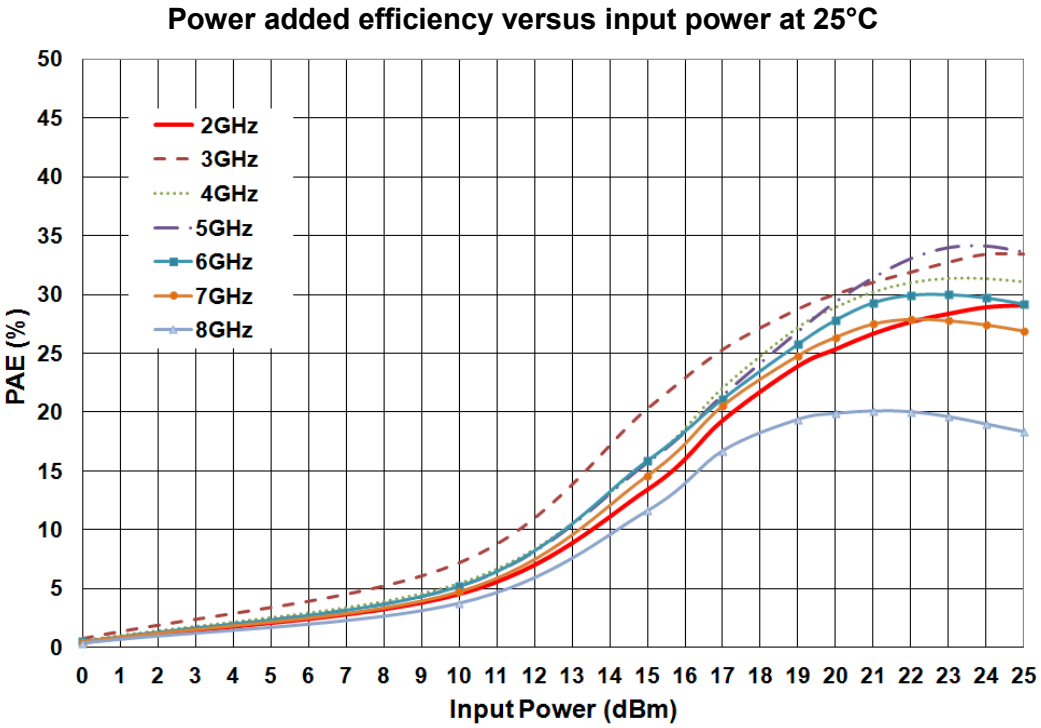
Typical Board Measurements

Vd =7V, Id (Quiescent) =2A, CW





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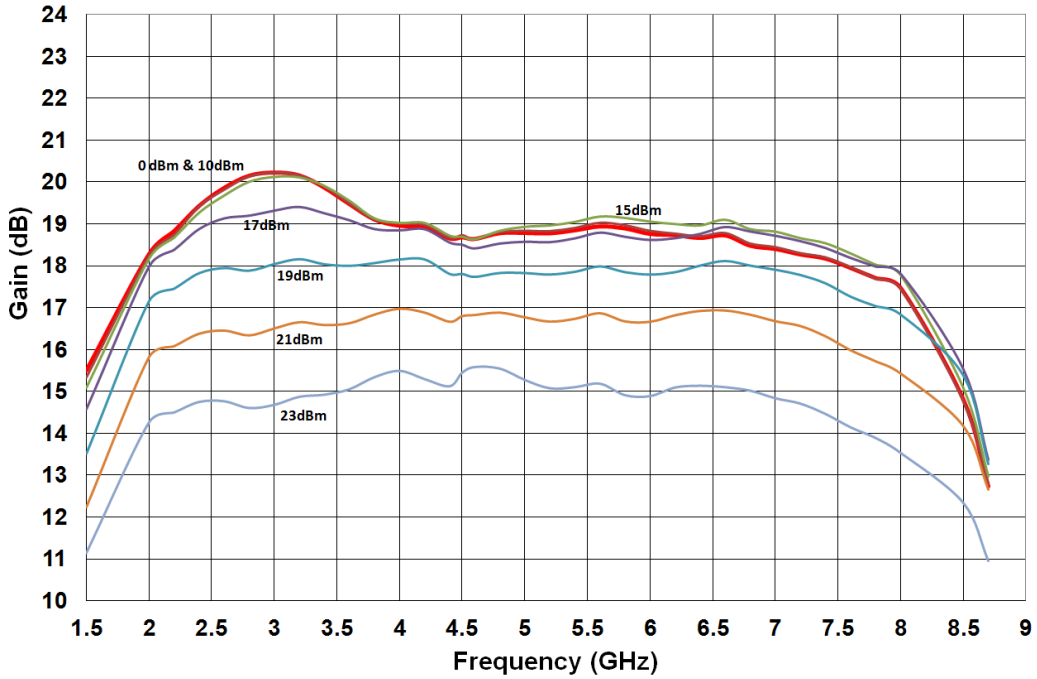
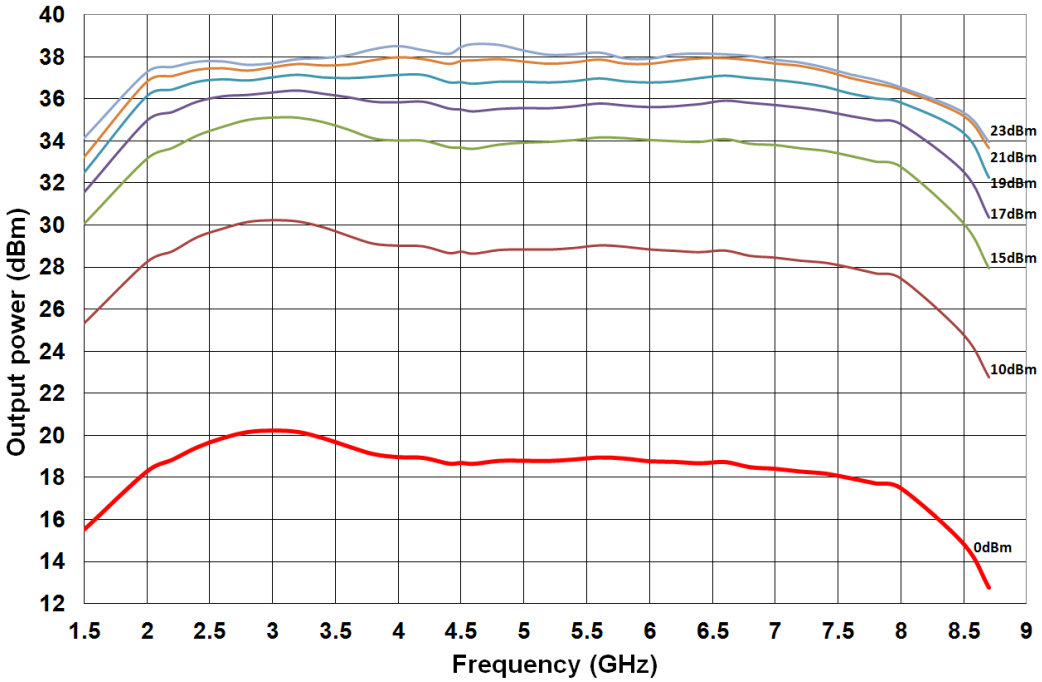
Typical Board Measurements

Vd =7V, Id (Quiescent) =2A, CW

Gain versus frequency at 25°C
for input power=0/10/15/17/19/21/23dBm



Output power versus frequency at 25°C
for input power=0/10/15/17/19/21/23dBm



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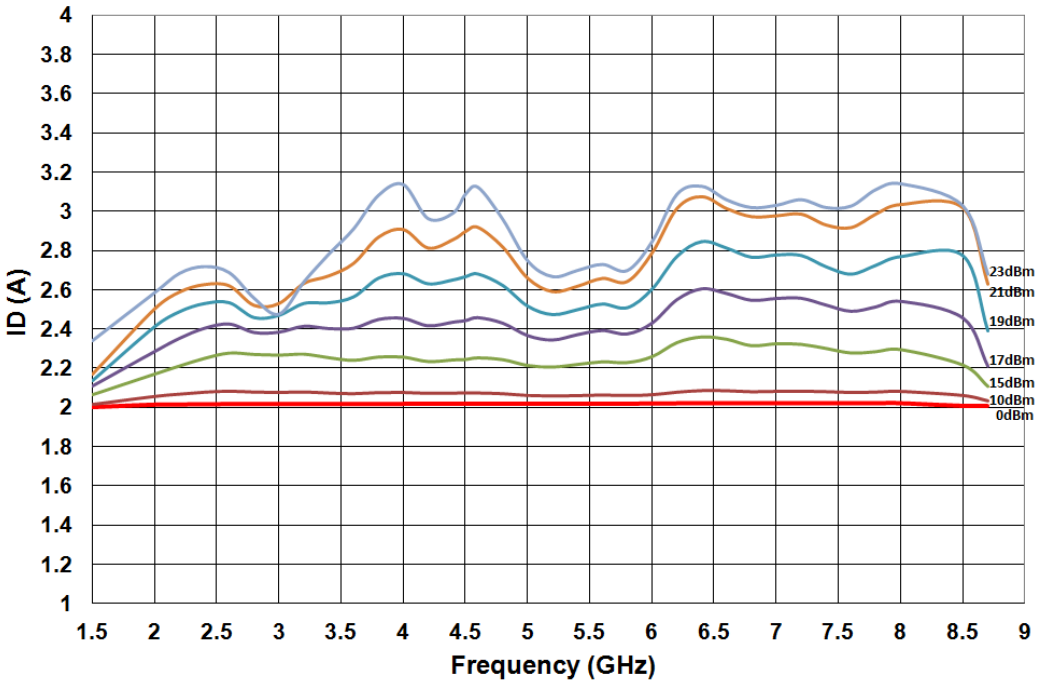
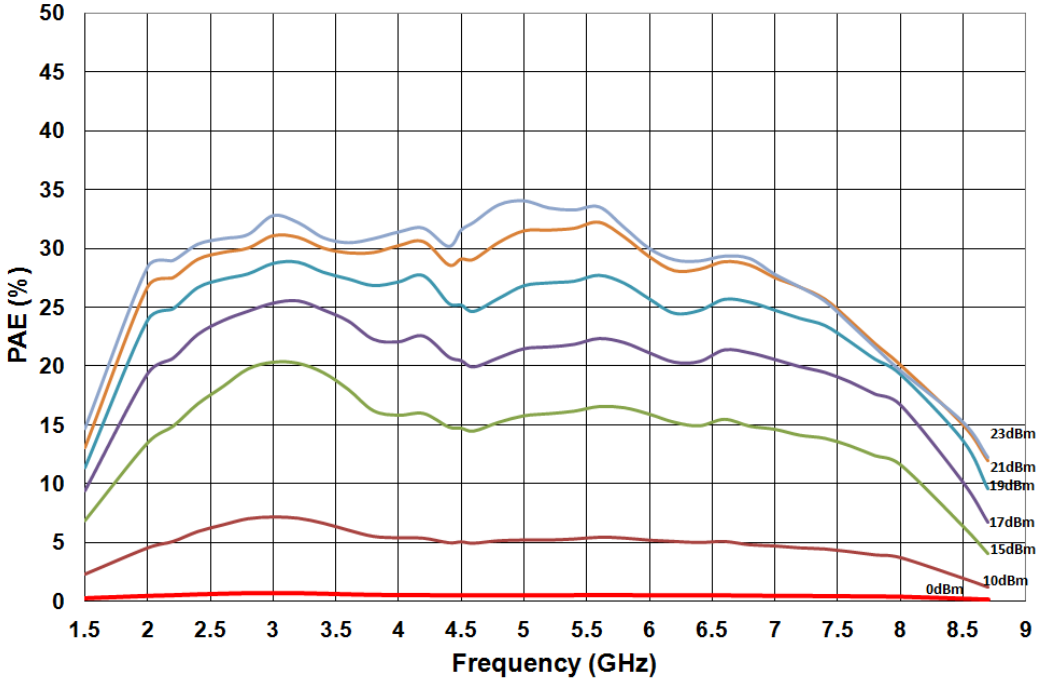
Typical Board Measurements

Vd =7V, Id (Quiescent) =2A, CW

Drain current versus frequency at 25°C
for input power=0/10/15/17/19/21/23dBm



Power added efficiency versus frequency at 25°C
for input power=0/10/15/17/19/21/23dBm



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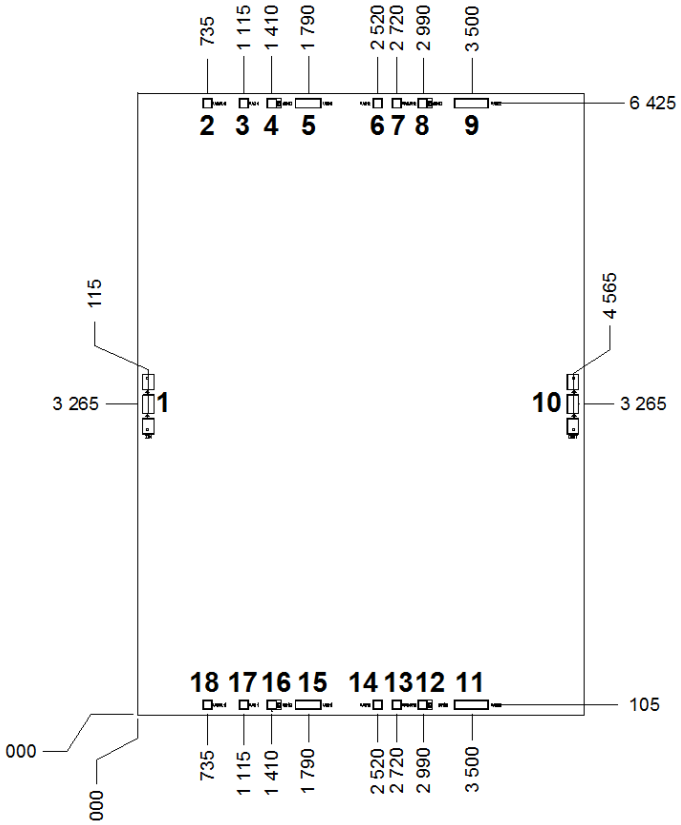
Mechanical data



All dimensions are in micrometers

Chip size	= 6530x4680
Chip thickness	= 70µm ±10µm
RF pads (1, 10)	= 200 x 122µm
DC pads (3, 6, 14, 17)	= 100 x 100µm
DC pads (5, 15)	= 270 x 100µm
DC pads (9, 11)	= 355 x 100µm

Chip width and length are given with a tolerance of ±35µm

Pin number	Pin name	Description
1	**IN**	**Input RF**
2, 18	VGR1	NC
3, 17	VG1	Vg1
4, 8, 12, 16	GND	ground
5, 15	VD1	Vd1
6, 14	VG2	Vg2
7, 13	VGR2	NC
9, 11	VD2	Vd2
10	OUT	Output RF

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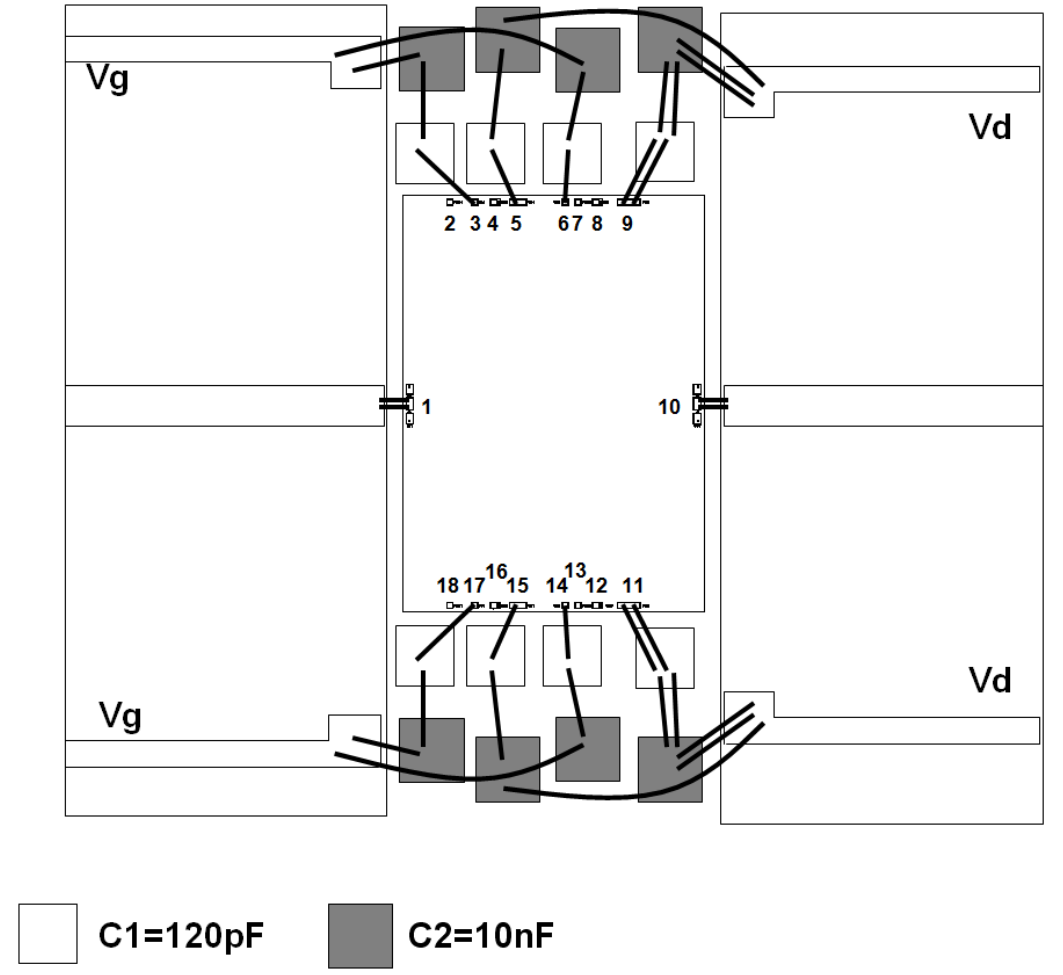
Recommended assembly plan



Recommended circuit bonding table

Port	Connection	External capacitor
IN	Inductance (Lbonding) = 0.25nH 2 gold wires with diameter of 25µm (typical length of 200µm)	
OUT	Inductance (Lbonding) = 0.25nH 2 gold wires with diameter of 25µm (typical length of 200µm)	
Vg	Inductance ≤ 1nH	C1 ~ 120pF, C2 ~10nF
Vd (1)	Inductance ≤ 1nH	C1 ~ 120pF, C2 ~ 10nF

(1) 2 gold wires with diameter of 25µm per pin are necessary to connect Vd2 (Pins 9 and 11)

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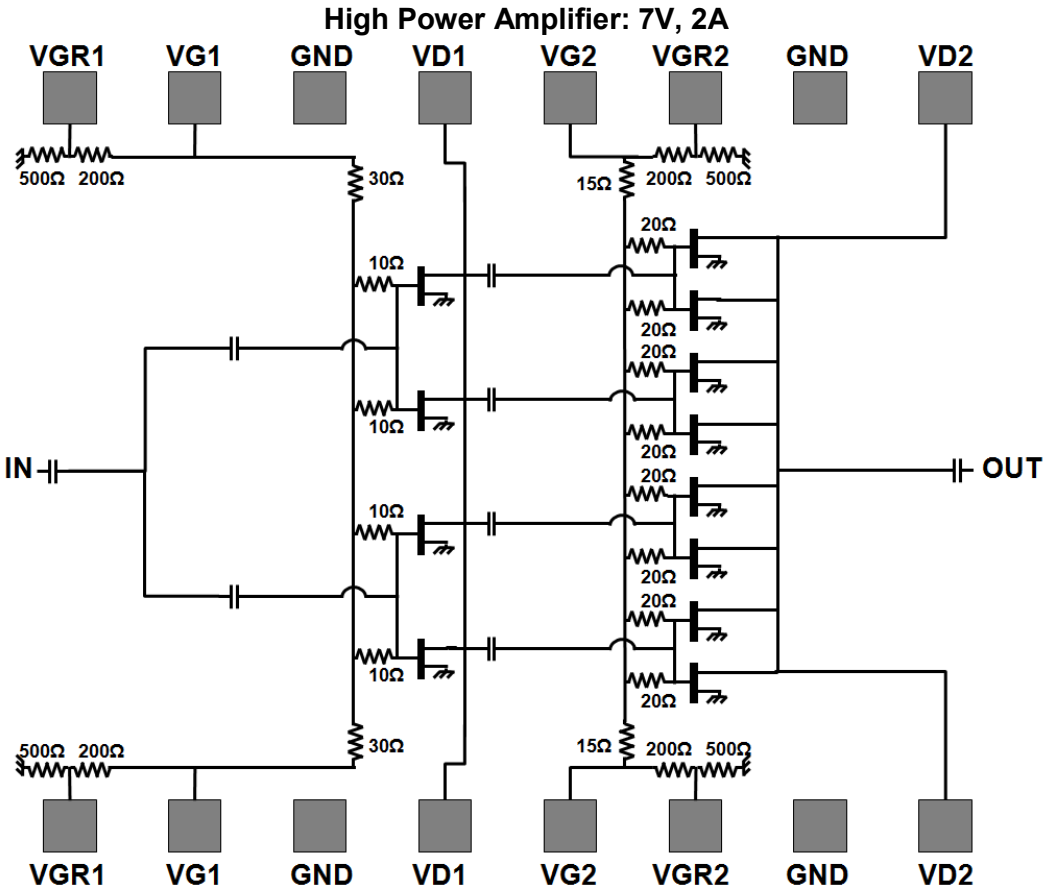
DC Schematic



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Notes

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Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Ordering Information

Chip form:	CHA6015-99F/00

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