25W Power Packaged Transistor

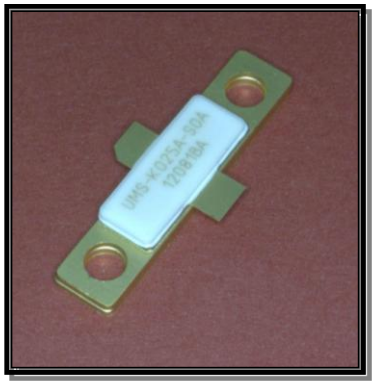
GaN HEMT on SiC

Description

The CHK025A-SOA is an unmatched packaged Gallium Nitride High Electron Mobility Transistor. It offers general purpose and broadband solutions for a variety of RF power applications. It is well suited for multi-purpose applications such as radar and telecommunication.

The CHK025A-SOA is developed on a 0.5µm gate length GaN HEMT process. It requires an external matching circuitry.

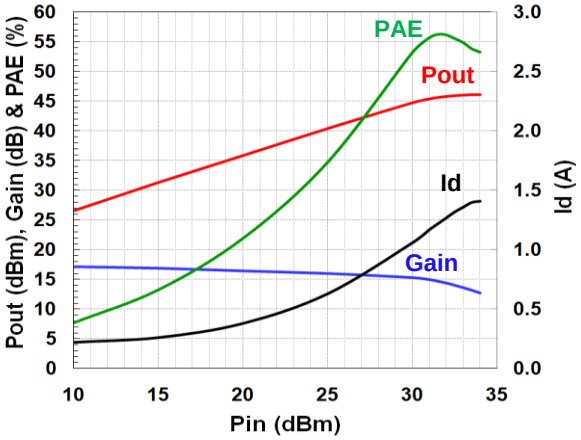
The CHK025A-SOA is available as a ceramic-metal flange power package providing low parasitic and low thermal resistance.



Main Features

- Wide band capability: up to 5GHz
- Pulsed and CW operating modes
- High power: > 25W
- High Efficiency: up to 70%
- DC bias: V_{DS} =50V @ I_{D_Q} =200mA
- MTTF > 10^6 hours @ Tj=200°C
- RoHS Flange Ceramic package
- ESD-HBM: Class1B (500V)
- ESD-MM: Class B (350V)

V_{DS} = 50V, I_{D_Q} = 200mA, Freq=4GHz
Pulsed mode



Intrinsic performances of the packaged device

Main Electrical Characteristics

Tcase= +25°C, **Pulsed mode**, F = 4GHz, V_{DS}=50V, I_{D_Q}=200mA

Symbol	Parameter	Min	Typ	Max	Unit
G_{SS}	Small Signal Gain	15	17		dB
P_{SAT}	Saturated Output Power	30	38		W
PAE	Max Power Added Efficiency	55	60		%
G_{PAE_MAX}	Associated Gain at Max PAE		13		dB

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Recommended DC Operating Ratings

Tcase= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{DS}	Drain to Source Voltage	20		50	V	
V_{GS_Q}	Gate to Source Voltage		-1.9		V	V_D=50V, I_{D_Q}=200mA
I_{D_Q}	Quiescent Drain Current		0.2	0.65	A	V_D=50V
I_{D_MAX}	Drain Current		1.3	(1)	A	V_D=50V, Compressed mode
I_{G_MAX}	Gate Current (forward mode)		0	8	mA	Compressed mode
T_{j_MAX}	Junction temperature			200	°C	

(1) Limited by dissipated power

DC Characteristics

Tcase= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_P	Pinch-Off Voltage	-3	-2	-1	V	V_D=50V, I_D= I_{DSS} /100
I_{D_SAT}	Saturated Drain Current		5.4 (1)		A	V_D=7V, V_G=2V
I_{G_leak}	Gate Leakage Current (reverse mode)	-1.5			mA	V_D=50V, V_G=-7V
V_{BDS}	Drain-Source Break-down Voltage		180		V	V_G=-7V, I_D=20mA
R_{TH}	Thermal Resistance (2)		3.7		°C/W	

(1) For information, limited by I_{D_MAX} , see on Absolute Maximum Ratings

(2) CW mode, reference = package back-side

RF Characteristics (CW)

Tcase= +25°C, **CW mode**, F = 4GHz, V_{DS}=50V, I_{D_Q}=200mA

Symbol	Parameter	Min	Typ	Max	Unit
G_{SS}	Small Signal Gain	14	16	-	dB
P_{SAT}	Saturated Output Power	28	35	-	W
PAE	Max Power Added Efficiency	50	55	-	%
G_{PAE_MAX}	Associated Gain at Max PAE		12	-	dB

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RF Characteristics (Pulsed)

Tcase= +25°C, **Pulse mode** [1], F = 4GHz, V_{DS}=50V, I_{D_Q}=200mA

Symbol	Parameter	Min	Typ	Max	Unit
G_{SS}	Small Signal Gain	15	17		dB
P_{SAT}	Saturated Output Power	30	38		W
PAE	Max Power Added Efficiency	55	60		%
G_{PAE_MAX}	Associated Gain at Max PAE		13		dB

[1] Input RF and gate voltage are pulsed. Conditions are 25µs width, 10% duty cycle and 1µs offset between RF and DC pulse.

These values are the intrinsic performance of the packaged device. They are deduced from measurements and simulations. They are considered in the reference plane defined by the leads of the package, at the connection interface with the PCB.

The typical performance achievable in more than 20% frequency band around 4GHz was demonstrated using the reference board 61500252 presented hereafter.

Absolute Maximum Ratings [1]

Tcase= +25°C[1], [2], [3]

Symbol	Parameter	Rating	Unit	Note
V_{DS}	Drain-Source Voltage	60	V	
V_{GS_Q}	Gate-Source Voltage	-10, +2	V	[6]
I_{G_MAX}	Maximum Gate Current in forward mode	48	mA	
I_{G_MIN}	Maximum Gate Current in reverse mode	-4	mA	
I_{D_MAX}	Maximum Drain Current	4	A	[4]
P_{IN}	Maximum Input Power (typical)	37	dBm	[5]
T_j	Junction Temperature	230	°C	
T_{STG}	Storage Temperature	-55 to +150	°C	
T_{Case}	Case Operating Temperature	See note	°C	[4]

[1] Operation of this device above anyone of these parameters may cause permanent damage.
[2] Duration < 1s.
[3] The given values must not be exceeded at the same time even momentarily for any parameter, since each parameter is independent from each other, otherwise deterioration or destruction of the device may take place.
[4] Max junction temperature must be considered
[5] @4GHz -Linked to and limited by I_{G_MAX} & I_{G_MIN} values
[6] V_{GS_Q} max limited by I_{D_MAX} and I_{G_MAX} values

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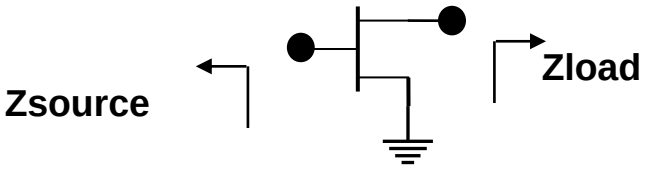
Simulated Source and Load Impedance

V_{DS} = 50V, I_{D_Q} = 200mA



Frequency (MHz)	Source	Load
1000	4.3 + j4	10.9 + j22.45
2000	1.5 - j1.5	7.2 + j10.7
3000	2.7 - j4.65	4.8 + j1.01
4000	3.9 - j8.6	4.27 - j0.38
4500	6.4 - j11	3.44 - j1.87
5000	7.8 - j3.2	2.5 - j3.8

These values are given in the reference plane defined by the connection between the package leads and the PCB. A gap of 200µm is considered between the edge of the package and the PCB.

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Typical S-parameters

Tcase= +25°C, CW mode, V_D=50V, I_{D_Q}=200mA, Phase S(i,j) in °

Freq (GHz)	Mag S(1,1)	Phase S(1,1)	Mag S(2,1)	Phase S(2,1)	Mag S(1,2)	Phase S(1,2)	Mag S(2,2)	Phase S(2,2)
0.25	0.89	-129.4	30.31	104.2	0.014	17.9	0.39	-86.2
0.50	0.88	-154.7	15.86	83.2	0.014	0.7	0.39	-106.8
0.75	0.88	-164.6	10.37	70.0	0.013	-8.1	0.45	-117.2
1.00	0.89	-170.5	7.50	59.4	0.011	-13.0	0.52	-125.1
1.25	0.90	-174.7	5.75	50.2	0.010	-14.5	0.59	-132.0
1.50	0.90	-178.3	4.58	42.2	0.008	-11.4	0.64	-138.2
1.75	0.91	178.6	3.75	34.9	0.007	-2.1	0.69	-143.8
2.00	0.92	175.6	3.14	28.4	0.006	14.0	0.73	-148.8
2.25	0.92	172.7	2.68	22.4	0.006	32.0	0.76	-153.5
2.50	0.93	170.0	2.33	16.8	0.007	45.4	0.79	-157.7
2.75	0.93	167.2	2.06	11.6	0.009	53.1	0.81	-161.7
3.00	0.93	164.4	1.84	6.7	0.011	56.8	0.83	-165.3
3.25	0.93	161.6	1.67	2.1	0.013	58.1	0.84	-168.8
3.50	0.93	158.7	1.53	-2.5	0.015	57.9	0.85	-172.1
3.75	0.93	155.7	1.42	-6.8	0.018	56.9	0.86	-175.3
4.00	0.93	152.6	1.33	-11.2	0.020	55.2	0.87	-178.4
4.25	0.93	149.4	1.26	-15.5	0.023	53.1	0.87	178.6
4.50	0.92	145.9	1.21	-19.8	0.025	50.8	0.88	175.6
4.75	0.92	142.2	1.17	-24.2	0.028	48.1	0.88	172.7
5.00	0.91	138.2	1.14	-28.7	0.031	45.2	0.88	169.7
5.25	0.91	133.8	1.13	-33.4	0.035	42.0	0.88	166.7
5.50	0.90	129.0	1.12	-38.3	0.038	38.6	0.88	163.6
5.75	0.89	123.7	1.13	-43.6	0.042	34.8	0.88	160.4
6.00	0.88	117.7	1.14	-49.2	0.047	30.6	0.88	157.1
6.25	0.87	110.9	1.17	-55.3	0.052	26.0	0.88	153.6
6.50	0.86	103.2	1.20	-62.0	0.058	20.9	0.88	149.9
6.75	0.84	94.3	1.25	-69.3	0.064	15.1	0.87	145.8
7.00	0.82	84.0	1.31	-77.5	0.071	8.5	0.87	141.4
7.25	0.80	72.0	1.37	-86.7	0.079	1.0	0.87	136.5
7.50	0.78	58.1	1.44	-96.9	0.087	-7.6	0.86	130.9
7.75	0.76	42.2	1.51	-108.3	0.096	-17.3	0.86	124.3
8.00	0.75	24.5	1.57	-120.9	0.105	-28.3	0.85	116.5
8.25	0.75	5.4	1.62	-134.8	0.113	-40.5	0.85	107.1
8.50	0.77	-14.1	1.64	-149.8	0.119	-53.9	0.84	95.4
8.75	0.79	-33.1	1.64	-165.8	0.123	-68.5	0.84	80.9
9.00	0.83	-50.8	1.59	177.3	0.125	-84.1	0.82	63.1
9.25	0.86	-66.9	1.50	159.6	0.122	-100.7	0.81	41.7
9.50	0.90	-81.2	1.37	141.5	0.115	-117.9	0.80	17.3
9.75	0.93	-93.8	1.20	123.6	0.105	-135.3	0.80	-8.7
10.00	0.95	-104.7	1.01	106.6	0.092	-152.1	0.82	-34.0

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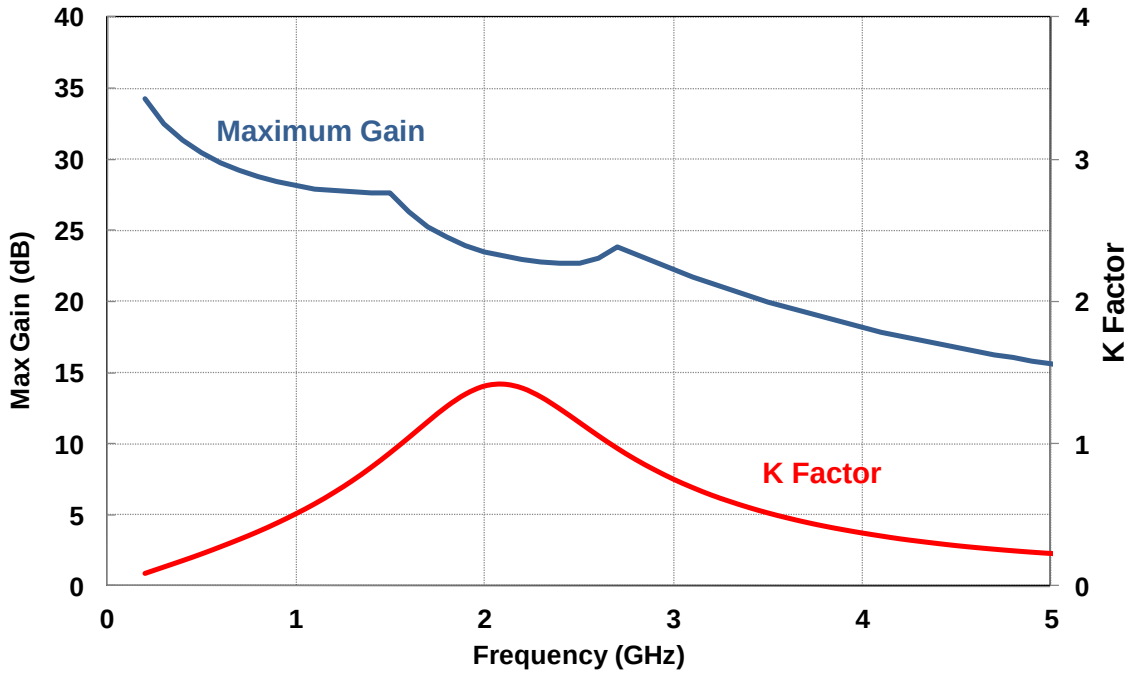
Maximum Gain & Stability Characteristics

Tcase= +25°C, CW mode, V_D=50V, I_{D_Q}=200mA



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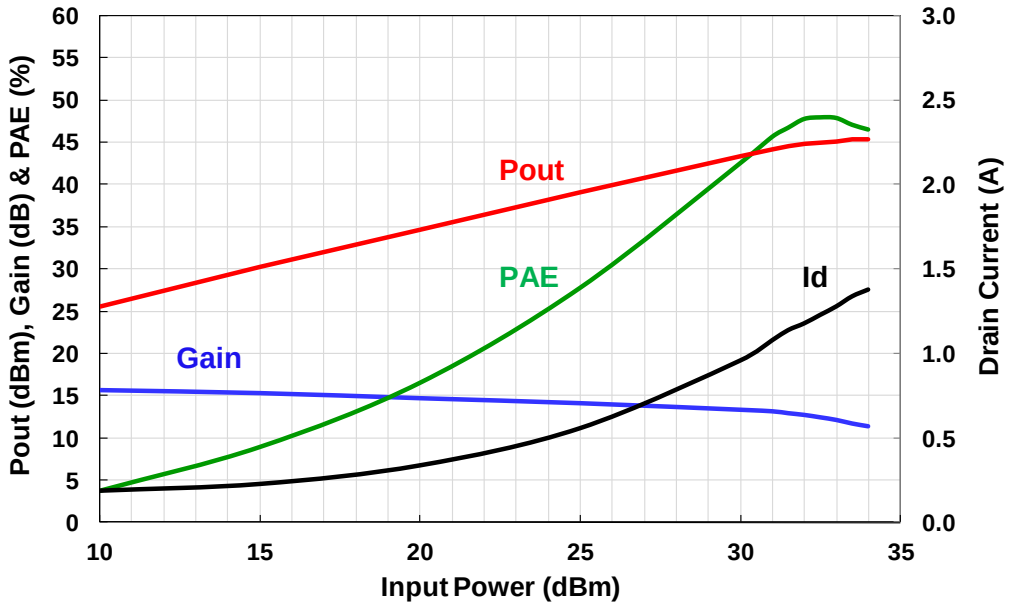
Typical Performance on Demonstration Board (Ref. 61500252)

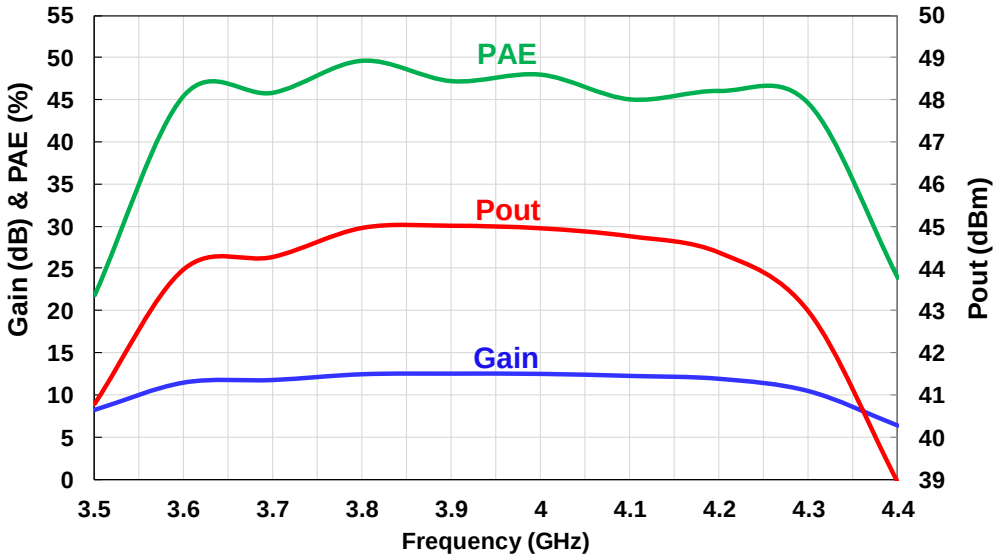
Calibration and measurements are done on the connector reference accesses of the demonstration boards.

Tcase = +25°C, CW mode

Measured Pout, Gain, PAE & Id
F = 4GHz, V_{DS} = 50V, I_{D_Q} = 200mA



Measured Pout, PAE & Gain
Pin = 32.5 dBm, V_{DS} = 50V, I_{D_Q} = 200mA



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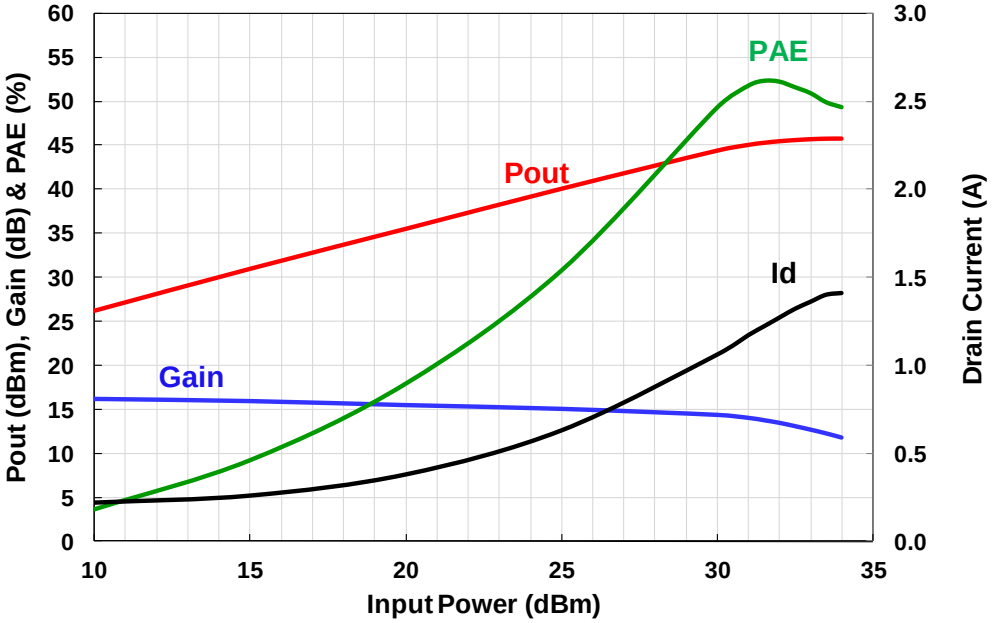
Typical Performance on Demonstration Board (Ref. 61500252)

Calibration and measurements are done on the connector reference accesses of the demonstration boards.

Tcase = +25°C, Pulsed mode (1)

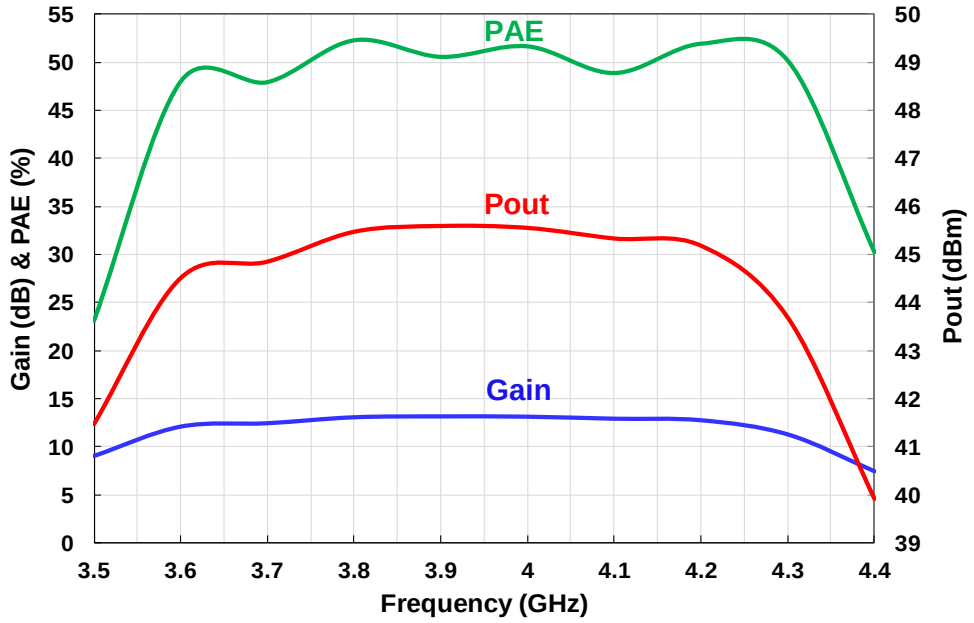
Measured Pout, Gain, PAE & Id

F = 4GHz, V_{DS} = 50V, I_{D_Q} = 200mA



Measured Pout , PAE & Gain

Pin = 32.5 dBm, V_{DS} = 50V, $I_{D\ Q}$ = 200mA



(1) Input RF and gate voltage are pulsed. Conditions are 25µs width, 10% duty cycle and 1µs offset between RF and DC pulse.

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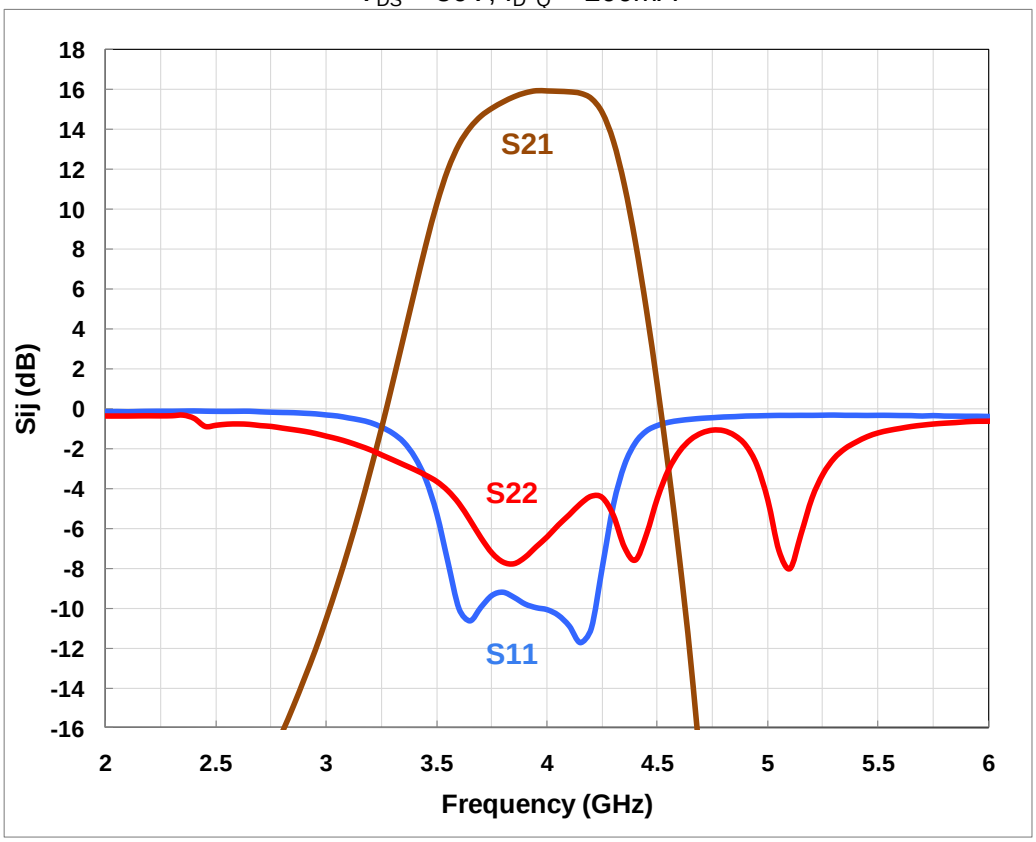
Typical Performance on Demonstration Board (Ref. 61500252)

Calibration and measurements are done on the connector reference accesses of the demonstration boards

Tcase = +25°C, CW mode

Measured S parameters

V_{DS} = 50V, $I_{D\ Q}$ = 200mA



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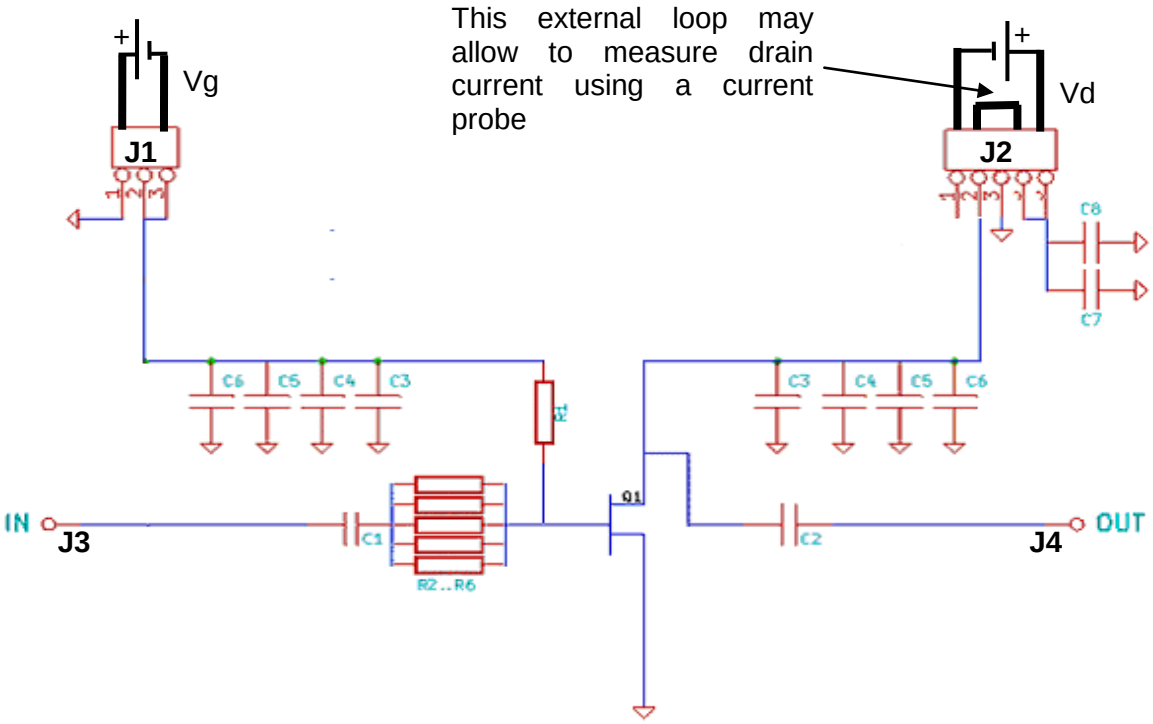
Demonstration Amplifier Low Frequency Equivalent Schematic (Ref. 61500252)



Demonstration Amplifier (Ref. 61500252) / Bill of Materials

Designator	Type	Value - Description	Qty
C1	Capacitor	0.4pF, +/- 0.05pF, 0603	1
C2	Capacitor	0.6pF, +/- 0.05pF, 0603	1
C3	Capacitor	8.2pF, +/- 0.25%, 0603	2
C4	Capacitor	82pF, +/- 5%, 0603	2
C5	Capacitor	1nF, +/- 5%, 0805	2
C6	Capacitor	10nF, +/- 5%, 0805	2
C7	Capacitor	1µF, +/- 10%, 1204	1
C8	Capacitor	68µF, +/- 10%, 1204	1
R1	Resistor	147Ω, +/- 1%, 0603	1
R2..R6	Resistor	5,6Ω +/- 1%, 0603	5
J1	Connector	CMS 3cts	1
J2	Connector	CMS 5cts	1
J3,J4	Connector	SMA	2
Q1	Packaged Transistor	CHK025A-SOA	1
-	PCB	RO4003, Er=3.55, h= 508µm	-

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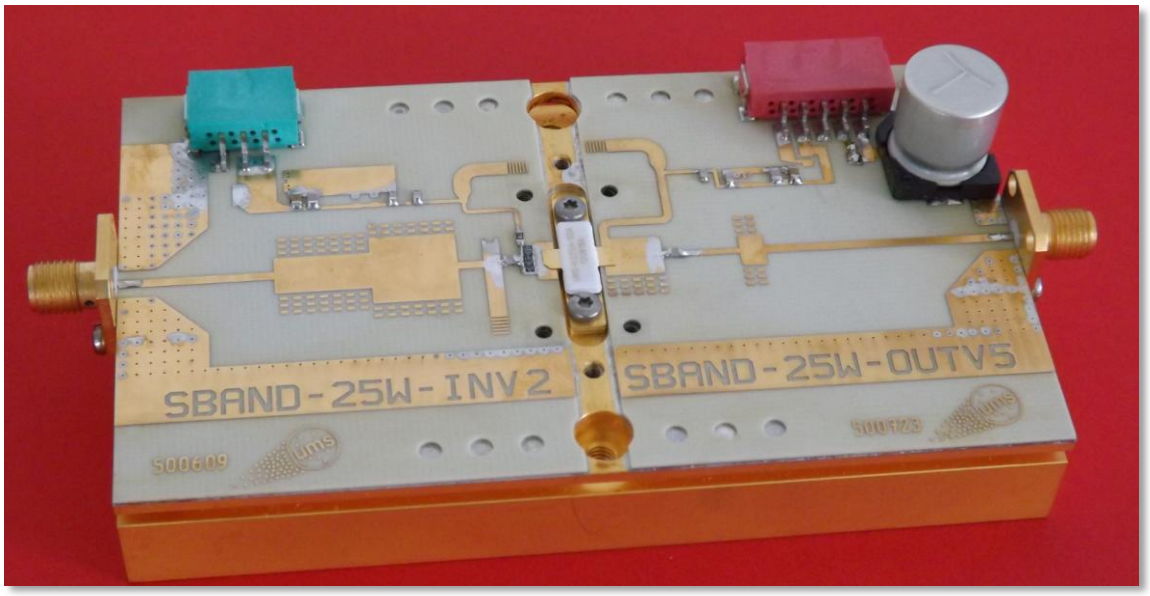
Demonstration Amplifier Circuit (Ref. 61500252)



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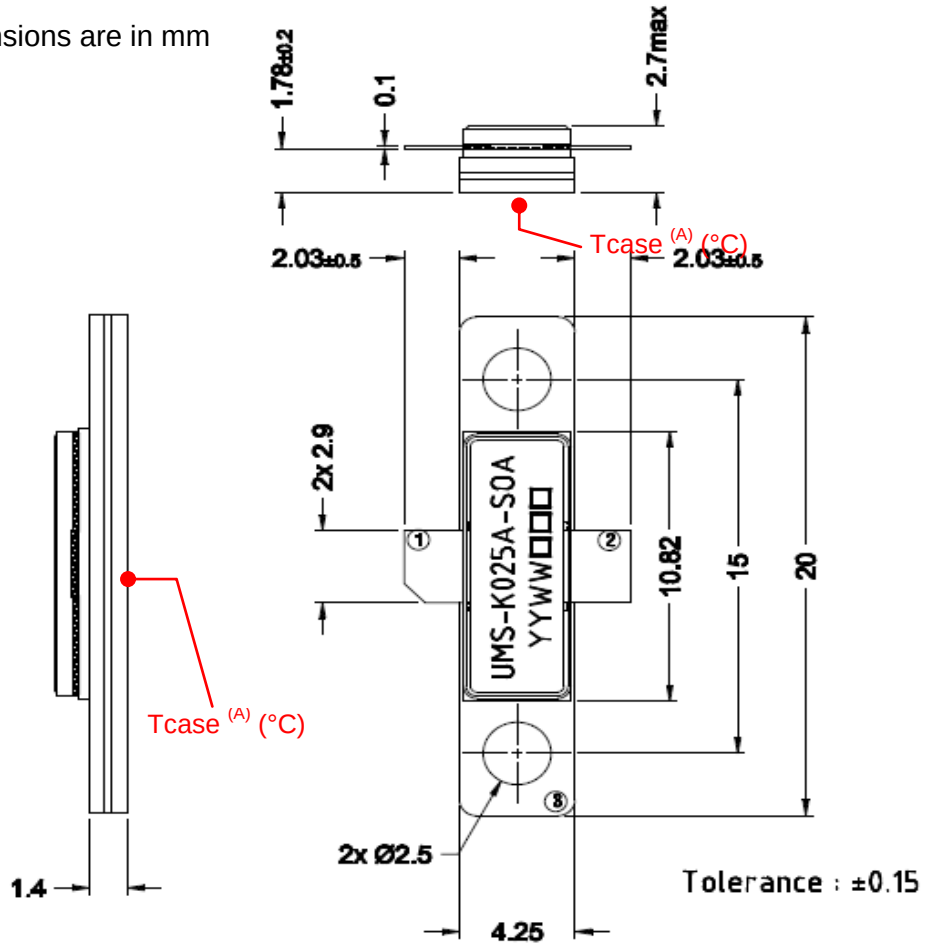
Package outline

All dimensions are in mm



PIN-OUT : 1- GATE
2- DRAIN
3- SOURCE (Gnd)

(A) Tcase locates the reference point used to monitor the device temperature. This point has been taken at the device / system interface to ease system thermal design.
Chamfered lead indicates the gate access of the packaged transistor.

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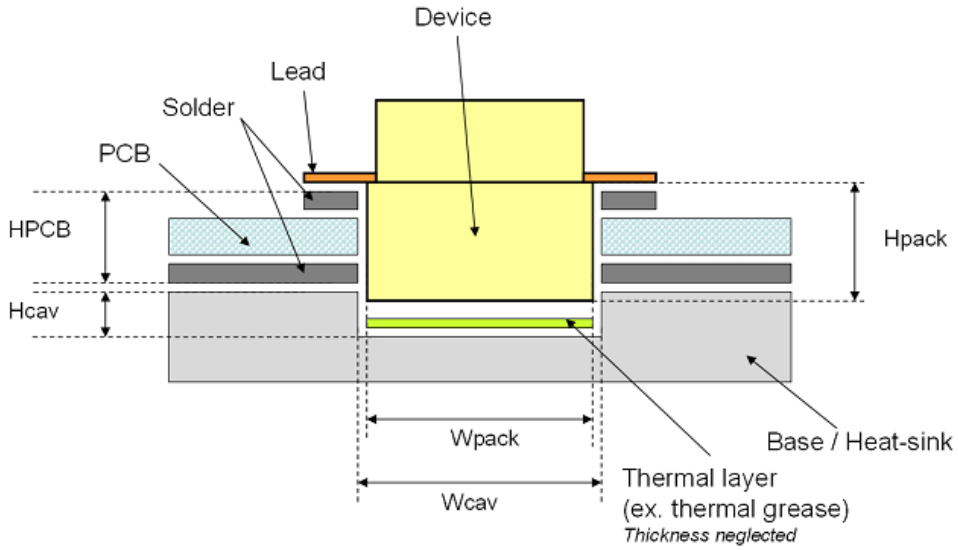
Recommended Assembly Procedure

CHK025A-SOA is available has a flange package to be bolt down onto a thermal heat sink also used as main electrical ground. Use preferably screw M2 and flat washers.
Thermal and electrical resistance at the package to heat sink interface has to be as low as possible. Thermal electrically conductive grease or conductive thin layer like indium sheets are recommended between the package and the heat sink.
In case a thermal grease is selected, we recommend to use material offering thermal conductivity >5W/m.K and electrical resistivity <0.01 ohm.cm. The grease layer thickness should be about 25µm (1 mil).
Contact interface quality can be improved by cleaning process prior device mounting on the heat-sink. Such operation will enhance the thermal and electrical contact by oxides removal at each interface.
Package leads can be soldered on printed circuit board's traces by using RoHS solder past.
Cavity depth and width to be performed into the heat-sink where the device will be mounted are important to achieve the best performances. These dimensions have to be optimized in order to minimize the distance between device and signal traces made on the printed circuit board (PCB). But they also have to be calculated in order to accommodate device variations in height. The following drawing gives the relationship between device dimensions (Hpack & Wpack) and optimal cavity depth (Hcav) and width (Wcav) depending on the printed circuit-board configuration (HPCB)



$Hcav = (Hpack_{min} - HPCB_{max})^{+0}{}_{/- 0.05}$

$Wcav = (Wpack_{max} + 0.4)_{+/- 0.05}$

dimensions are in mm

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Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Qualification domain

The CHK025A-SOA is qualified according to UMS rules, excluding humid environment as it is in non hermetic package.

Ordering Information

Package:	CHK025A-SOA/XY Tray: XY = 26

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