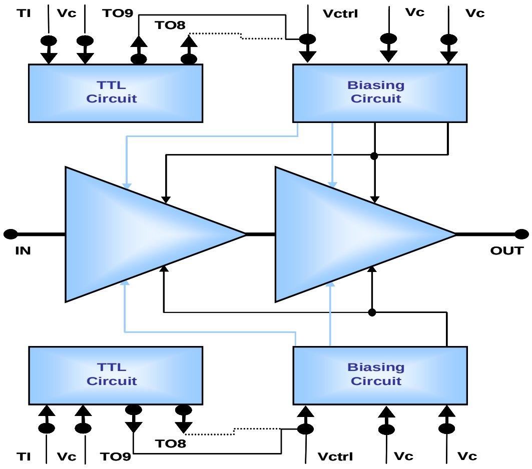
# X-band HBT High Power Amplifier

## GaAs Monolithic Microwave IC

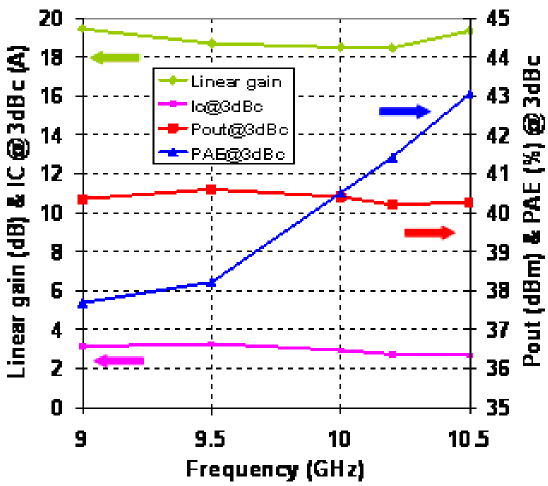
## Description




The CHA8100 chip is a monolithic two-stage high power amplifier designed for X band applications. The HPA provides typically 11W output power, 40% power added efficiency and a high robustness on mismatched output. Moreover it includes:

- an analogue biasing circuit that makes it less sensitive to spread and chip environment.
- an integrated TTL interface that enables to switch the HPA with a current consumption lower than 1mA

The circuit is 100% DC and RF tested on wafer to ensure performance compliance. This device is manufactured using a GaInP HBT process, including, via holes through the substrate and air bridges.




## Main Features

- 11W output power in pulse mode
- High gain: > 18dB @ 10GHz
- High PAE: 40% @ 10GHz
- Two biasing modes:
  - Digital control thanks to TTL interface
  - Analog control thanks to biasing circuit
- Chip size: 4.9 x 3.68 x 0.1mm$^3$

## Main Characteristics

Vc=9V, Ic (Quiescent) = 2.1A, Pulse width=100µs, Duty cycle = 20%

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Top | Operating temperature range (1) | -40 | | +80 | °C |
| F_op | Operating frequency range | 9 | | 10.5 | GHz |
| P_sat | Saturated output power @ 25°C | | 12.5 | | W |
| P_3dBc | Output power @ 3dBc @ 25°C | | 11 | | W |
| G_lin | Linear gain @ 25°C | 17 | 18.5 | | dB |

ESD Protections: Electrostatic discharge sensitive device. Observe handling precautions!
(1) The reference is the back-side of the chip.



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## Electrical Characteristics

Tamb = 25℃, Vc=9V, Ic (Quiescent) = 2.1A, Pulse wi dth=100µs, Duty cycle = 20%

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| F_op | Operating frequency | 9 | | 10.5 | GHz |
| G_lin | Linear gain (9 to 10GHz) | 17 | 18.5 | | dB |
| G_lin_T | Linear gain variation versus temperature | | -0.025 | | dB/℃ |
| RL_in | Input Return Loss | | -9 | | dB |
| RL_out | Output Return Loss | | -15 | | dB |
| P_sat | Saturated output power | | 41 | | dBm |
| P_sat_T | Saturated output power variation versus temperature | | -0.01 | | dB/℃ |
| P_3dBc | Output power @ 3dBc (3) | 39.5 | 40.5 | | dBm |
| PAE_3dBc | Power Added Efficiency @ 3dBc | 35 | 40 | | % |
| Vc | Power supply voltage (3) | 8 | | 9 | V |
| Ic | Power supply quiescent current (1) | | 2.1 | | A |
| TI | TTL input voltage | 0 | | 5 | V |
| I_TI | TTL input current | | 0.7 | | mA |
| Vctrl | Collector current control voltage | | 5 | | V |
| Ictrl | Control supply current | | 22 | | mA |
| Zctr | Vctrl input port impedance (2) | | 350 | | Ohm |
| Top | Operating temperature range | -40 | | +85 | ℃ |

(1) Parameter tunable by Vctrl when control biasing circuit used.
(2) This value corresponds to the 4 ports in parallel
(3) 0.5V variation on Vc leads to around 0.4dB variation of the output power (impact on robustness see Maximum ratings)

## Absolute Maximum Ratings (1)

Tamb = 25℃

| Symbol | Parameter | Values | Unit |
|---|---|---|---|
| Cmp | Compression level (2 & 3) | 8 | dB |
| Vc | Power supply voltage (4) | 10 | V |
| Ic | Power supply quiescent current | 3 | A |
| Ic_sat | Power supply current in saturation | 4 | A |
| Vctrl | Collector current control voltage | 6.5 | V |
| Tj | Maximum junction temperature (5) | 175 | ℃ |
| Tstg | Storage temperature range | -55 to +125 | ℃ |

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) For higher compression the level limit can be raised by decreasing the voltage Vc using the rate 0.5 V / dBc
(3) VC=9V, Temperature=-40℃, Output VSWR=2:1
(4) Without RF input power
(5) Equivalent Thermal resistance to Backside: 6℃/W



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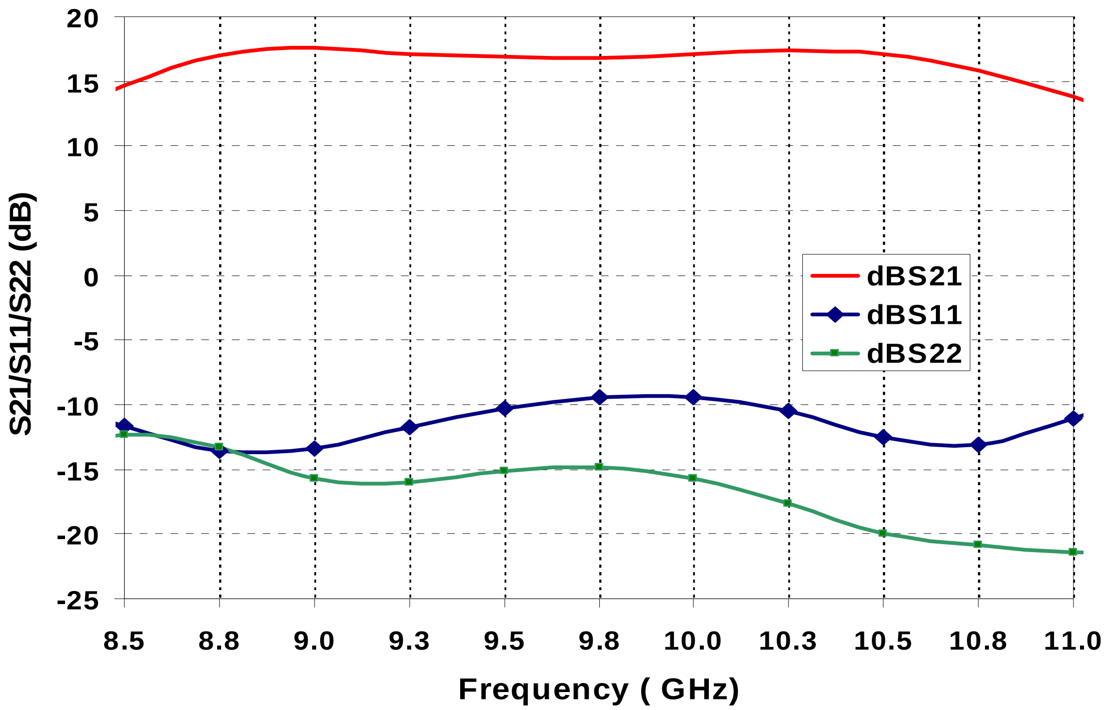
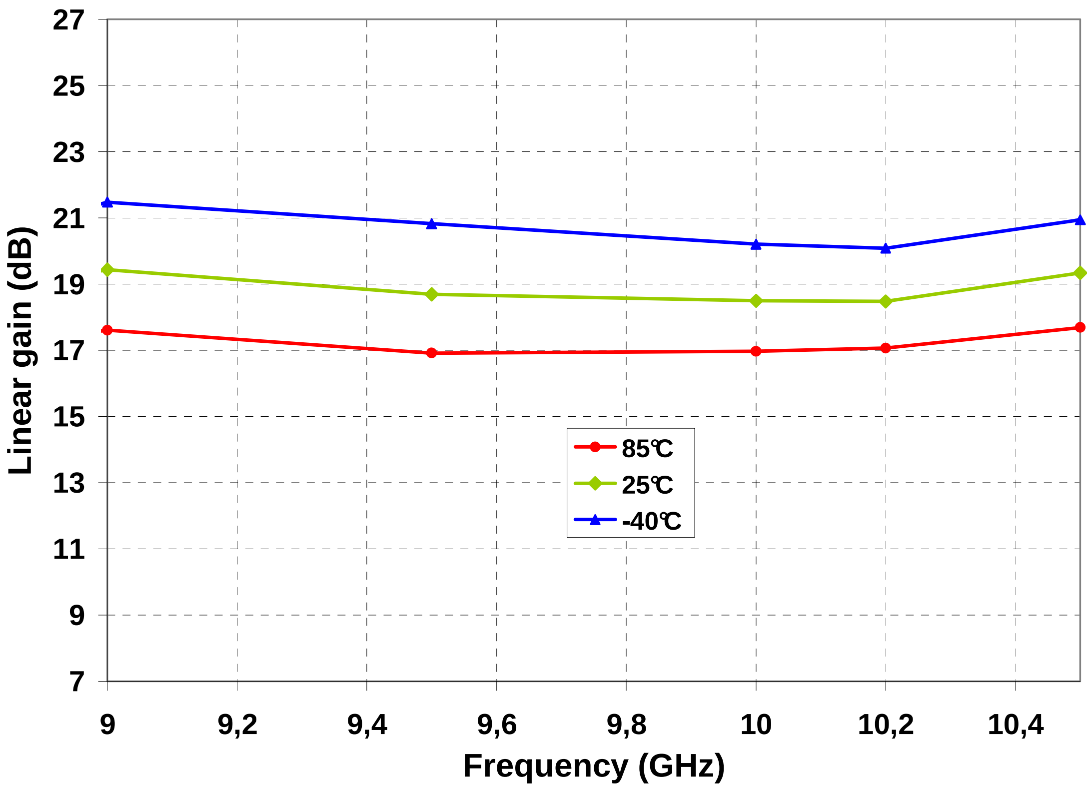
## Typical measured characteristics

**Measurements on Jig**:
Vc = 9V, VTTL=5V, Ic (Quiescent) = 2.1A, Pulse width=100µs, Duty cycle = 20%




*Gain/Input & Output Return losses (dB). Temperature:+20°C*




*Linear Gain versus frequency and temperature*



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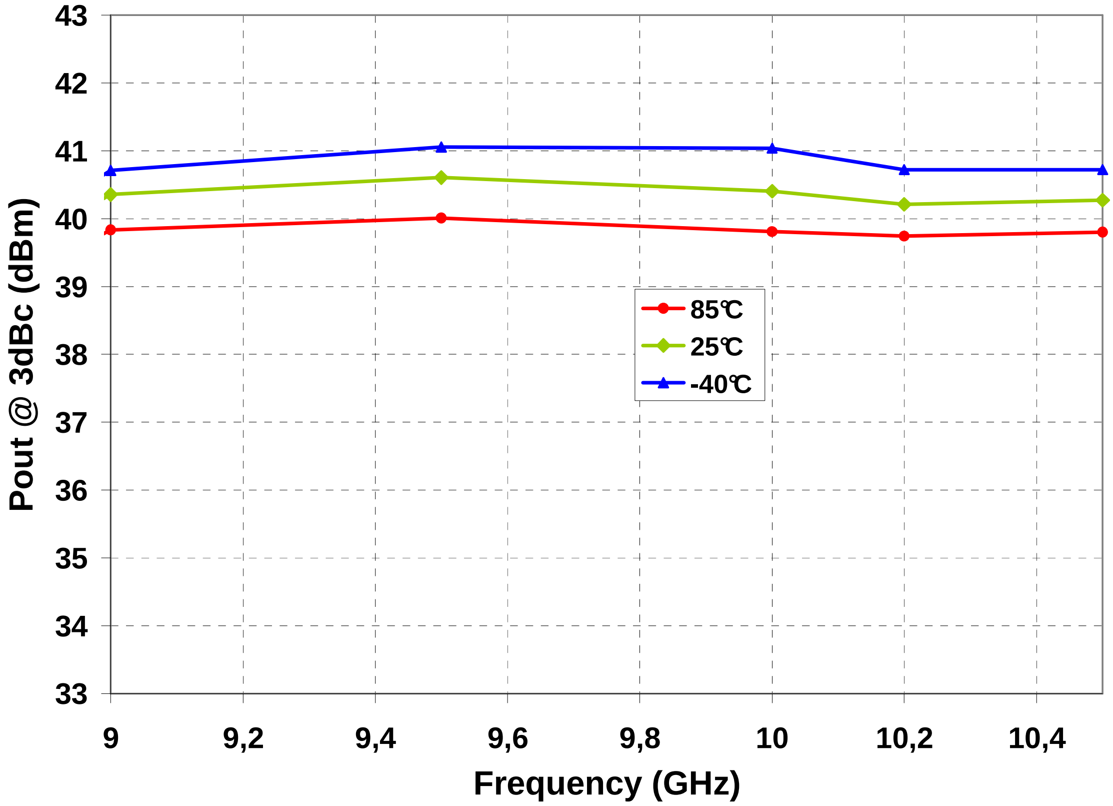
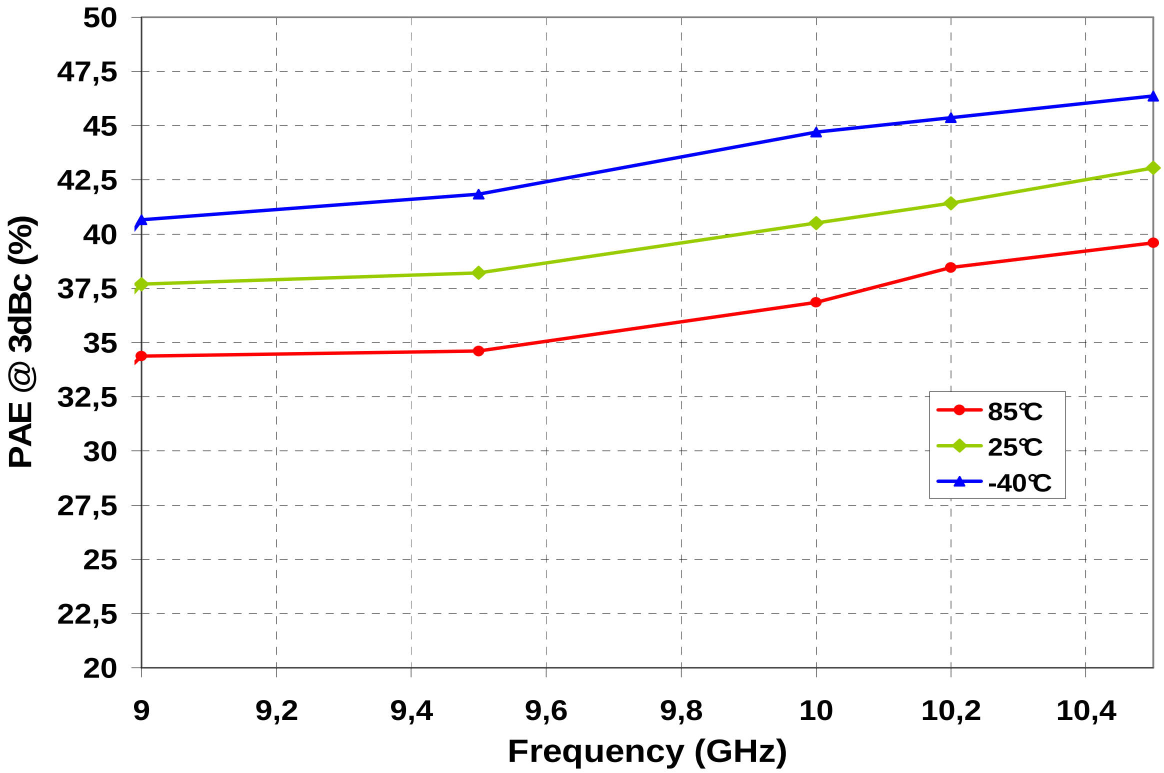



***Output Power @ 3dBc versus frequency and temperature***




***PAE @ 3dBc versus frequency and temperature***



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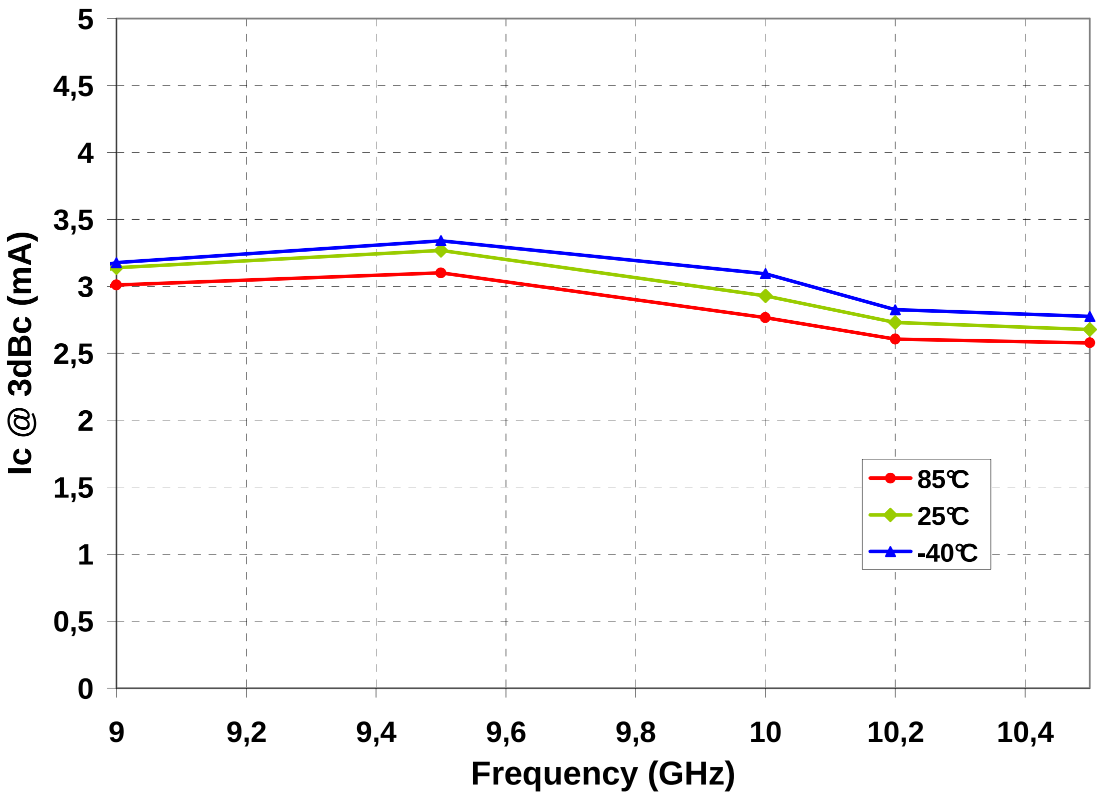


***Ic @ 3dBc versus frequency and temperature***



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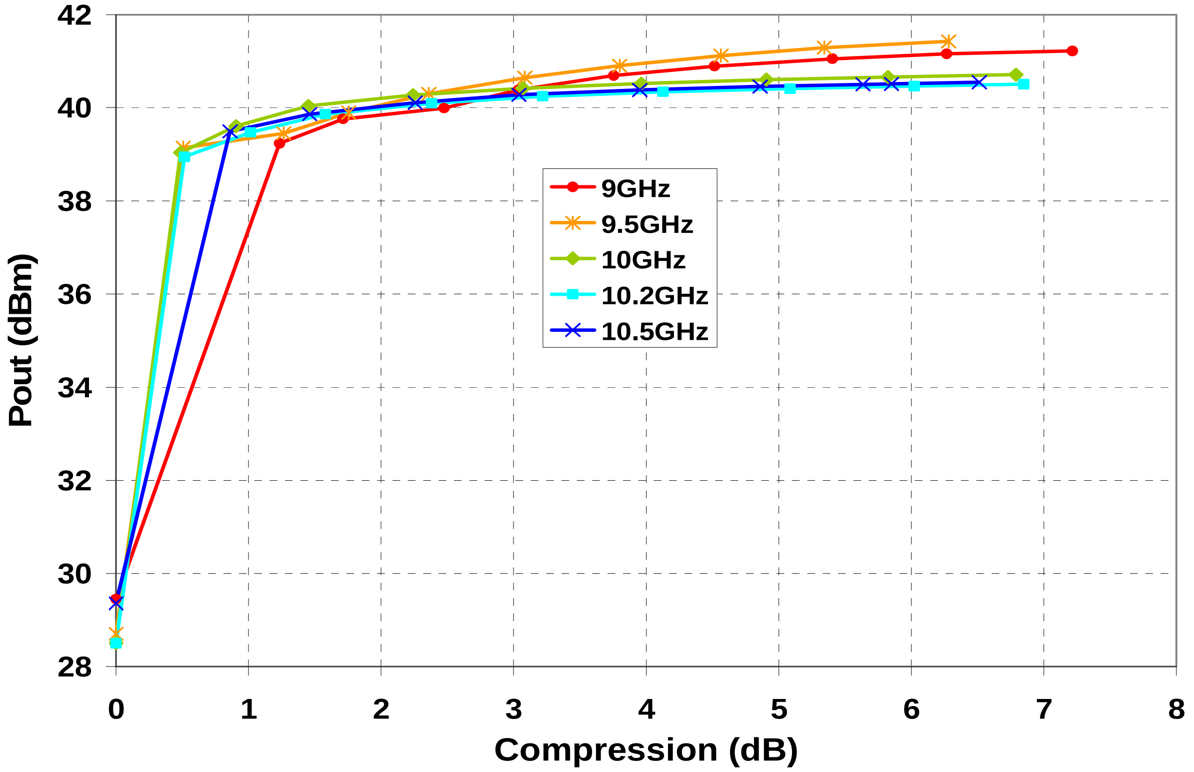
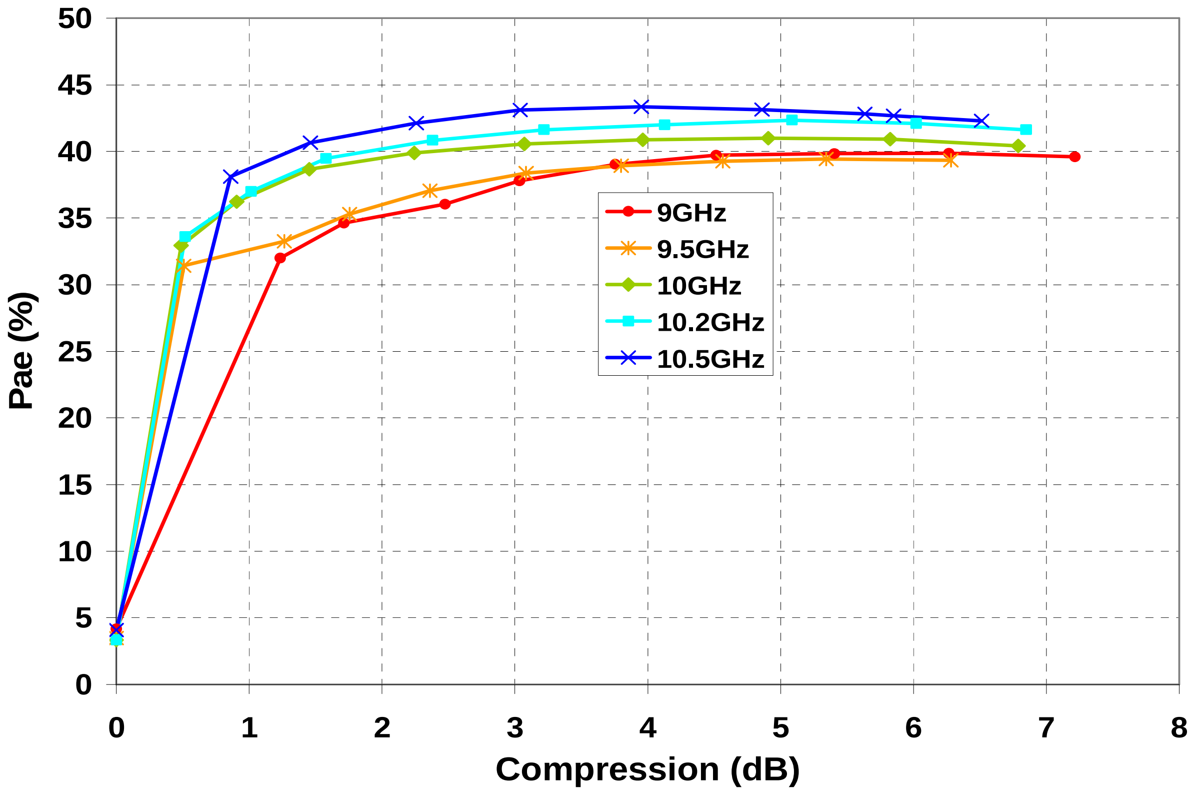



*Output Power @ 25°C versus compression and frequency*




*PAE @ 25°C versus compression and frequency*

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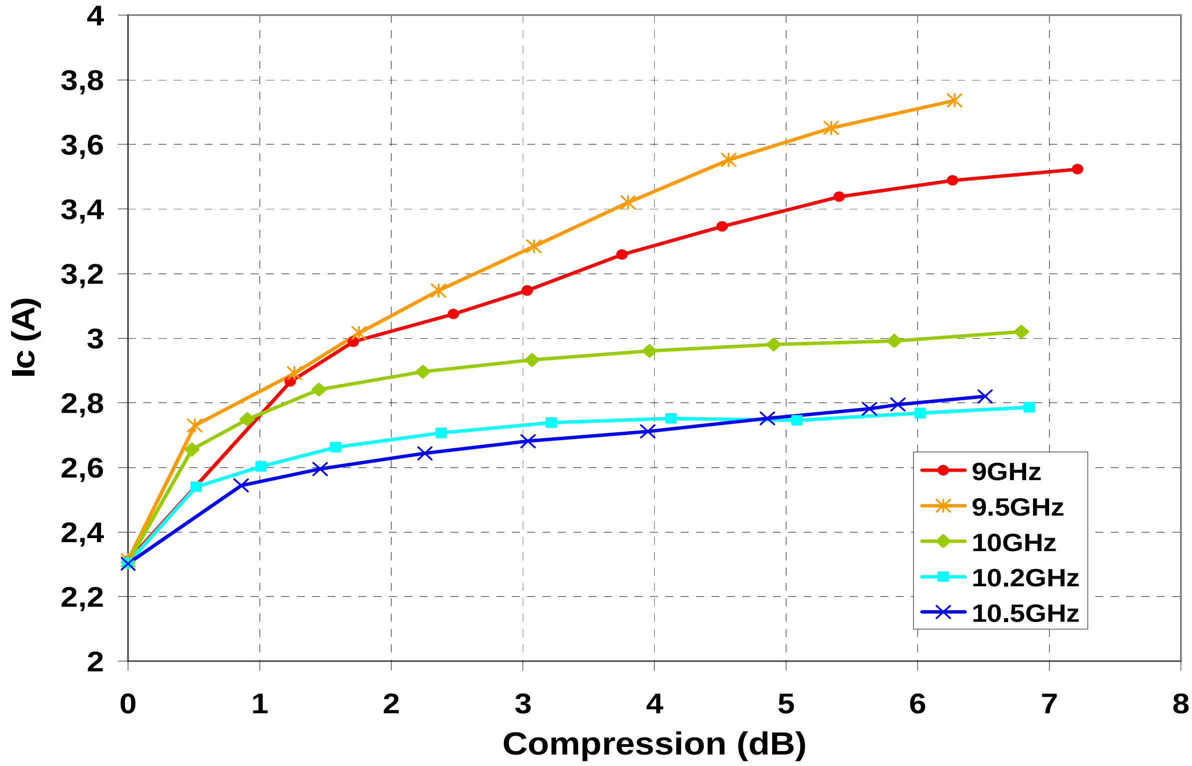
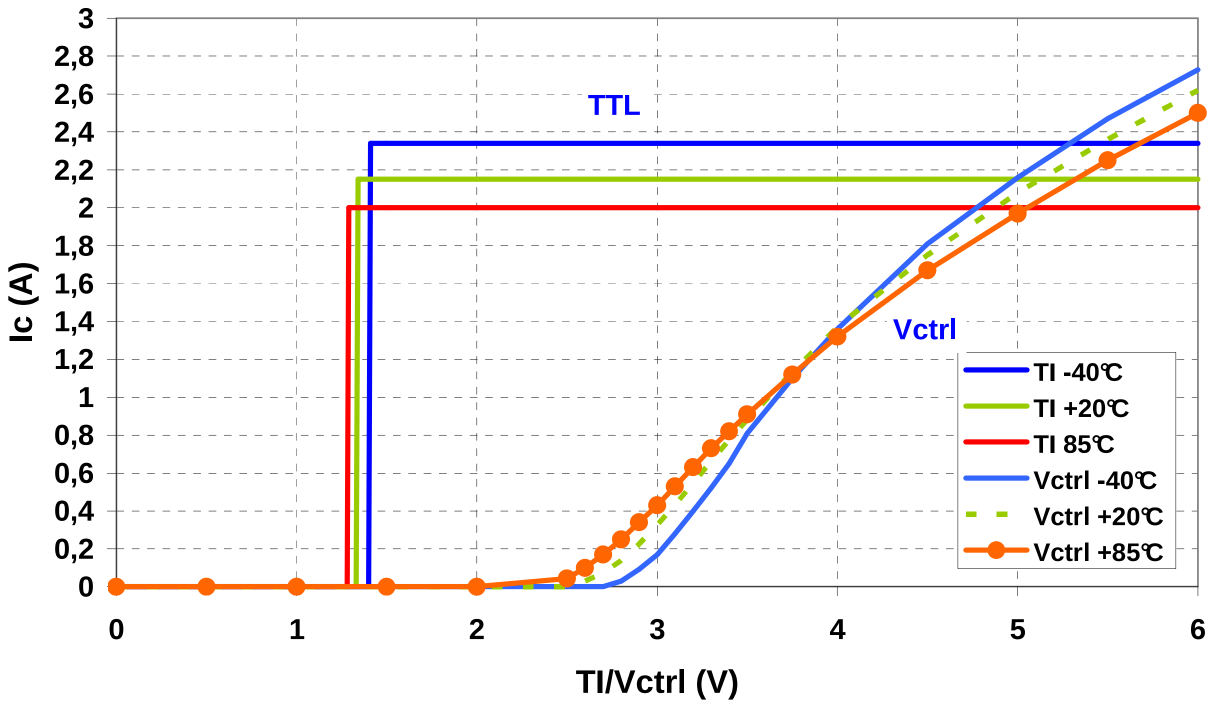



*Collector current @ 25°C versus compression and frequency*




*Collector quiescent current versus TI & Vctrl and temperature*



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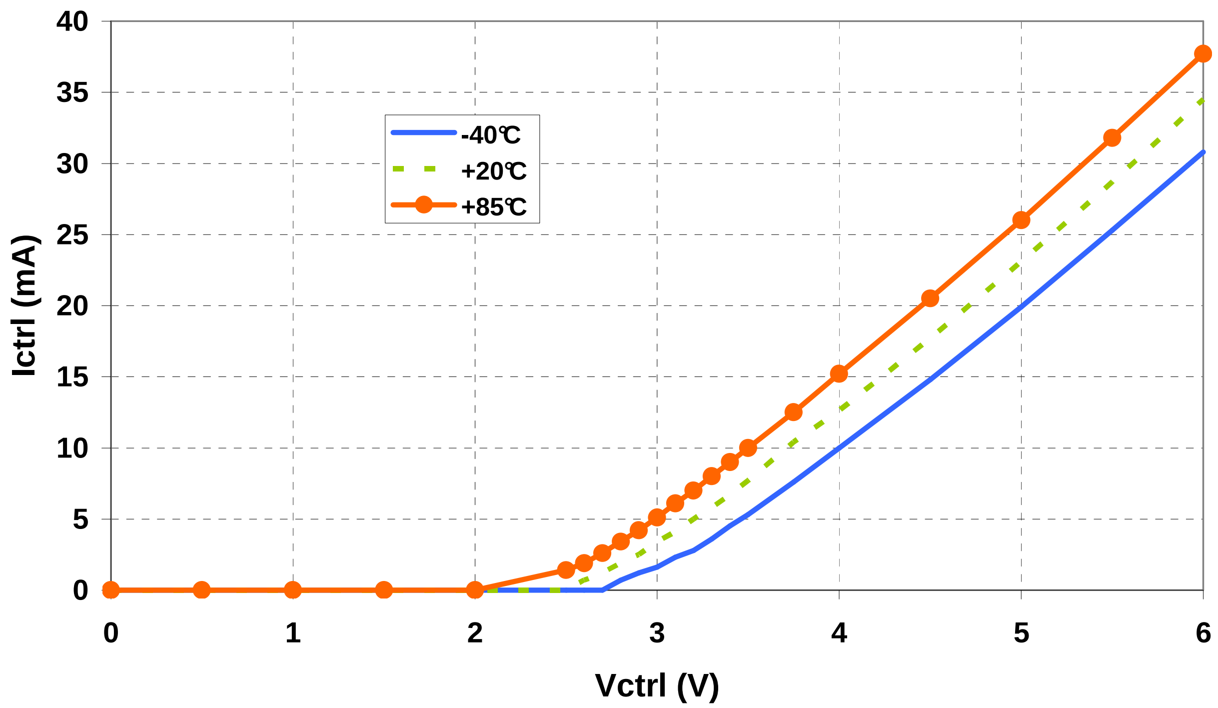
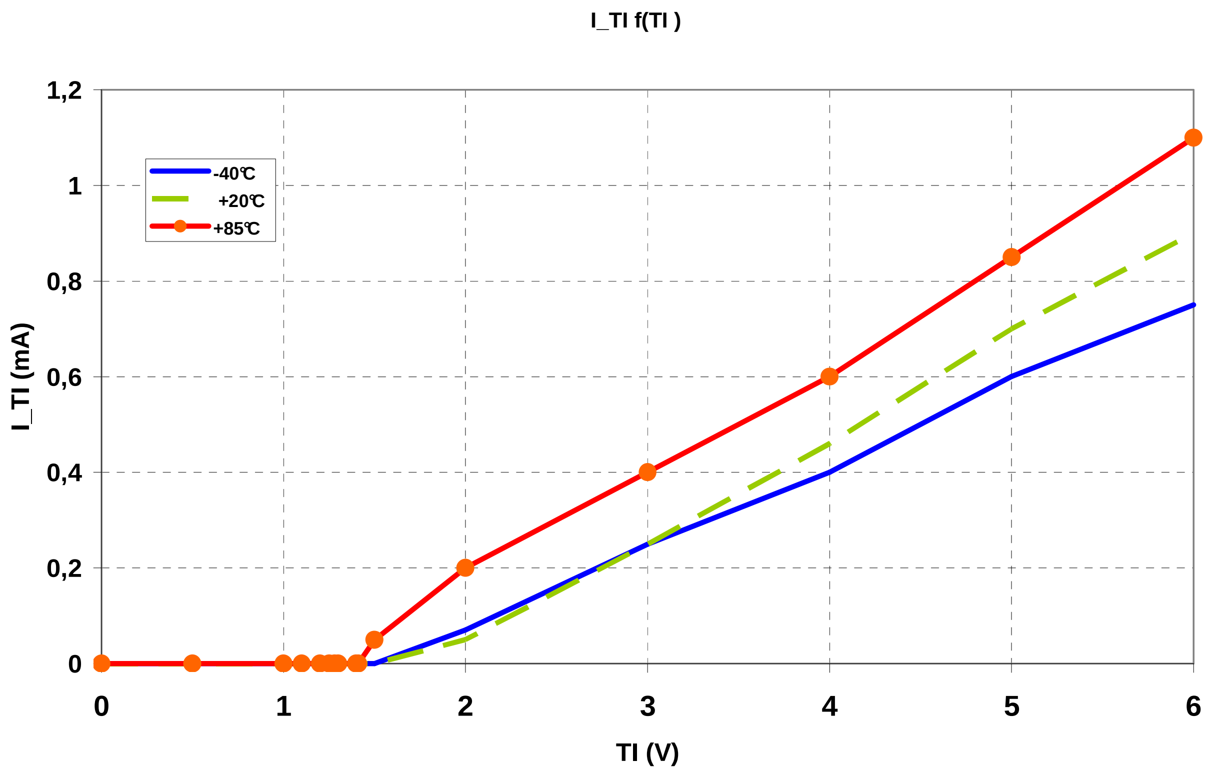



*Control current versus control voltag e & temperature*




*TTL input current versus TTL voltage and temperature*



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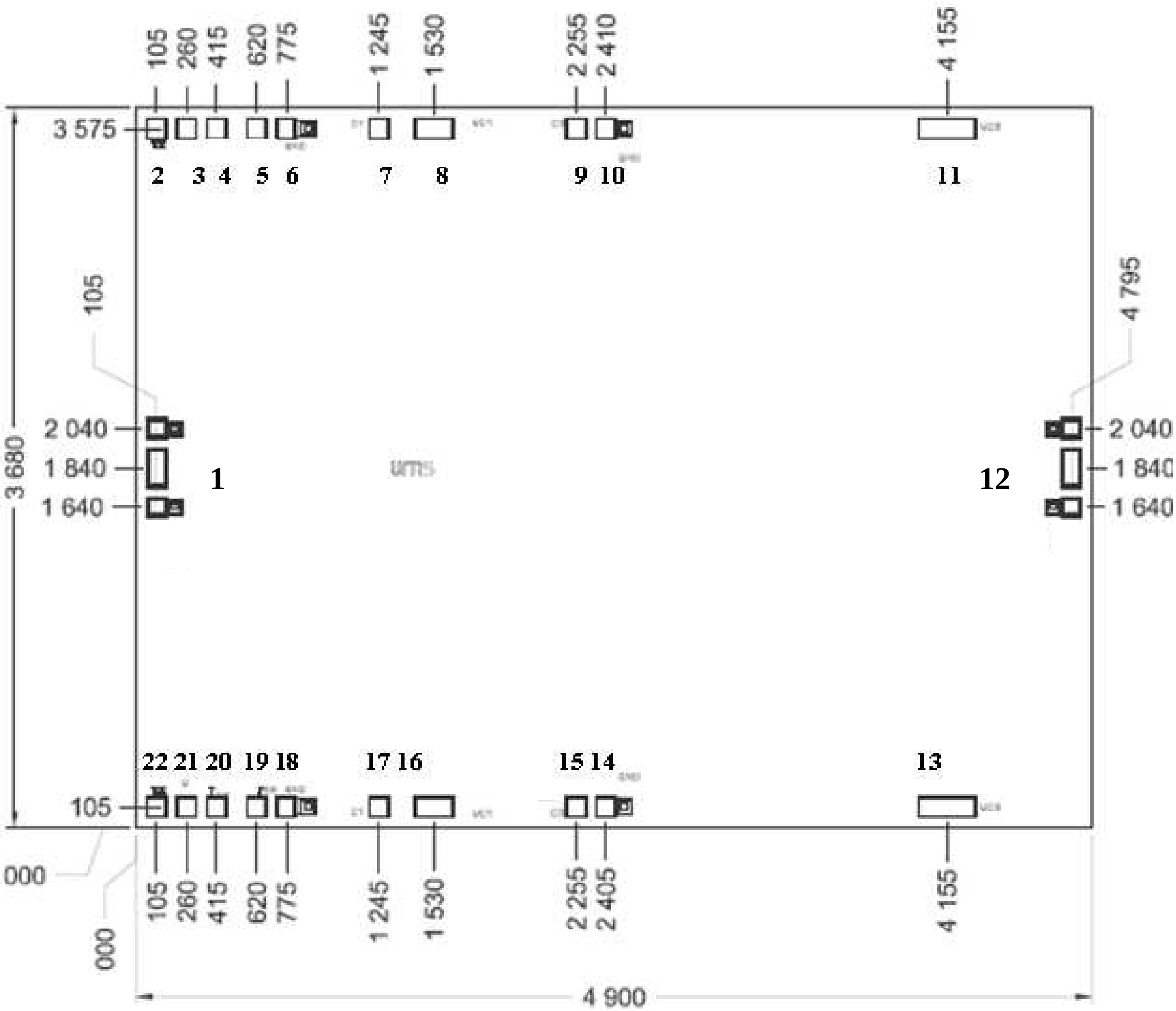
## Chip Mechanical Data and Pin references




Units: µm
Chip width and length are given with a tolerance of ±35µm
Chip thickness = 100µm +/- 10 µm
RF pads (1, 12) = 96 x 196µm²
DC pads (2, 3, 4, 5, 6, 7, 9,10, 14, 15, 17, 18, 19, 20, 21, 22) = 96 x 96µm²
DC pads (8, 16) = 192 x 96µm²
DC pads (11, 13) = 288 x 96µm²

| Pin number | Pin name | Description |
|---|---|---|
| 1 | IN | Input RF |
| 7, 9, 15, 17 | C1, C2 | Collector current control voltage |
| 2, 22 | TI | TTL input |
| 4, 20 | TO9 | TTL output when Vcx=9V |
| 5, 19 | TO8 | TTL output Vcx=8V |
| 6, 10, 14, 18 | GND | Ground (NC) |
| 3, 8, 11, 13, 16, 21 | V,Vc1,Vc2 | Power supply voltage |
| 12 | OUT | Output RF |



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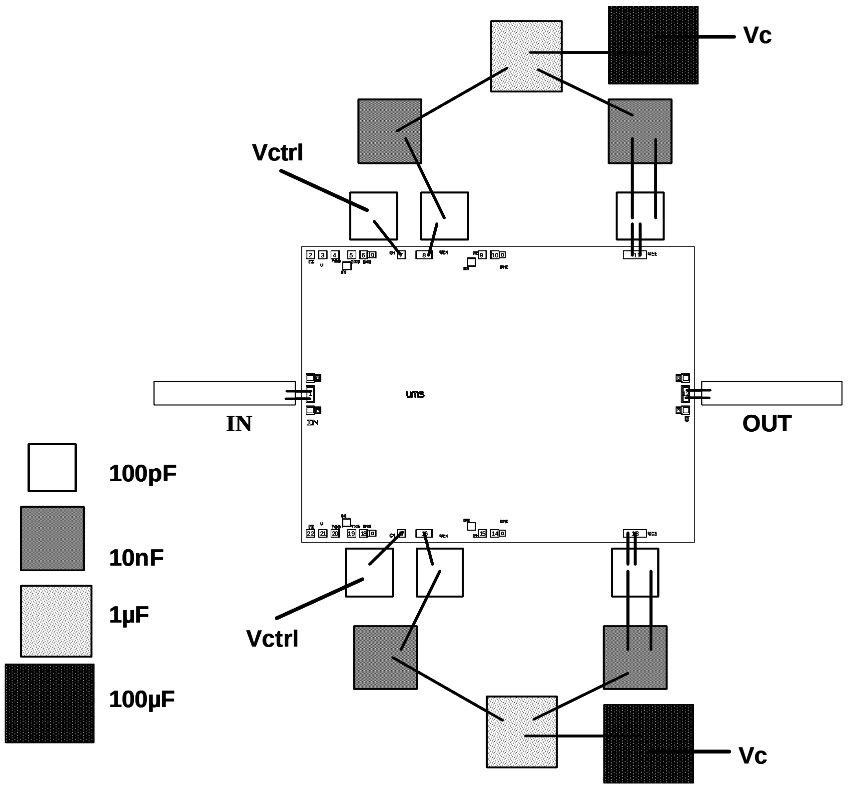
## Bonding recommendations

For thermal and electrical considerations, the chip should be brazed on a metal base plate. The RF, DC and modulation port inter-connections should be done according to the following table:

| Port | Connection |
|---|---|
| IN (1) | Inductance (Lbonding) = 0.3nH<br>400µm length with wire diameter of 25 µm x2 |
| OUT (12) | Inductance (Lbonding) = 0.3nH<br>400µm length with wire diameter of 25 µm x2 |
| DC pads to 1st decoupling level for double bonding | Inductance (Lbonding) =0.7nH<br>Two 1.2mm length wires with a diameter of 25 µm |
| DC pads to 1st decoupling level for single bonding | Inductance (Lbonding) =1nH<br>One 1.2mm length wires with a diameter of 25 µm |
| 1st decoupling level to 2nd decoupling level for double bonding | Inductance (Lbonding) =0.7nH<br>Two 1.2mm length wires with a diameter of 25 µm |
| 1st decoupling level to 2nd decoupling level for single bonding | Inductance (Lbonding) =1nH<br>One 1.2mm length wires with a diameter of 25 µm |

## Assembly recommendations in test fixture (using analogue biasing circuits)




Note: Supply feed should be capacitively by-passed. 25µm diameter gold wire is to be preferred.



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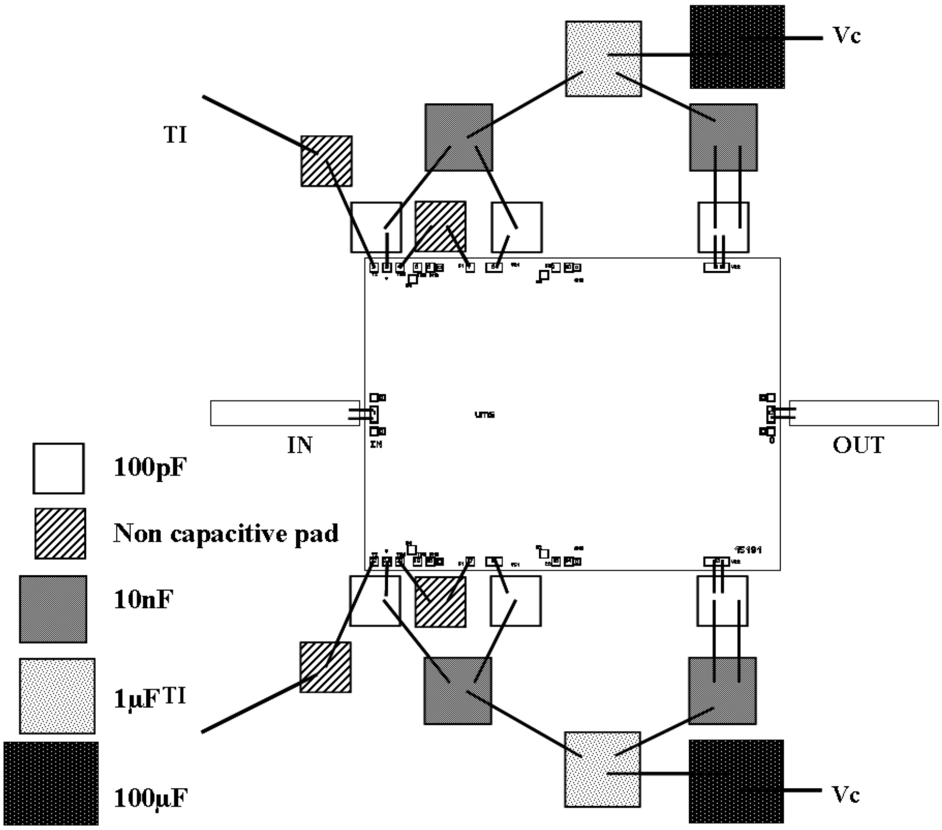
## Assembly recommendations in test fixture (using TTL circuits)




* Performances obtained with the same accesses connected to the same supply
Note: Supply feed should be capacitively by-passed. 25µm diameter gold wire is to be preferred.

## Biasing possibilities

| TTL / Vcontrol | $Vc_1$, $Vc_2$, V | Connections |
|---|---|---|
| Biasing via TTL interface | 9V | TO9 connected to C1 and C2<br>C2 & T08 not connected |
| Biasing via TTL interface | 8V | TO8 connected to C1 and C2<br>C2 & T09 not connected |
| Biasing via analogue control device | 9V or 8V | C2,V, Ti, TO8, TO9 not connected |



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## Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS products.

Ordering Information

Chip form : CHA8100-99F/00





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