Enabling Precise Timing Control in SDRs

Srikanth Pagadarai

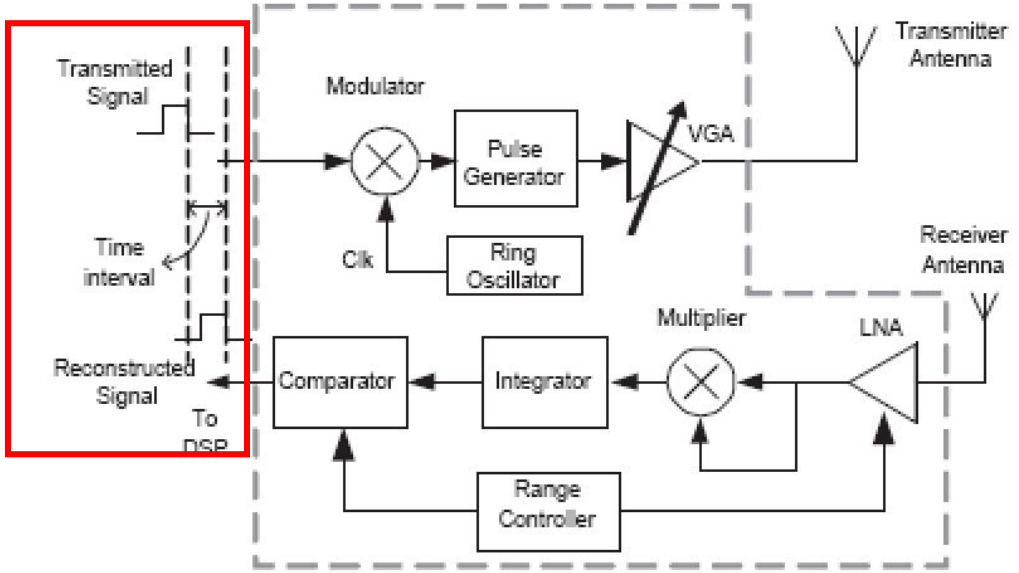
Systems Applications Engineer, Analog Devices

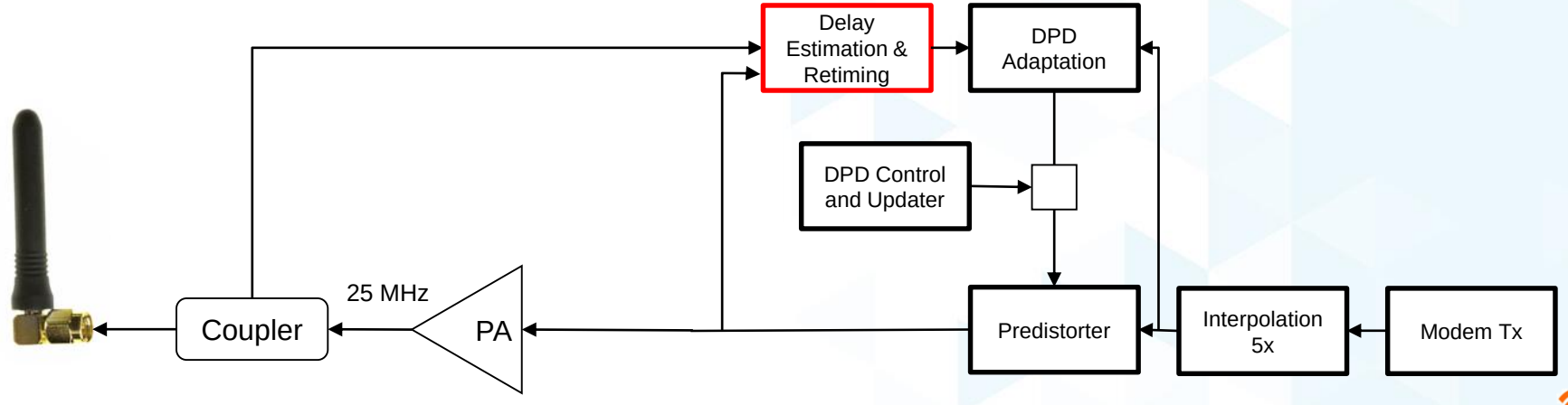
AHEAD OF WHAT'S POSSIBLE™

Outline

- Motivating Examples
- ADRV9361-Z7035
- Loopback Delay Estimation Algorithm
- Reference Design
- Performance Results

Motivating Examples





Digital Pre-Distortion

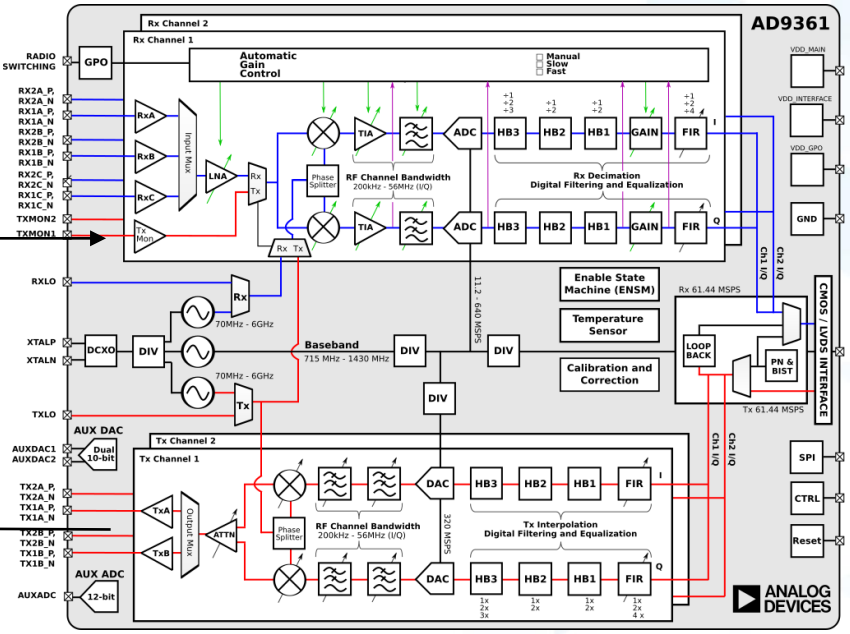
Occupied Bandwidth

Synthesized Bandwidth

Coupler

25 MHz

PA



38.4 MSPS
25 MHz

Delay Estimation & Retiming

DPD Adaptation

DPD Control and Updater

7.68 MSPS
4.5 MHz

38.4 MSPS
25 MHz

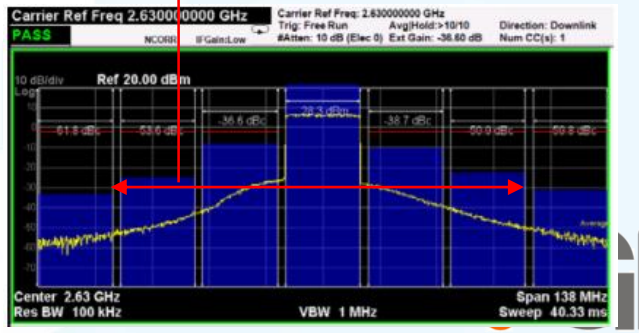
Predistorter

Interpolation 5x

LTE 5 Modem Tx

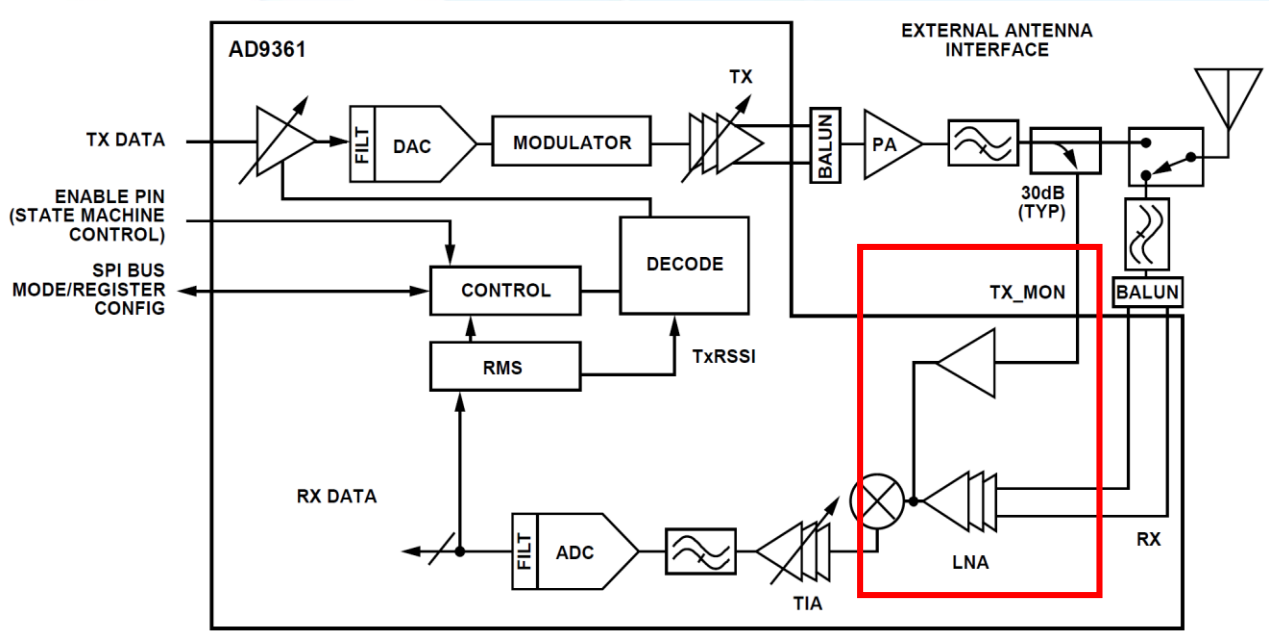
38.4 MSPS
25 MHz

Synthesized Bandwidth

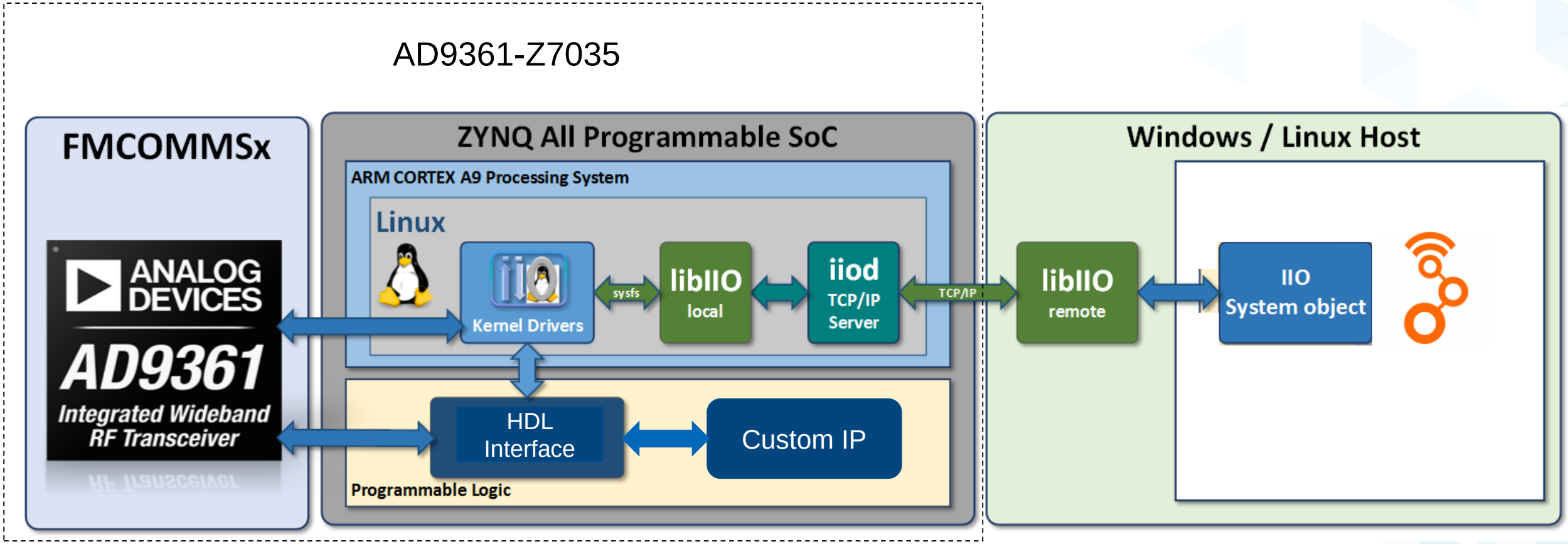


AD9361 Tx Power Monitor

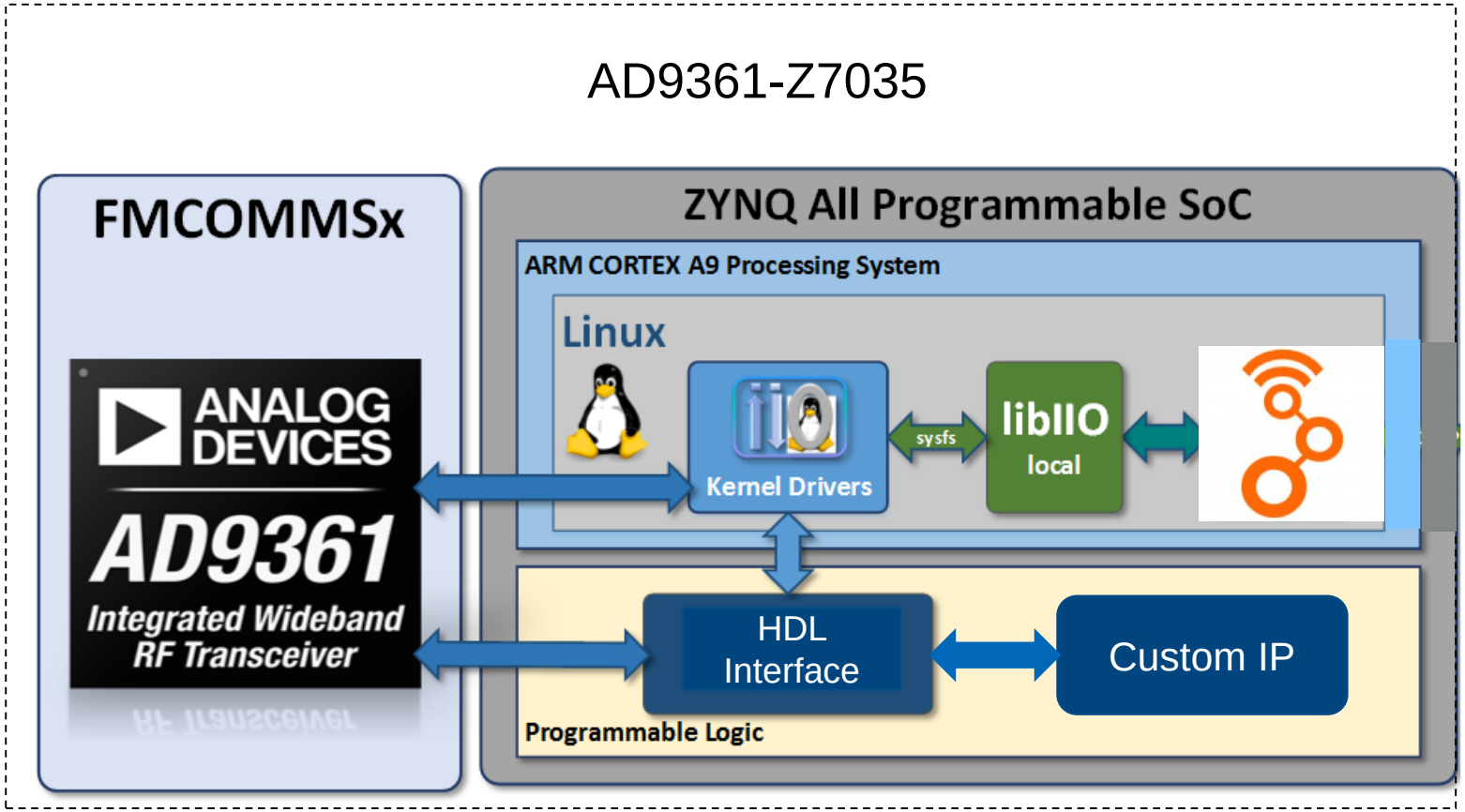
- Available in TDD mode only.
- Multiplexed in the Rx chain after LNA.
- Inputs require matching network, built into AD9361-Z7035 RF-SOM.
- Local oscillator signal used to downconvert TPM input is Tx LO.



ADRV9361-Z7035 Architecture: A Short Summary



ADRV9361-Z7035 Architecture: A Short Summary



- The most compelling use case for a ADRV9361-Z7035 is to use PS and PL in conjunction for signal processing.
- MW IPcore devices accessible through libiio.
- AXI MM registers utilized in the design are written to/read from using a GR application using libiio.

Design Flow

- Development, modeling and simulation of communications algorithms
- Testing and verification of algorithms with real-world data
  - Streaming from RF hardware
- Deployment of communications system to hardware for prototyping and production
  - Fixed-point implementation
  - Code generation and Targeting

Loopback Delay Estimation Algorithm

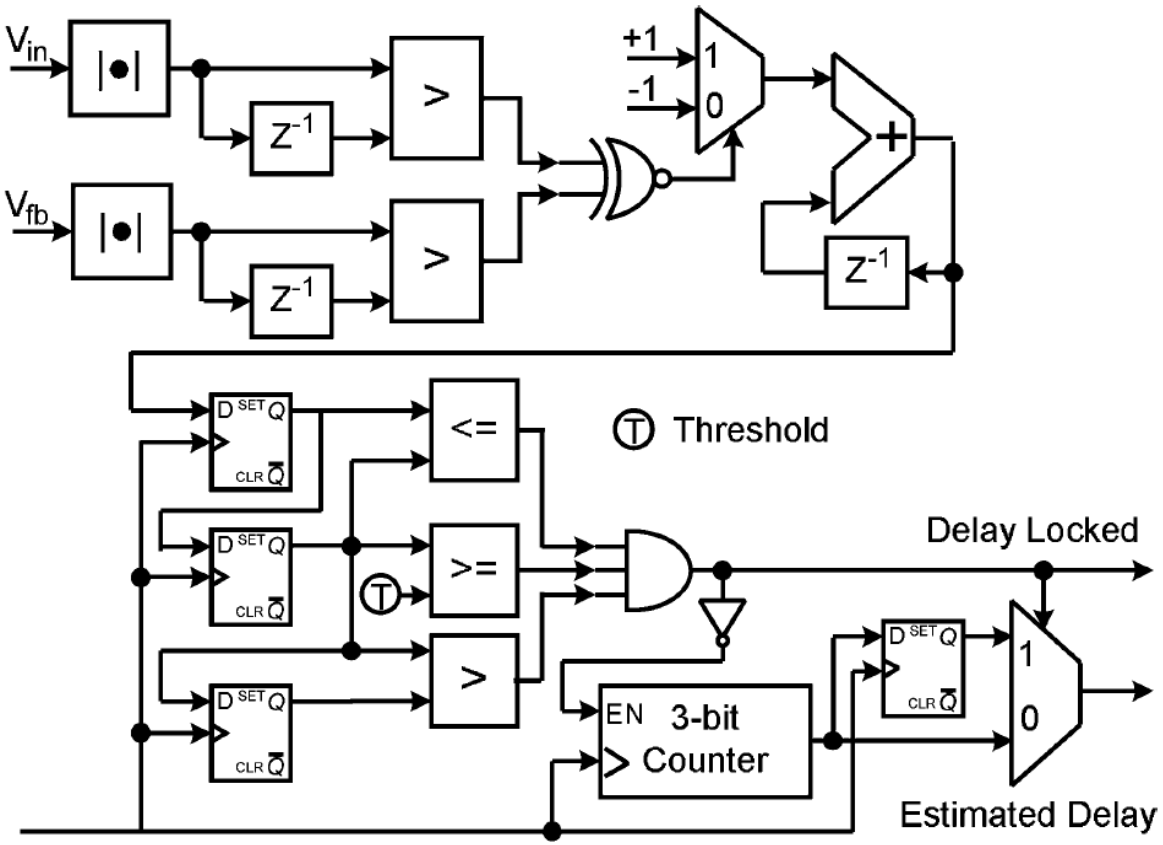
- A correlation-based approach.
- Amplitude difference function of input and feedback signals are computed as follows:

$$D[v(n)] = sign[|v(n)| - |v(n-1)|]$$

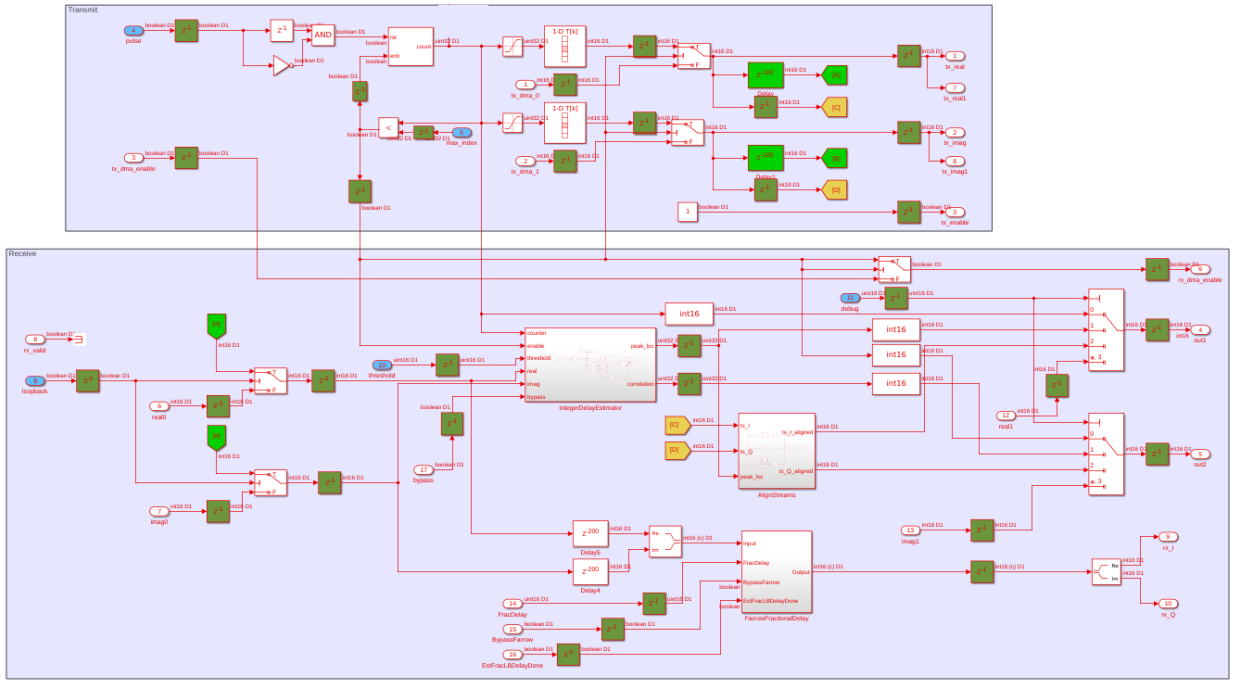
- Autocorrelation of the resultant signals:

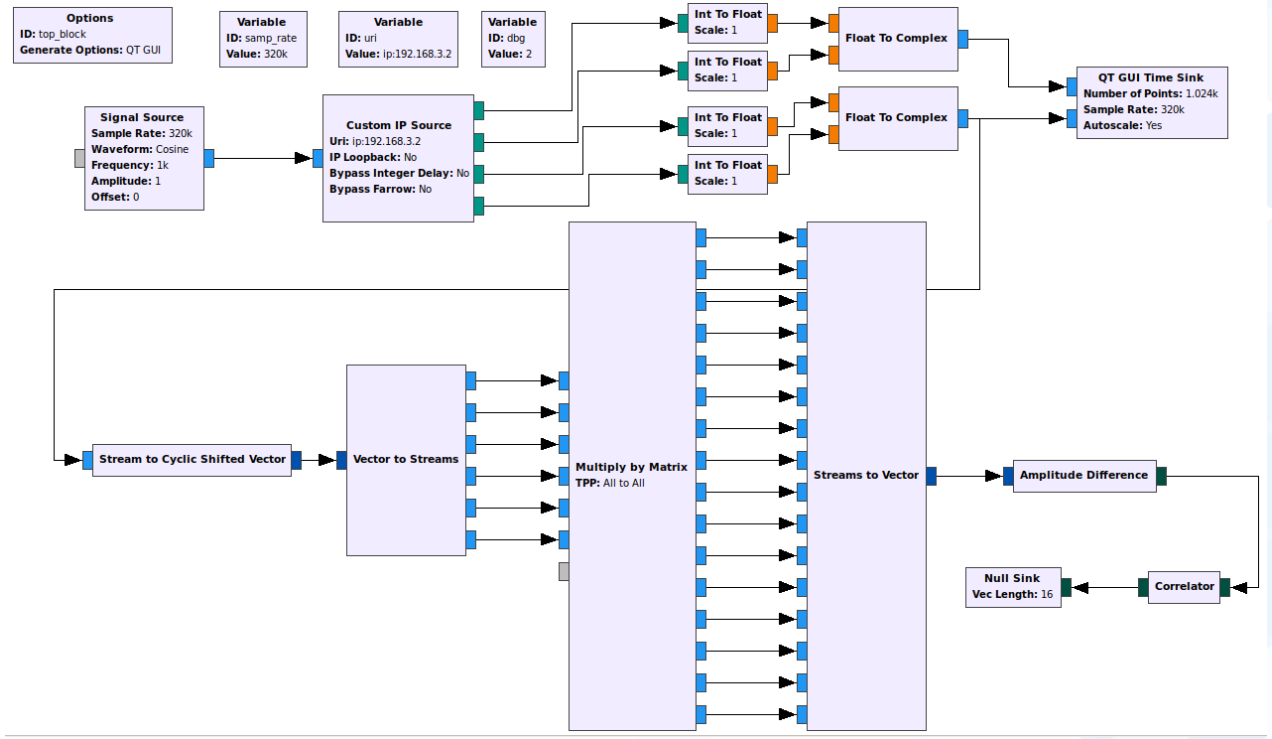
$$R(m) = \sum_{i=1}^{M} D[v_{in}(i-m)]D[v_{fb}(i)]$$

- Find index where peak appears.



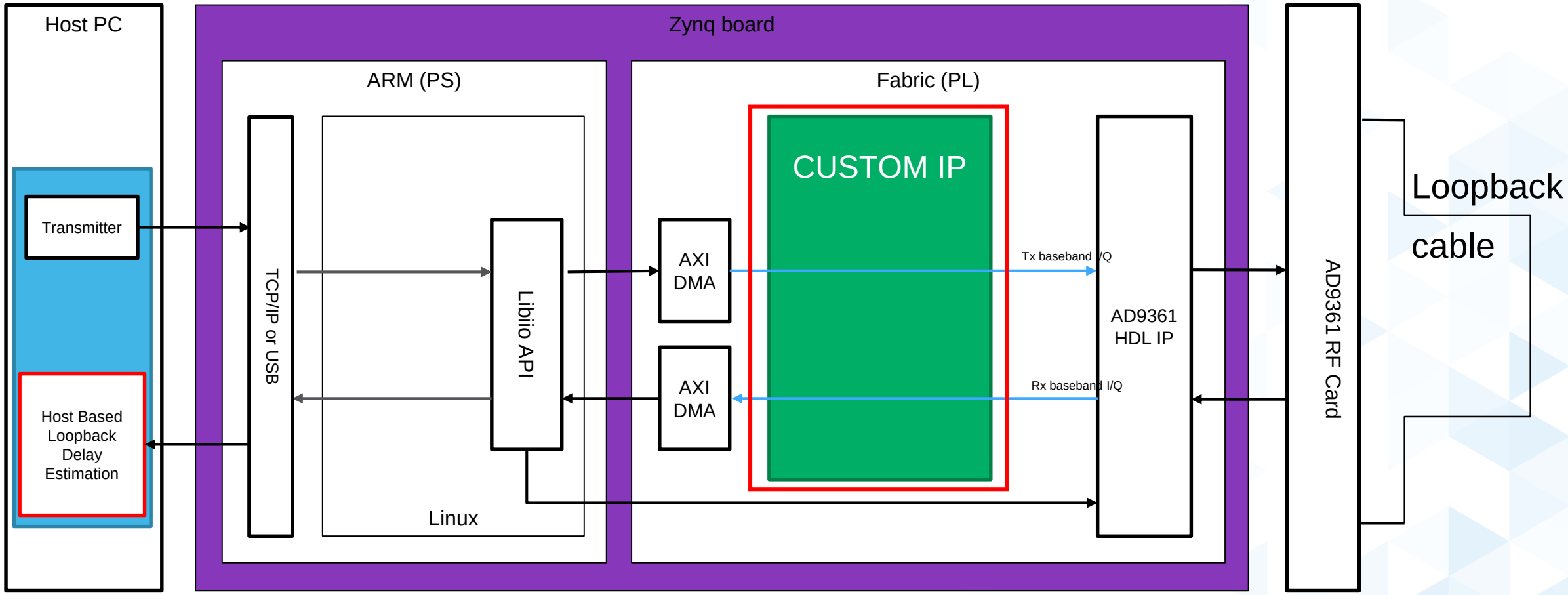
Reference Design





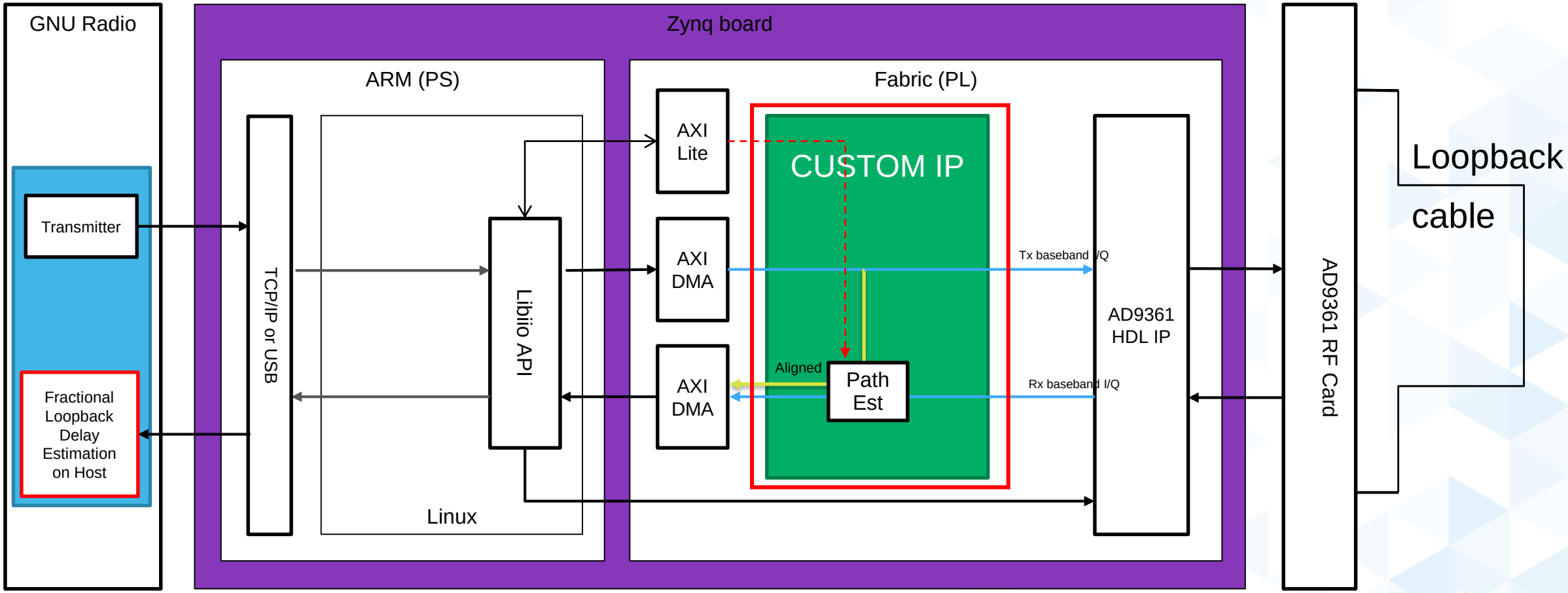
Reference Design

- Both integer and fractional loopback delay estimation are implemented on the host.



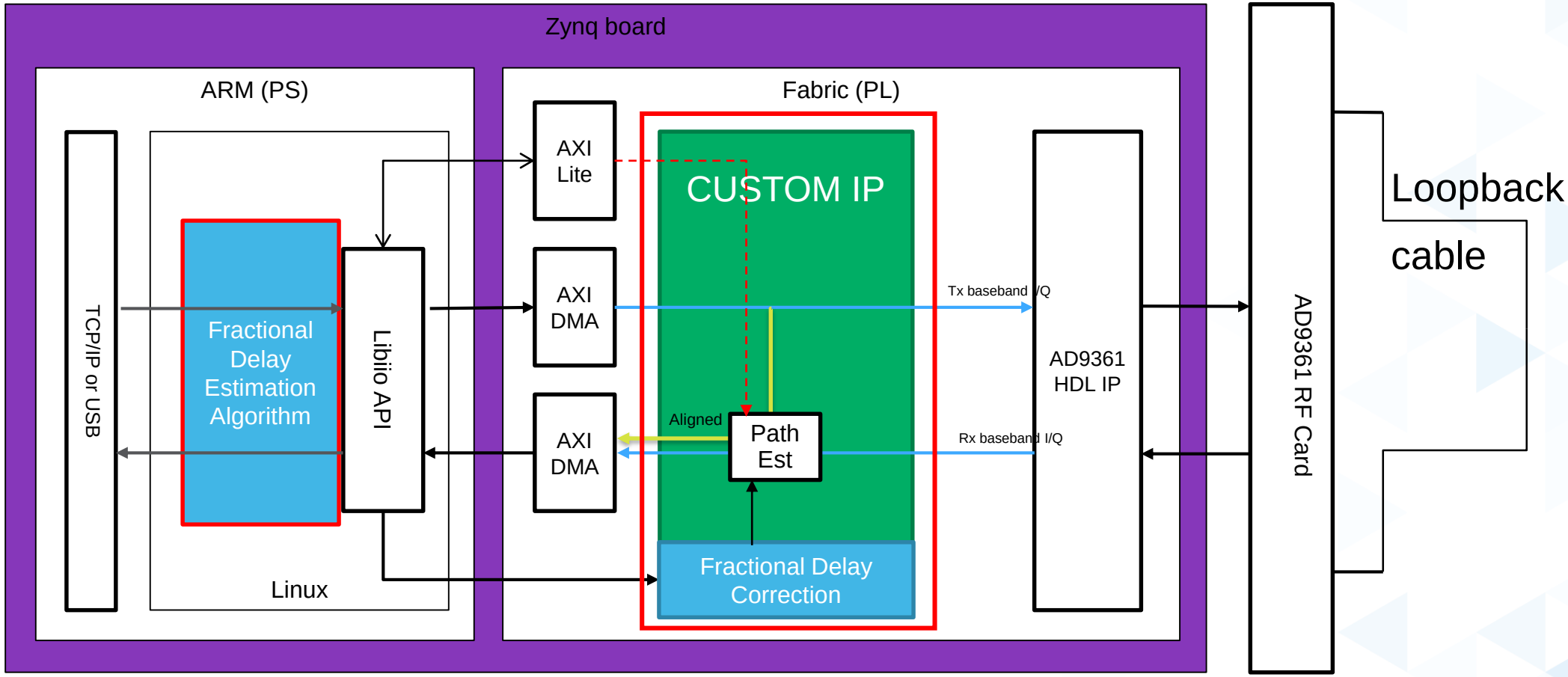
Reference Design

- Integer loopback delay estimation is implemented in FPGA, whereas fractional loopback delay is implemented in GNU Radio on the host.



Reference Design

- Transmit data is read using a GR application in ARM.



Loopback Delay Measurement Results

- Loopback delay algorithm deployed on FPGA.
- Three cables of different lengths tested to determine accuracy of algorithm.

Mean Loopback Delay

	Cable Length = 8 in	Cable Length = 10 in	Cable Length = 16 in
Sample Rate = 3 MSPS	0.52 µs	0.72 µs	1.1 µs
Sample Rate = 6 MSPS	0.54 µs	0.75 µs	1.06 µs
Sample Rate = 9 MSPS	0.51 µs	0.74 µs	1.04 µs
Expected	0.434 µs	0.612 µs	0.946 µs

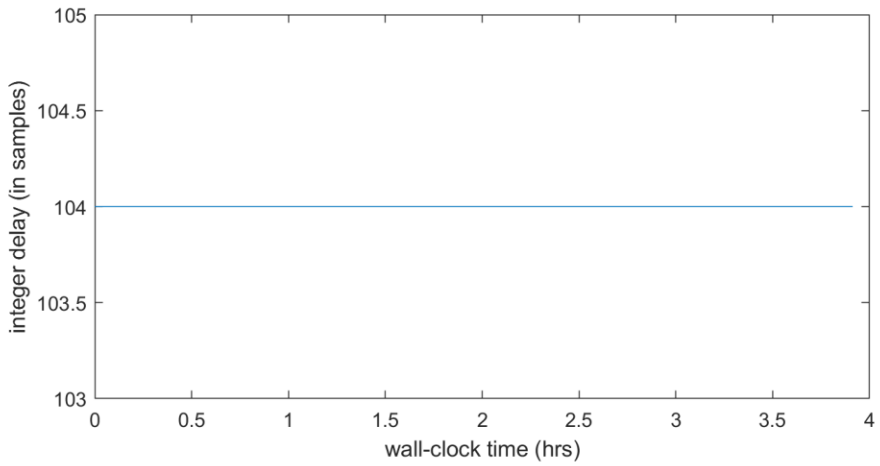
Loopback Delay Measurement Results

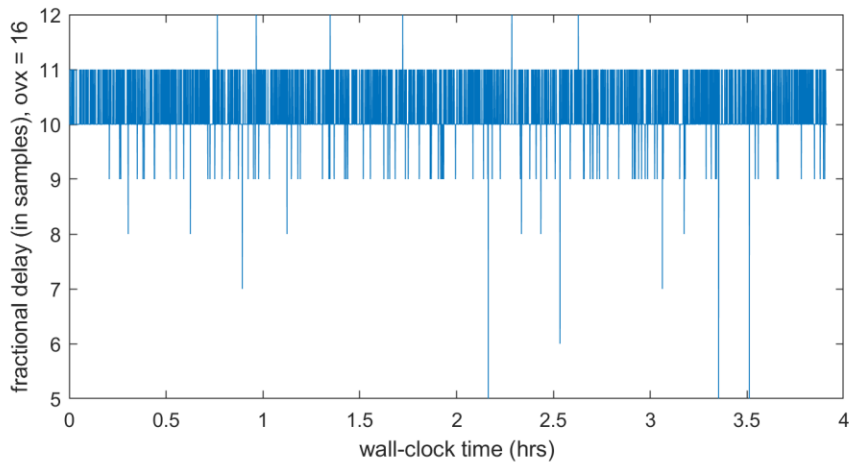
Std. Dev of Loopback Delay

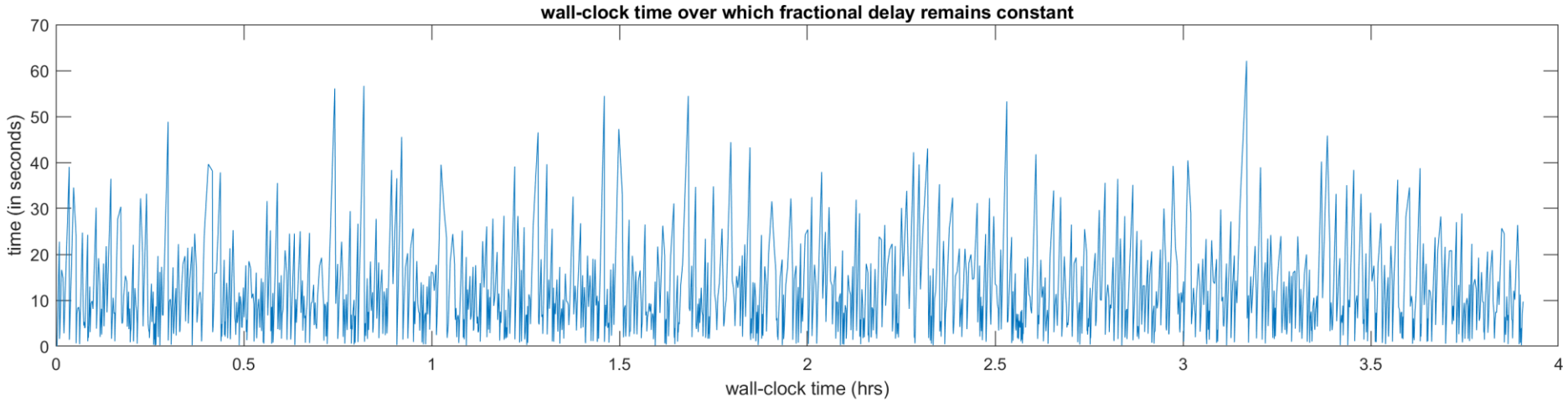
	Cable Length = 8 in	Cable Length = 10 in	Cable Length = 16 in
Sample Rate = 3 MSPS	0.02 µs	0.02 µs	0.03 µs
Sample Rate = 6 MSPS	0.02 µs	0.03 µs	0.04 µs
Sample Rate = 9 MSPS	0.03 µs	0.02 µs	0.02 µs

- A delta of the order of tenths of µs observed between observed and theoretical value.
- Possibly due to the on-chip interconnects, propagation through DSP etc.

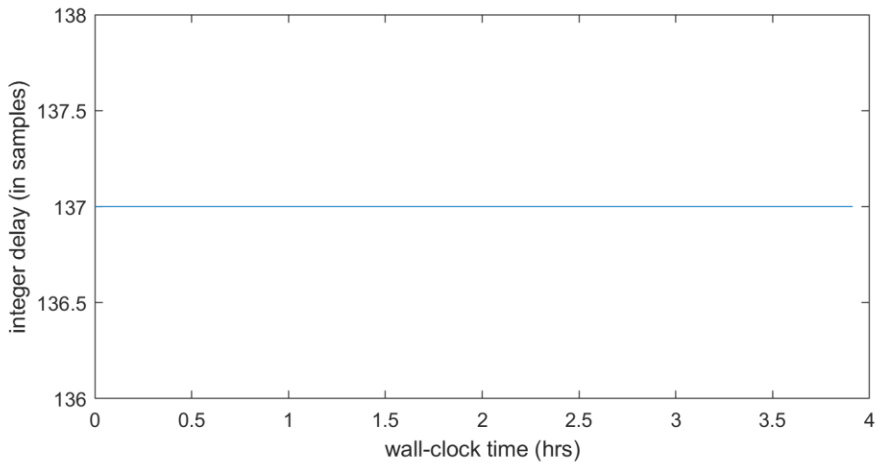
Loopback Delay Measurement Results

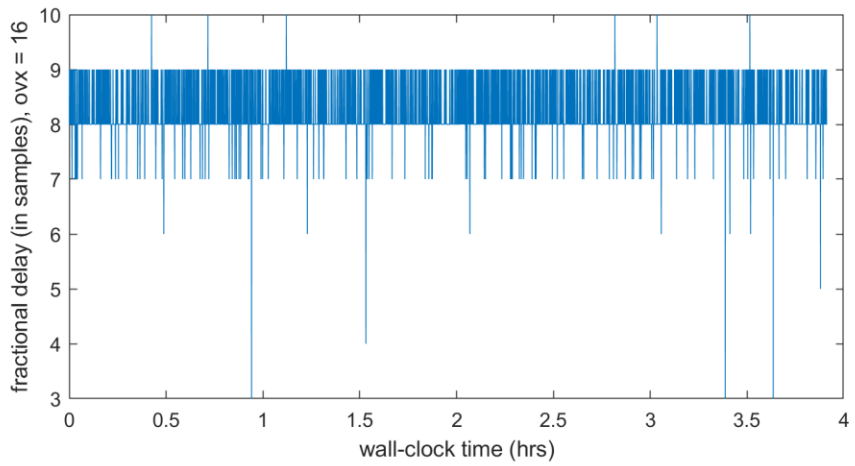


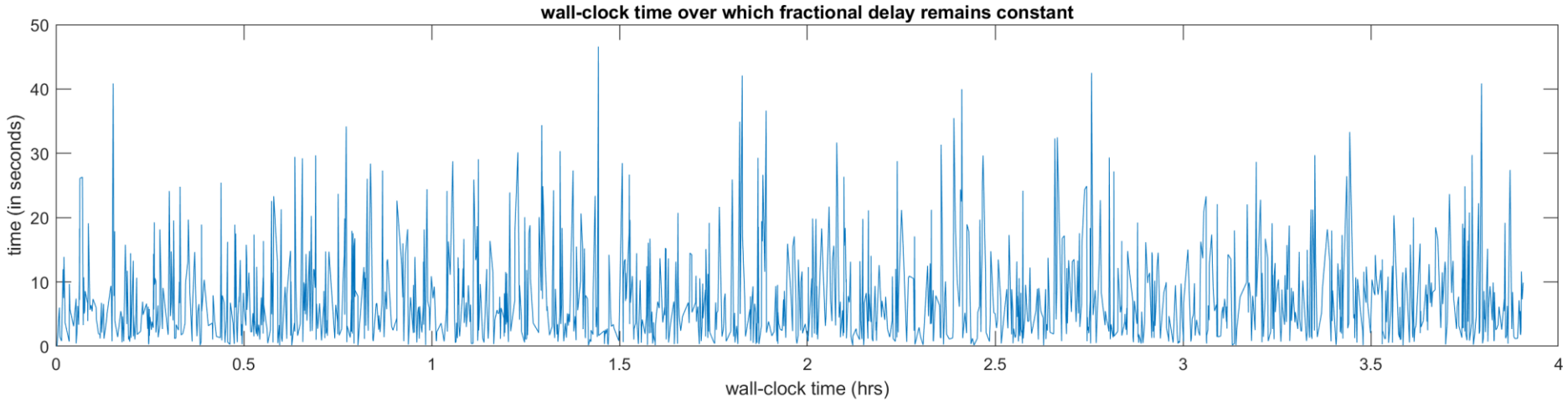




Loopback Delay Measurement Results







Q &A

Thank you!

Visit our booth for a demo.