CML Microcircuits
COMMUNICATION SEMICONDUCTORS

CMX998
Cartesian Feed-back Loop Transmitter

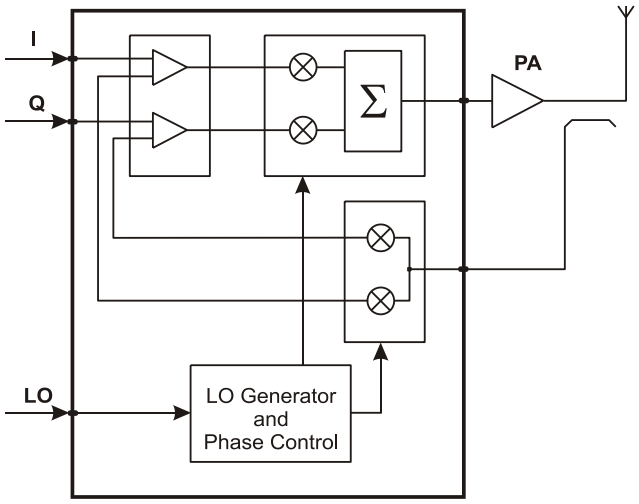
D/998/16 May 2021

Features

- Frequency Range 30MHz to 1GHz
- Wide Band Noise –148dBc/Hz
- C-BUS (SPI compatible) Serial Interface
- Gain Control
- Error Amplifier
- Up Converter Forward Path
- Down Converter for Feedback Linearisation
- 360° Loop Phase Shift Control
- DC Offset Measurement Output
- Open Loop Function
- Instability Detector
- Flexible Digital Interface

Applications

- TETRA Terminals
- TETRA 2 Terminals
- APCO P25 Phase 2
- Aviation Systems
- Mobile Satellite Terminals
- Linear Modulation Schemes: QPSK, π/4-DQPSK, 8PSK, QAM, OFDM, F4FM, etc.
- Direct Interface to CMX981, CMX980A and CMX7163/CMX7164



1 Brief Description

A Cartesian Loop improves the efficiency and linearity of transmitters for non-constant envelope modulation systems.

The CMX998 is an integrated solution for a Cartesian Feedback Loop based linear transmitter. Acting as a direct conversion quadrature mixer from I and Q to RF output, it provides the capability to linearize the Power Amplifier (PA) via feedback from the PA's output. Included are forward and feedback paths; local oscillator circuitry including loop phase control; an instability detector and uncommitted op-amps for input signal conditioning.

The device operates from a single 3.3V supply over a temperature range of -40°C to +85°C and is available in a 64-pin VQFN (Q1) package.

CONTENTS

2 Block Diagram

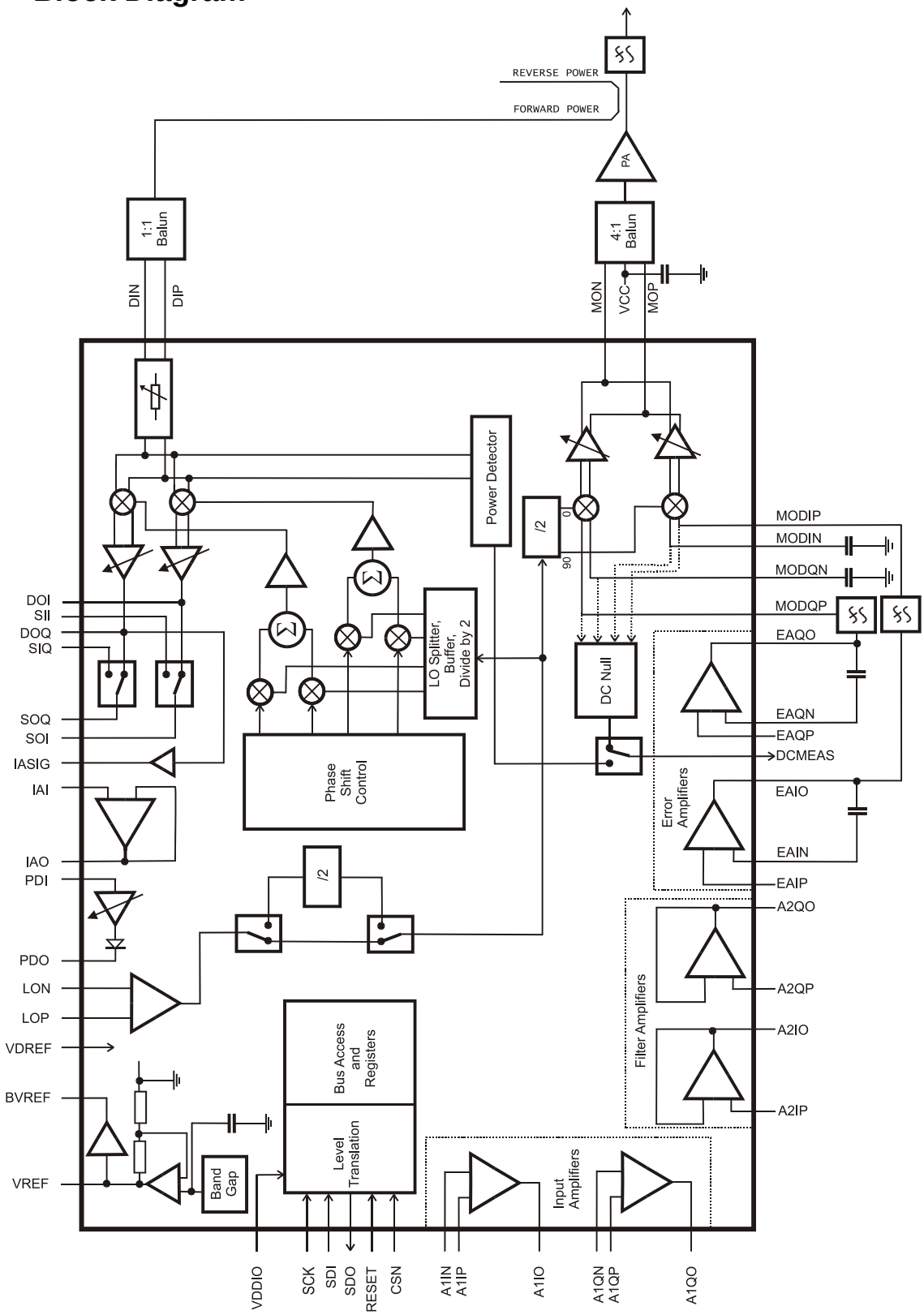


Figure 1 Block Diagram

3 Signal List

Package Q1 Pin No.	Name	Description
1	A2QO	Amplifier 2 output (Q Channel)
2	EAQP	Error Amplifier Input Positive (Q Channel)
3	EAQN	Error Amplifier Input Negative (Q Channel)
4	EAQO	Error Amplifier Output (Q Channel)
5	MODQP	Modulator Input (Q Channel)
6	MODQN	Modulator input reference (Q Channel)
7	VEEQTX	Analogue Ground for Q Channel Modulator
8	MON	Modulator Output Negative
9	MOP	Modulator Output Positive
10	VEEITX	Analogue Ground for I Channel Modulator
11	MODIN	Modulator input reference (I Channel)
12	MODIP	Modulator Input (I Channel)
13	EAIO	Error Amplifier Output (I Channel)
14	EAIN	Error Amplifier Input Negative (I Channel)
15	EAIP	Error Amplifier Input Positive (I Channel)
16	A2IO	Amplifier 2 output (I Channel)
17	A2IP	Amplifier 2 input Positive (I Channel)
18	A1IO	Amplifier 1 Output (I Channel)
19	A1IN	Amplifier 1 Input Negative (I Channel)
20	A1IP	Amplifier 1 Input Positive (I Channel)
21	VCCITX	Analogue Supply for I Channel Modulator
22	VCCLO1	Analogue Supply for LO path
23	VEELO1	Analogue Ground for LO path
24	LON	Local Oscillator Negative Input (Note: when differentially driving LOP and LON this LON pin requires a low impedance dc path to ground otherwise it may be decoupled to ground)
25	LOP	Local Oscillator Positive Input (Note: this pin requires a low impedance dc path to ground)
26	VEELO2	Analogue Ground for LO path
27	VCCLO2	Analogue Supply for LO path
28	VCC	Analogue Supply
29	Spare	(Do not connect to this pin: reserved for future use)
30	VREF	Bandgap reference decoupling
31	BVREF	Buffered V_{REF}
32	VEE	Analogue Ground (0V)
33	DCMEAS	DC Measurement Output
34	VDREF	Reference Supply for monitor signals full scale value
35	VCCIRX	Analogue Supply I Channel Downconverter
36	SOI	Switch Output (I Channel)
37	SII	Switch Input when open loop (I Channel)
38	DOI	Demodulator Output (I Channel)
39	VEEIRX	Analogue Ground I Channel Downconverter
40	DIP	Demodulator Input Positive
41	DIN	Demodulator Input Negative
42	VEEQRX	Analogue Ground Q Channel Downconverter
43	DOQ	Demodulator Output (Q Channel)
44	SIQ	Switch Input when open loop (Q Channel)

Package Q1 Pin No.	Name	Description
45	SOQ	Switch Output (Q Channel)
46	IASIG	Demodulator Output for Instability Detector
47	VCCQRX	Analogue Supply Q Channel Downconverter
48	IAI	Instability Amplifier Input
49	IAO	Instability Amplifier Output
50	PDI	Peak Detector Input
51	PDO	Peak Detector Output
52	VDD	Digital Supply
53	VDDIO	Supply voltage for digital control interface
54	SCK	C-BUS Serial Clock
55	SDI	C-BUS Command Data Input
56	SDO	C-BUS Reply Data Output
57	CSN	C-BUS Enable
58	RESET	General RESET (RESET active LOW)
59	VSS	Digital Ground
60	VCCQTX	Analogue Supply for Q Channel Modulator
61	A1QP	Amplifier 1 Input Positive (Q Channel)
62	A1QN	Amplifier 1 Input Negative (Q Channel)
63	A1QO	Amplifier 1 Output (Q Channel)
64	A2QP	Amplifier 2 Input Positive (Q Channel)
EXPOSED METAL PAD	VEE	This pad must be connected to Analogue Ground (0V).

Table 1 Pin List

3.1 Signal Definitions

Signal Name	Pins	Usage
AV_{DD}	VCC, VCCIRX, VCCQRX, VCCITX, VCCQTX, VCCLO2, VCCLO1	Power supply for analogue circuits
DV_{DD}	VDD	Power supply for digital circuits
VD_{IO}	VDDIO	Power supply voltage for digital interface (C-BUS)
VD_{ref}	VDREF	Power Supply for scaling analogue measurement signal outputs. (RF detector, instability detector and dc offset measurement)
DV_{SS}	VSS	Ground for digital circuits
AV_{SS}	VEE, VEEIRX, VEEQRX, VEEITX, VEEQTX, VEELO2, VEELO1	Ground for analogue circuits
V_{REF}	VREF	Connection for decoupling of internal band-gap reference voltage
BV_{REF}	BVREF	Buffered version of V_{REF} which may be used for bias of input signals etc.

Table 2 Definition of Power Supply and Reference Voltages

4 External Components

4.1 Power Supply Decoupling

The CMX998 has separate supply pins for the analogue and digital circuitry: a 3.3V nominal supply is recommended for all circuits.

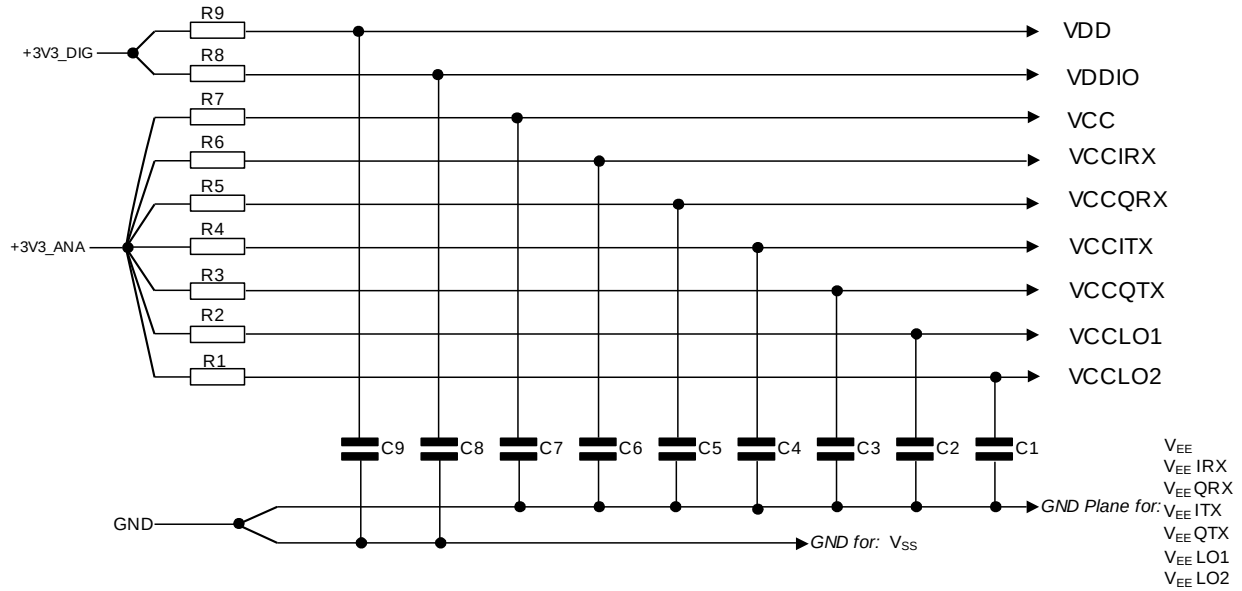


Figure 2 Power Supply Connections and Decoupling

C1	10nF	R1	3.3 Ω
C2	10nF	R2	3.3 Ω
C3	10nF	R3	3.3 Ω
C4	10nF	R4	3.3 Ω
C5	10nF	R5	3.3 Ω
C6	10nF	R6	3.3 Ω
C7	10nF	R7	3.3 Ω
C8	10nF	R8	10 Ω
C9	10nF	R9	10 Ω

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated

Note:

It is expected that low frequency interference on the 3.3 Volt supply will be removed by active regulation; a large capacitor is an alternative but may require more board space and so may not be preferred. It is particularly important, to ensure that there is no interference from the VDDIO (which supplies the digital I/O) or from any other circuit that may use the +3V3_DIG supply (such as a microprocessor), to sensitive analogue supplies like VCCITX or VCCIRX. It is therefore advisable to use separate power supplies for the digital and analogue circuitry.

The supply decoupling shown is intended for RF noise suppression. It is necessary to have a small series impedance prior to the decoupling capacitor for the decoupling to work well; this may be cost effectively done with the resistor and capacitor values shown. The use of resistors results in small dc voltage drops (up to approx 0.1V). Choosing resistor values approximately inversely proportional to the dc current requirements of each supply, ensures the dc voltage drop on each supply are reasonably matched. In any case the dc voltage change that results is well within the design tolerance of the device. If higher

impedance resistors are used (not recommended) then greater care will be needed to ensure the supply voltages are maintained within tolerance, even when parts of the device are enabled or disabled.

It is also advisable to have separate ground planes for the analogue and digital circuits.

4.2 Upconverter

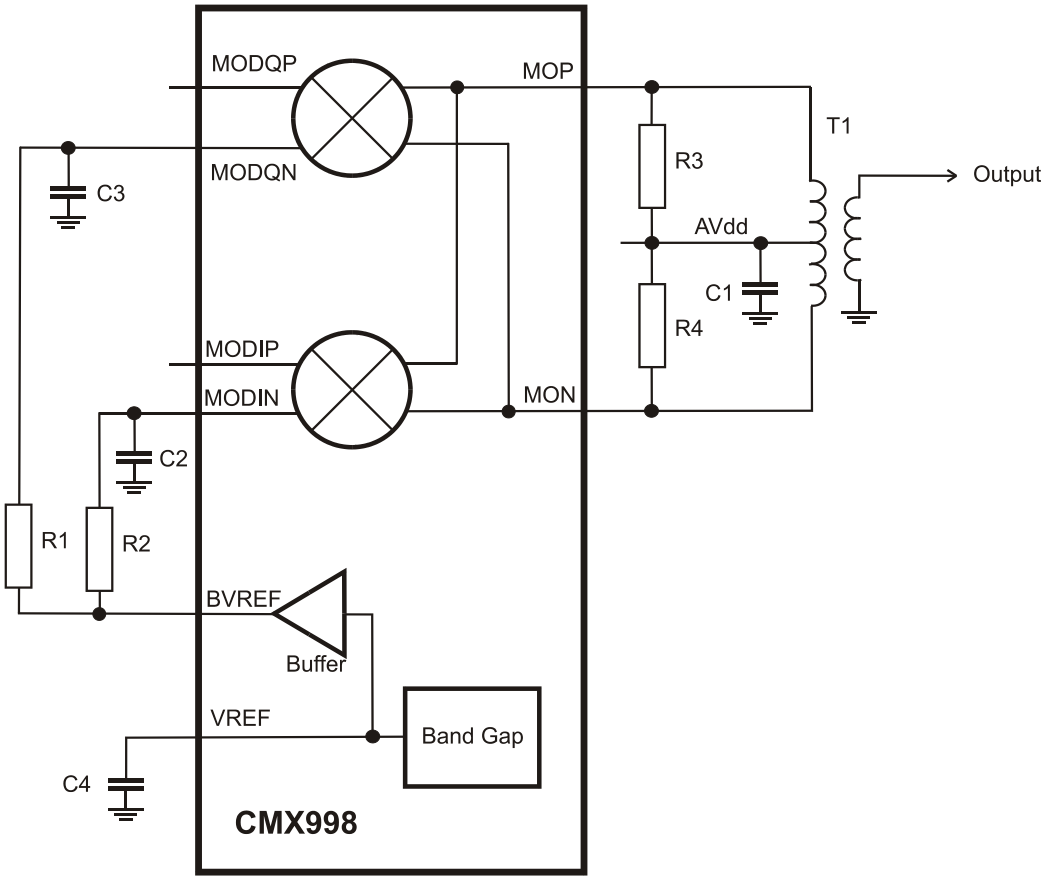


Figure 3 Modulator and Bias External Components

C1	10nF	T1	Balun 4:1 (See note 1)
C2, C3	33nF	R1, R2	100 Ω
C4	1µF	R3, R4	(See note2)

Note 1: For example TC4-14+ from mini circuits, for applications between 200MHz and 1GHz, or Coilcraft WBC4-1WL, for applications between 30MHz and 300MHz.

Note 2: The resistors R3 and R4 are optional. Fitting these with 110 Ω resistors will give a good broadband match however will reduce output level available. For many applications they will be unnecessary.

Table 3 Up-converter Components

Note: A simplified output circuit described in an Application Note for the CMX993 may also be used with the CMX998, details available from www.cmlmicro.com.

4.3 Down Converter

A 1:1 balun transformer should be used on the input to the down converter.

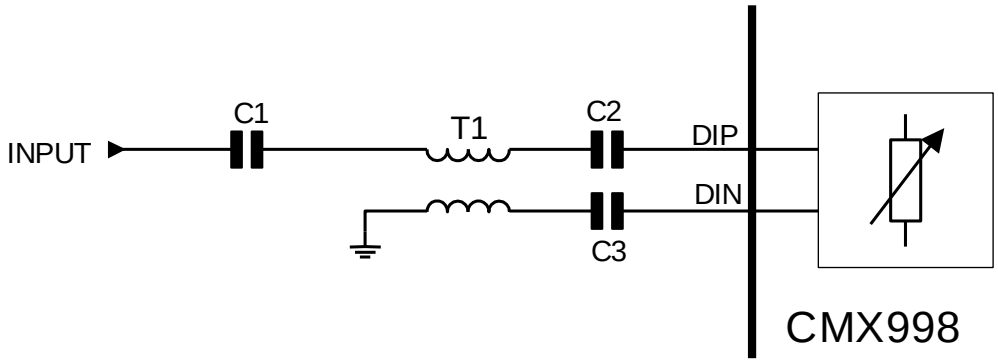


Figure 4 Downconverter External Component Configuration

C1	1nF	T1	Balun 1:1 (e.g. TC1-1-13M from Mini Circuits)
C2	1nF		
C3	1nF		

4.4 Local Oscillator Input

A 1:1 balun transformer should be used on the local oscillator input for optimum performance. In the local oscillator divide by 4 mode, a single ended input may be used by decoupling the LON pin to ground and applying the LO signal to LOP noting that a dc path to ground on LOP must still be provided.

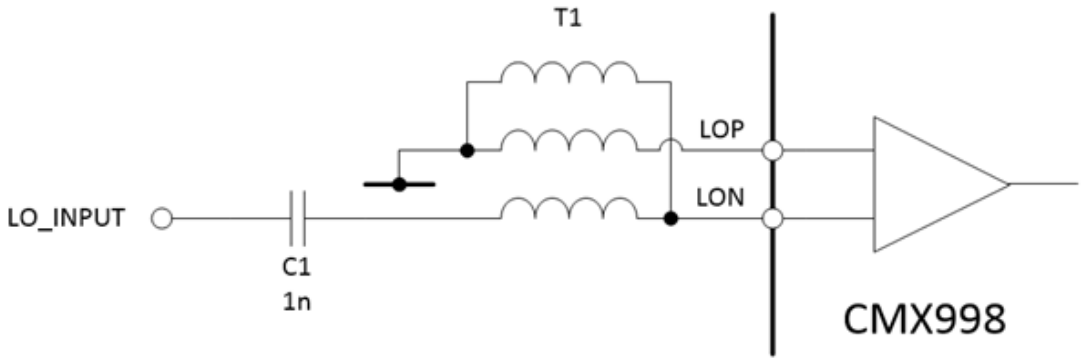


Figure 5 LO Input Configuration using a 1:1 Balun

C1	1nF	T1	Balun 1:1 (e.g. MABA-007748-CT1160) from M/A-com, see Note 3)

Notes:

1. The configuration of the 1:1 balun used at the LO input has to create a dc path to analogue GND for both LO inputs, LOP and LON, as shown in Figure 5.
2. The capacitor C1 is optional and should be used where the 0V dc connection provided by the balun is not acceptable to the circuitry providing the LO signal.
3. The MABA-007748-CT1160 is specified between 5MHz and 1.2GHz. The part has been found to remain functional with the CMX998 up to at least 2GHz, however, such operation is outside the manufacturer's rating.

4.5 Instability Detector

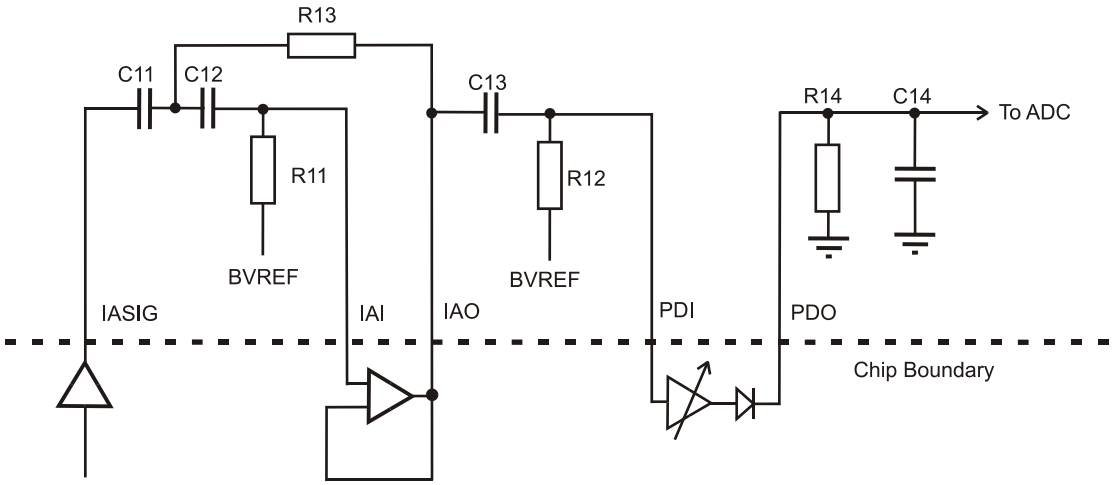


Figure 6 Typical Instability Detector Section Configuration

C11	1nF	R11	47kΩ
C12	220pF	R12	4.7kΩ
C13	470pF	R13	1.8kΩ
C14	47nF	R14	470kΩ

Table 4 Instability Detector Components with Passband above 40kHz

C11	150pF	R11	56kΩ
C12	22pF	R12	4.7kΩ
C13	68pF	R13	1.5kΩ
C14	47nF	R14	470kΩ

Table 5 Instability Detector Components with Passband above 300kHz

4.6 Error Amplifier

A typical error amplifier configuration is shown in Figure 7.

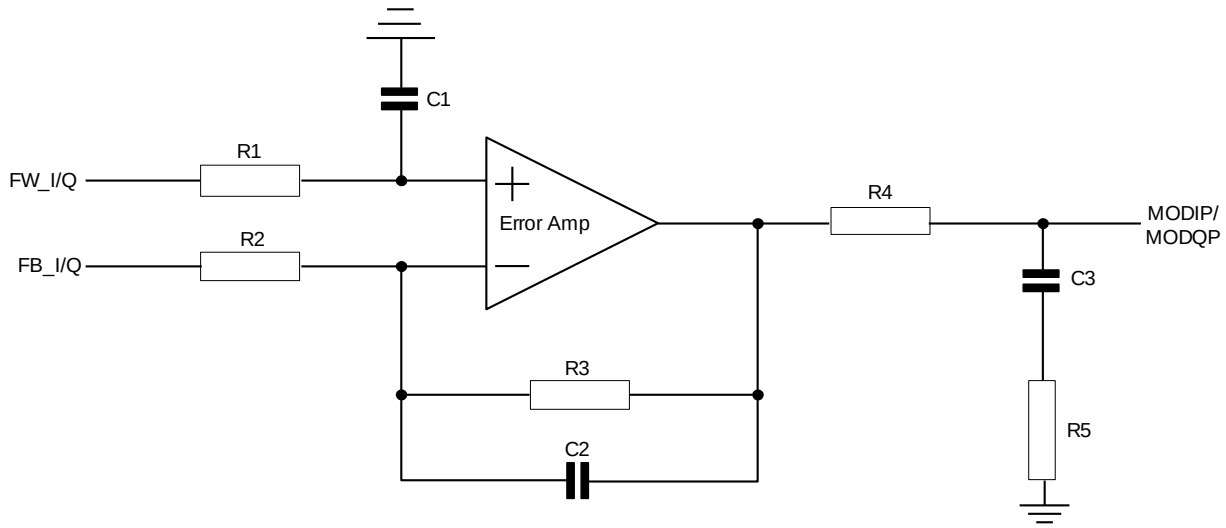


Figure 7 Error Amplifier External Component Configuration

C1	100pF	R2	1kΩ
C2	100pF	R3	100kΩ
C3	33nF	R4	150Ω
R1	1kΩ	R5	15Ω

Table 6 Error Amplifier Typical Component Values

The component values shown in Table 6 give 40dB of gain, with the 1st pole at ~16kHz, 2nd pole at ~32kHz and the zero at ~320kHz.

5 General Description

The CMX998 is single chip transmitter IC providing all the functionality necessary to implement a Cartesian Feed-back Loop transmitter with the addition of an external power amplifier, coupler and fixed value feed-back attenuator as shown in Figure 8. A detailed block diagram of the IC is shown in section 2. The IC can support a wide range of modulation formats and standards including TDMA operation. Cartesian Feed-back linearisation is typically used for applications with signal bandwidths of up to 200 kHz and useful linearisation has been demonstrated up to at least 400 kHz frequency offsets. Performance in any application will depend on loop configuration and the figures quoted are not 'hard' limits, just guidelines.

The following sections describe the functionality of the IC.

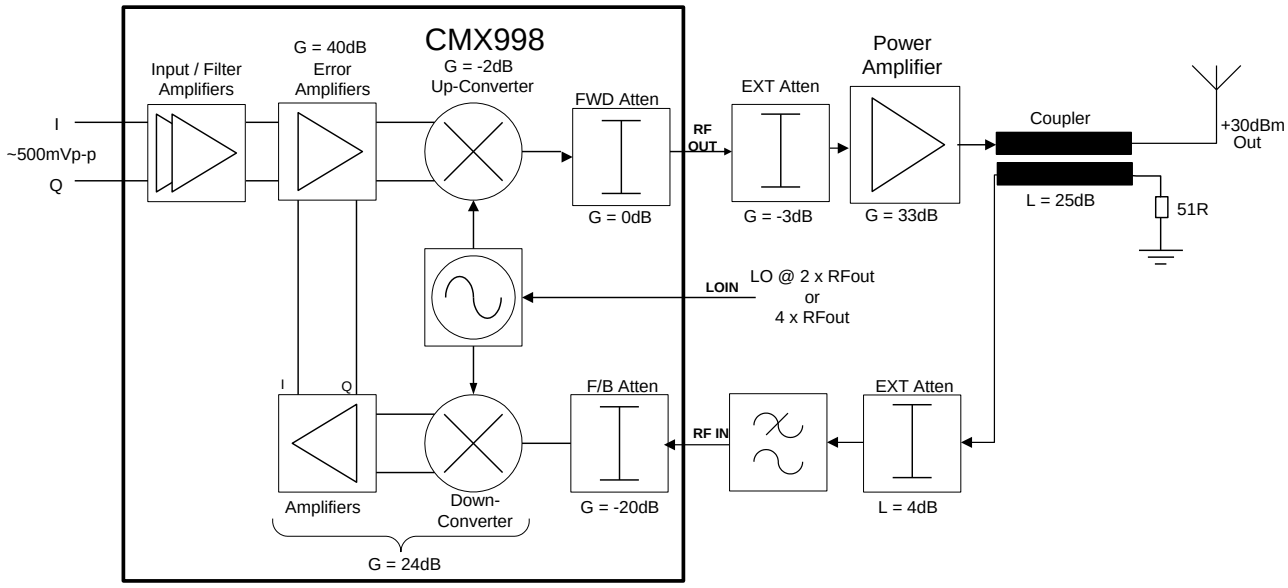


Figure 8 Typical Cartesian Loop Configuration using the CMX998

5.1 Input Amplifiers

Differential amplifiers are provided for conversion of differential input signals to single ended format. This is necessary when interfacing to the CMX980A / CMX981 Advanced Digital Baseband Processor or CMX7163FI-4/CMX7164FI-4 QAM Modem. This amplifier may also be configured to provide dc level translation, filtering and signal gain/attenuation.

Further amplifiers are provided that may be used to implement additional filtering, if required.

5.2 Forward Path

The forward path of the IC comprises two 'error amplifiers' followed by an I/Q vector modulator.

The 'error amplifiers' are differential amplifiers where the feedback signal is compared with the reference modulation input and an 'error' signal is produced. This 'error' signal is effectively a pre-distorted waveform that when applied to the remainder of the forward path will produce a 'perfect' signal at the output. To ensure loop stability a filter must be used. The 'error amplifier' may be configured as an active filter /

integrator to provide this function. The bandwidth of the filter is selectable with external components as this can be used to optimise parameters in the loop. Additional filtering may be used between the 'error amplifier' output and the input to the I/Q modulator.

The I/Q modulator provides translation from baseband I and Q signals to a modulated RF signal. The wideband noise of this modulator is optimised to ensure a low noise floor at the output, compliant with common product standards. This stage also provides gain control to allow levels around the loop to be optimised.

5.3 Feedback Path

The feedback path of the IC comprises a variable attenuator, down-converter I/Q mixers, baseband amplifiers and switching, to enable operation in 'open loop' mode.

Linearity of the down-converter is critical to the overall performance of the Cartesian loop, also a low noise figure is vital to ensure that emissions limits of typical product standards are met. As a result the input attenuators and I/Q down-converter mixers offer an excellent combination of noise and linearity.

Low noise baseband amplifiers provide the correct gain to ensure signal levels around the loop are optimised for noise and linearity. The baseband chain provides various outputs to allow connection to monitoring ADC for loop calibration. To ensure the loop has good stability and can thus achieve maximum linearisation, the down-converter baseband path is broadband and achieves low time-delay.

The loop switches provide the ability to break the loop and operate in open loop mode while simultaneously reducing the gain of the error amplifiers. This mode can be useful for loop phase calibration. When the loop switches are in the normal (closed loop) position, the output of the down-converter is connected to the error amplifiers via external resistors. With the loop switches open, the error amplifier inputs are connected to the SII and SIQ pins. These pins may be connected to the reference voltage via a resistor which may be chosen to set the error amplifier gain in the open-loop mode.

5.4 Local Oscillator Phase Shifting

The local oscillator signal supplied to the IC may be at twice or four times the desired operating frequency and a selectable divider is provided to select between these two options. Internal division is used to generate in phase and quadrature local oscillator signals. The feedback path LO chain has a 360 degree phase shifter included to allow loop phase to be adjusted. The forward path LO chain is optimised for low noise to achieve the best possible wideband noise floor of the transmitter.

A bit is provided in the frequency control register to tune the phase shifter for optimum phase step accuracy at low and high frequencies, the breakpoint being around 500MHz.

Note 1: It is recommended that the signal provided to the CMX998 does not have excessive spurious or harmonic content.

Note 2: The amplitude of the LO signal applied has an influence on down-converter quadrature accuracy particularly for operating frequencies above 600MHz, the accuracy also varies with phase shifter setting in a pattern that repeats over each quadrant; see also note 6b in section 7.1.3.

5.5 DC Nulling

Note: Further information on DC Nulling is available in an Application Note available from: www.cmlmicro.com.

An error in the dc content of the drive to the up-converter modulator will result in carrier leakage in the output signal. In the Cartesian loop, dc signals can be caused by offset errors generated in the down-converter path, or errors in the input signal. It is possible to correct the errors by pre-compensating the input signal. The IC includes circuits to allow easy measurement of the error between the reference and the modulation signal from the error amplifier, as shown in Figure 9.

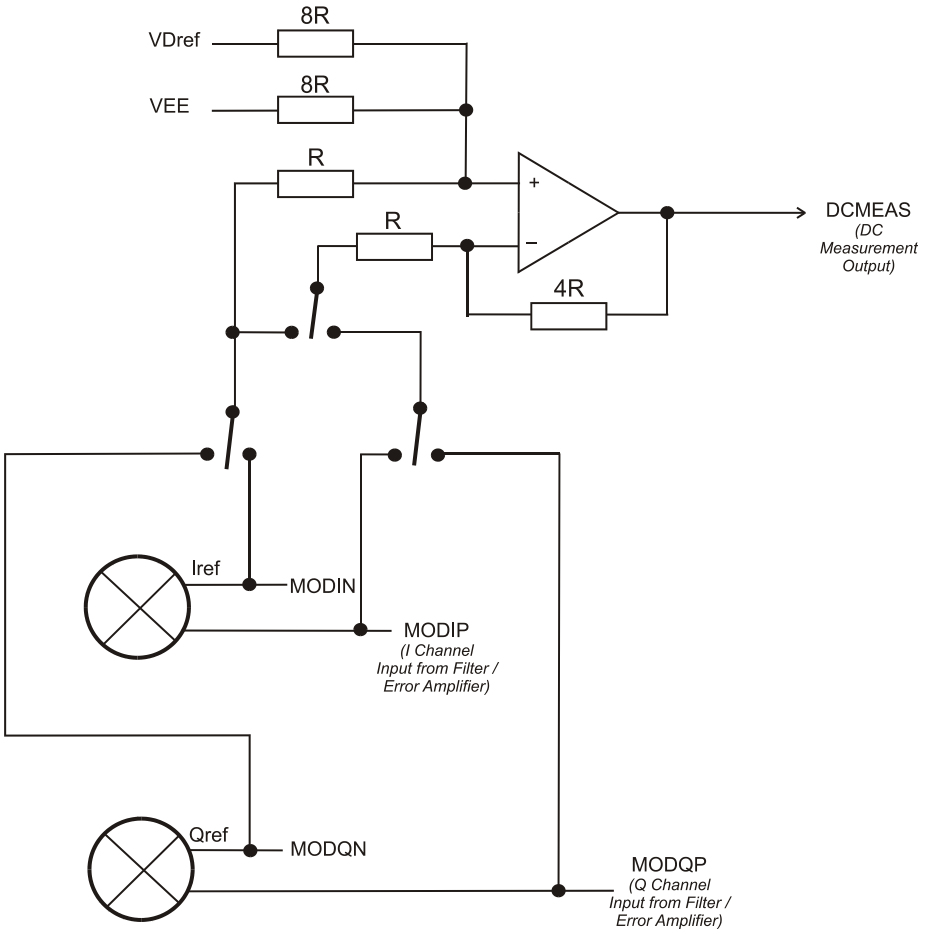


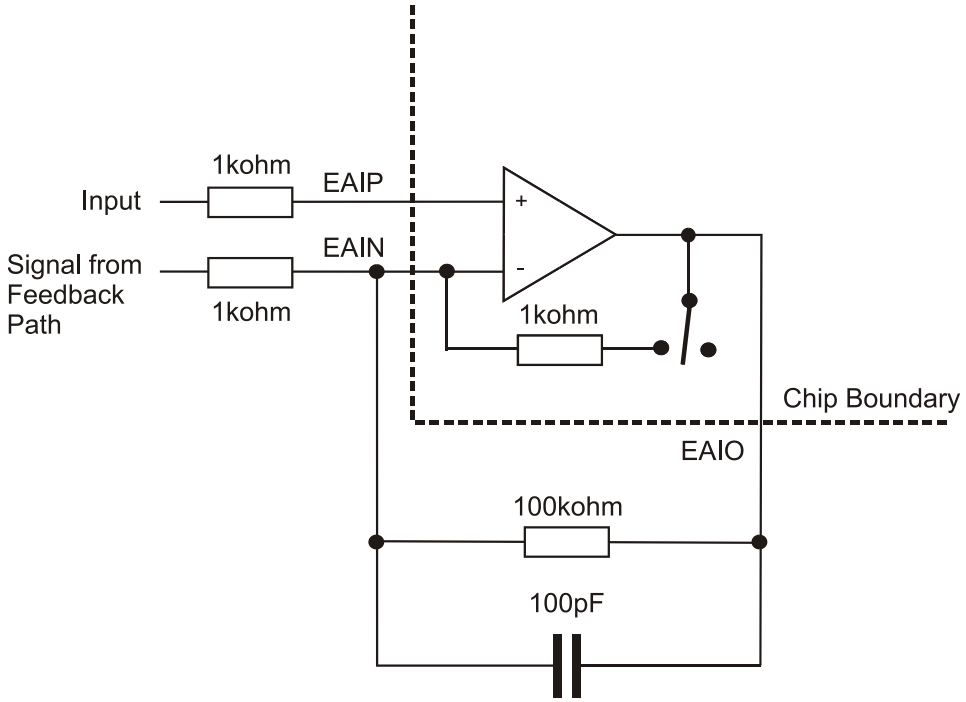
Figure 9 Configuration of DCMEAS output switching

The levels have been optimised to allow direct interface to an ADC. If the CMX980A, CMX981 or CMX7163 is used to generate the I/Q input signals the auxiliary ADC in the same device can be used for measuring the dc offset levels. The x4 scaling of the error allows easy digital arithmetic to find the dc offset correction values which can then be loaded into the CMX980A / CMX981 Transmit I Channel Offset Register and the Transmit Q Channel Offset Register (or equivalent features in the CMX7163FI-4).

The DC Bias Measurement Output (DCMEAS) is a measure of the difference between the mixer reference voltage and the I or Q channel input to the mixer (normally driven from the error amplifier). The measurement is taken from the input to the mixers to allow any losses / gains due to external circuits after the error amplifier to be included in the measurement. The DCMEAS output is centred around a nominal voltage of $VD_{ref}/2$ (see Figure 9). In a typical application the VD_{ref} input should be the full scale voltage of the ADC used to sample DCMEAS output. Any error in the reference bias point (VD_{ref} /2) may be removed from the measurement by connecting both the differential inputs to the mixer bias, as can be see in Figure 9. If DCMEAS is sampled in this mode, then measured with the mixer input signal connected to one of the differential inputs, the difference between the two results is a measure of the dc offset, excluding the effect of VD_{ref} /2.

The reference voltage (VD_{ref}) may have any value from 2.1 volts up to the same voltage as AV_{DD}. VD_{ref} may not be greater than AV_{DD} + 0.3V. The VD_{ref} supply is shared with the instability detector and the RF detector circuits. The dc bias measurement output pin 'DCMEAS' is shared with the RF detector circuit. The decoder circuit for enabling the two functions, DCMEAS or RF detector, results in these functions being mutually exclusive.

To aid the measurement and correction of dc levels, the error amplifiers have an internal feedback resistor which may be connected between the output pin and the negative input of each amplifier. A typical configuration is shown in Figure 10. In the normal closed loop operation the error amplifier will typically have a high gain, e.g. 40dB as shown in the figure. In this case the internal switch should be open. During measurement of dc parameters it may be beneficial to reduce the error amp-gain, in which case the internal switch may be closed using the general control register. This method of error amplifier gain reduction is in addition to that provided by the loop switches (see section 5.3).



Note: Only the I channel is shown but same arrangement is provided on the Q channel.

Figure 10 Configuration of Error amplifier gain switching.

5.6 Instability Detector

The function of this section is to detect the increasing presence of out-of-band energy that occurs if the Cartesian Loop approaches a region of instability due to incorrect phase correction. To achieve this the Instability Detector is connected so as to look at the down-converter 'Q' signal provided by the buffered output IASIG.

The Instability Detector comprises a high pass filter and a detector (peak-hold) stage. The filter is to remove the lower frequencies, (i.e. modulation, present during stable operation). The detector (peak-hold) stage provides an analogue level indicating the presence of off-channel energy. The circuitry is designed to allow the simple construction of a 3rd order Sallen-Key filter. Figure 6 show how typical filters may be configured; Table 4 and Table 5 show some typical values. The filter can be optimised for a particular application based on signal bandwidth and loop bandwidth. The stop-band should reject the normal modulation while the pass-band should not attenuate off-channel energy caused by loop instability. For a

particular design the frequency offset where loop oscillation tends to occur first is at the edge of the loop bandwidth and this varies with loop gain and loop filter characteristics. The point can be identified empirically by adjusting the loop phase setting until the onset of instability is observed. This allows the high-pass filter to be designed appropriately.

There is a gain control stage and level shifter included as part of the detector circuit. This allows the user to select one of four gain settings prior to the detection (see Auxiliary Control Register); it also shifts the region of operation so that the detector output is a nominal $VD_{ref}/2$ for no signal and has a maximum limited value of VD_{ref}. (Note: VD_{ref} is the maximum output and the signal at pin PDO will not necessarily attain VD_{ref}, the level depends on the nature of the off-channel energy; an instability threshold should be determined based on the characteristics of a particular implementation.)

VD_{ref} is a supply that allows the output of the detector to be conveniently connected to the input of an A-D converter operating from a supply that may be different from that of this device. An example would be connection of this circuit to an auxiliary A-D input on the CMX981, which operates from 2.5V; by supplying the 2.5V as the supply VD_{ref}, this would allow the A-D converter to operate so that 1.25V would represent zero signal and give a reasonable dynamic range of operation with a maximum output of close to 2.5V. VD_{ref} must be in the range 2.1V to AV_{DD}+ 0.3V (but not greater than 3.6V).

The examples in Figure 6 have a peak hold capacitor of 47nF and a discharge resistor of 470k. These values may be changed to suit the requirements. A larger capacitor will hold longer at the expense of having a slower attack time; a larger resistor will also give a longer hold time (without affecting attack time). The above example gives attack times (to 90% of final value) in about 100µs and decay to 10% in about 7ms.

5.7 Reference Voltages

The IC includes on-chip reference voltage generation. A pin is provided to allow decoupling of noise. A buffered version of the reference is also provided on a pin. After filtering to remove noise, this may be used to provide dc reference for modulator mixer inputs. Decoupling of the VREF pin is recommended, the rise time of the reference voltage is proportional to the capacitance used, see Figure 11.

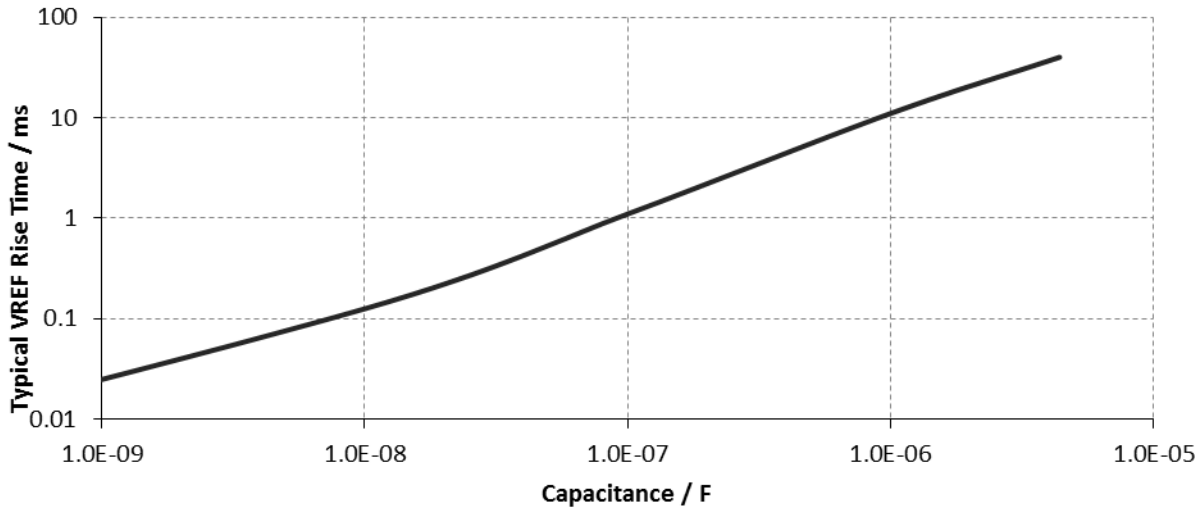


Figure 11 – Typical Rise Time of Reference Voltage

5.8 RF Power Detector

An RF envelope detector is provided in the down converter. The input to the detector is taken between the attenuator block and the down-converter mixers.

Note: The input signal to the detector will vary as the gain control in the feedback path is split between baseband and RF as shown in Figure 12. This results in the detector output increasing as the attenuation increases in 1dB steps (and therefore as the output power from the PA increases), but then returning to its first value on every 5th step increase.

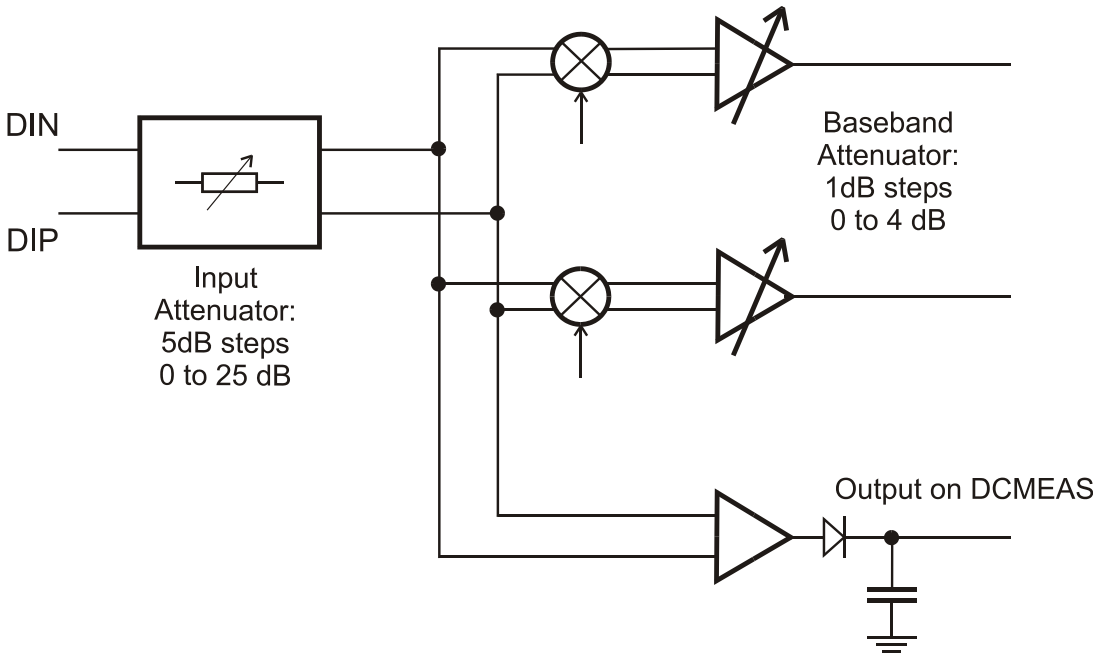


Figure 12 Downconverter Attenuation Configuration and RF Detector

Note: The detector responds to peak envelope rather than average level and has a detection bandwidth greater than 100kHz (response to amplitude modulation). This may be restricted by external capacitance after the DCMEAS output.

5.9 Operation over 30MHz to 100MHz

The operating frequency range of the CMX998 is 100MHz to 1GHz however the IC may also be used over the Extended Frequency Range 30MHz to 100MHz. Although the device will be functional over the 'extended' range, the performance parameters specified in section 7.1.3 are not guaranteed.

Some specific issues that users should be aware of are:

- Feedback path intermodulation will degrade significantly, with greater degradation as the frequency decreases.
- Feedback path intermodulation degradation is worse at higher values of the feedback path attenuator (when the input level is adjusted to give a constant output level).
- Phase shifter accuracy degrades significantly, especially for operation below 50MHz. Individual phase shift steps at 30MHz can be as low as 0 degrees and as high as 30 degrees (compared to the nominal step of 11.25 degrees), see Figure 13.

- I/Q amplitude and phase balance degrades as frequency reduces and will vary with phase shift setting.
- Forward path noise degrades at lower frequencies; a typical figure at 40MHz is –146dBc/Hz at a 5MHz offset.
- LO divide by 4 mode is not recommended for output frequencies below 50MHz.

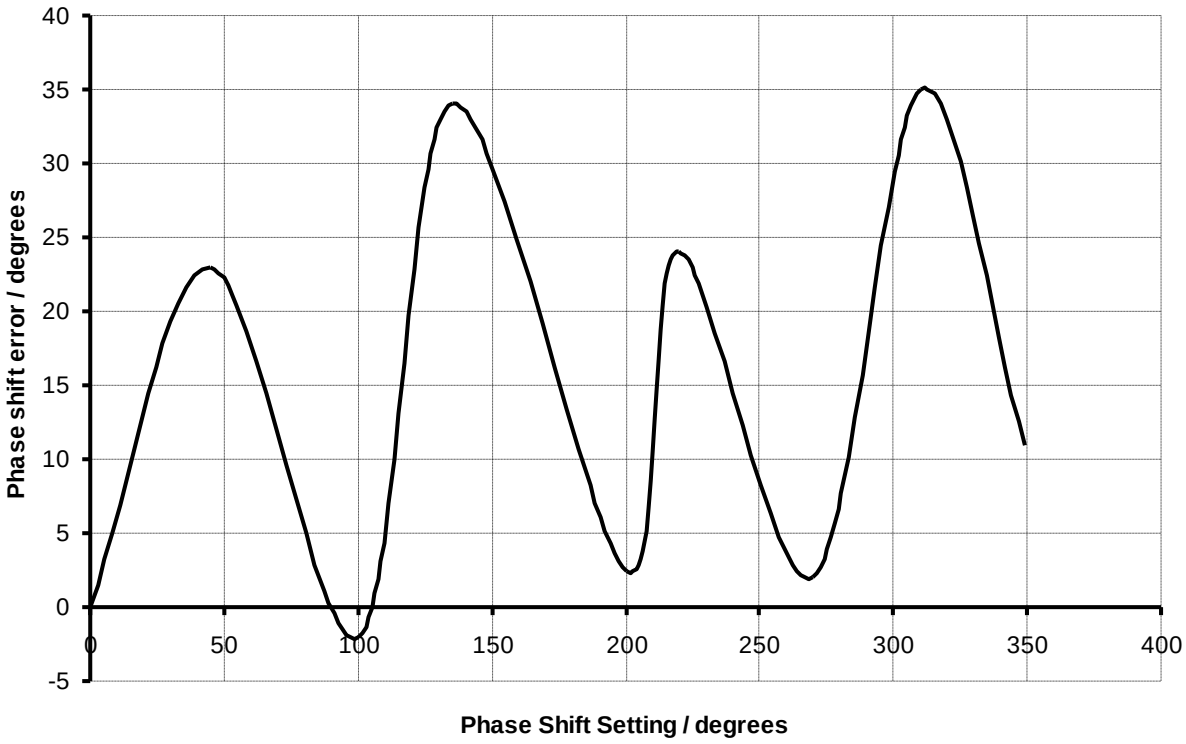


Figure 13 Typical variation in errors in phase shifter steps at 30MHz

The user should also be aware of the following helpful characteristics:

- Feedback path gain does not change significantly over the Extended Frequency Range.
- The phase shift errors generally follow a consistent pattern between devices, see Figure 13.

6 C-BUS Interface and Register Description

This block provides for the transfer of data and control or status information between the CMX998 internal registers and the µC over the C-BUS serial bus. Each transaction consists of a single Register Address byte sent from the µC which may be followed by one or more data bytes sent from the µC to be written into one of the CMX998's registers, as illustrated in Figure 14.

Data sent from the µC on the Command Data line is clocked into the CMX998 on the rising edge of the Serial Clock input. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine. Figure 14 gives detailed C-BUS timing requirements.

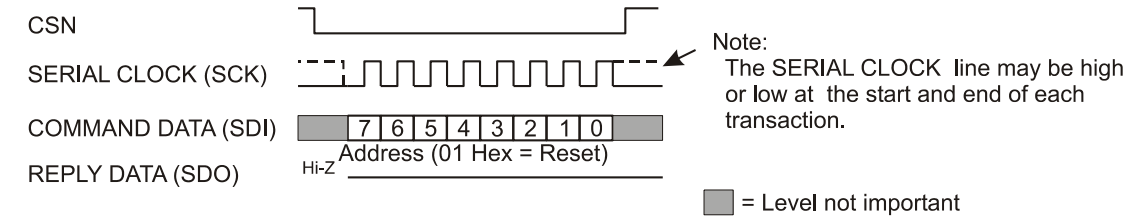
The following C-BUS addresses and registers are:

General Reset Register (Address only, no data)	Address $01
General Command, 8-bit write only.	Address $02
Phase Control Register, 8-bit write only.	Address $03
Gain Control, 16-bit write only .	Address $04
Forward Path Gain Control, 8-bit write only.	Address $05
Feedback Path Gain Control, 8-bit write only.	Address $06
Aux Control, 8-bit write only	Address $07
Frequency Control Register, 8-bit write only	Address $08
General Command, 8-bit read only.	Address $F2
Phase Control Register, 8-bit read only.	Address $F3
Gain Control, 16-bit read only .	Address $F4
Forward Path Gain Control, 8-bit read only.	Address $F5
Feedback Path Gain Control, 8-bit read only.	Address $F6
Aux Control, 8-bit read only	Address $F7
Frequency Control Register 8-bit read only	Address $F8

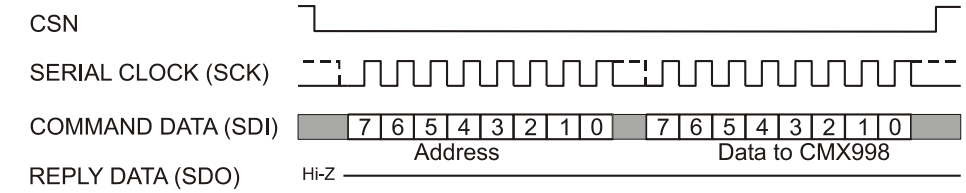
Notes:

- All registers will retain data if DV_{DD} and VD_{IO} are held high, even if all other power supply pins are disconnected.
- If clock and data lines are shared with other devices DV_{DD} and VD_{IO} must be maintained in their normal operating ranges otherwise ESD protection diodes may cause a problem with loading signals connected to SCK, SDO and SDI pins, preventing correct programming of other devices. Other supplies may be turned off and all circuits on the IC may be powered down without causing this problem.

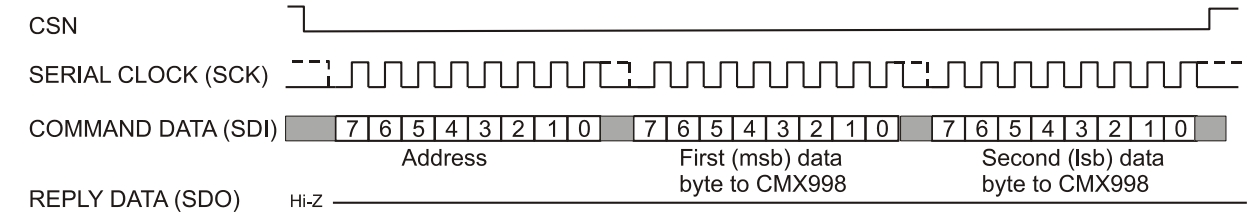
a) Single byte from µC (General Reset command)



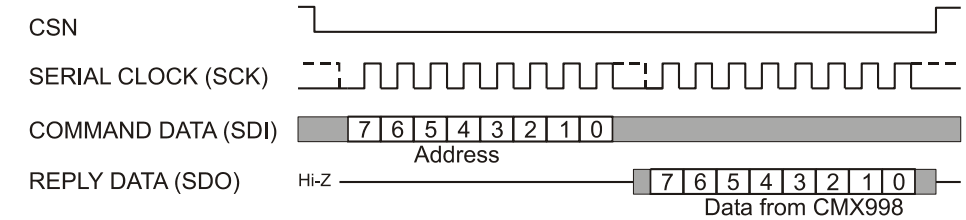
b) One Address and one Data byte from µC to CMX998



c) One Address and 2 Data bytes from µC to CMX998



d) One Address byte from µC and one Reply byte from CMX998



e) One Address byte from µC and 2 Reply bytes from CMX998

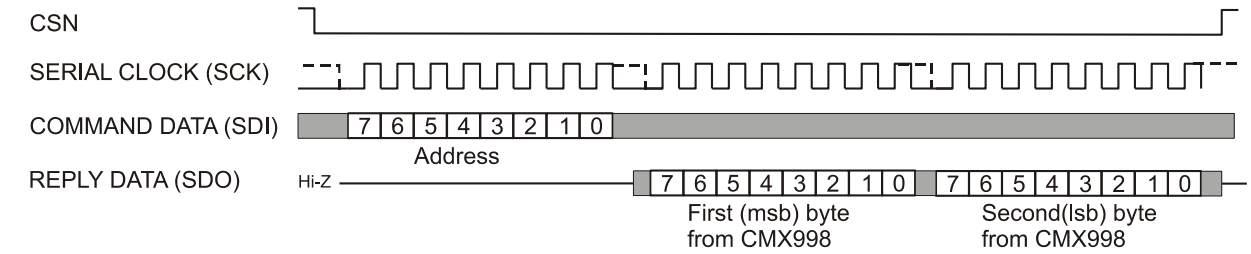


Figure 14 C-BUS Transactions

6.1 General Reset Command

6.1.1 General Reset Command C-BUS address $01 (no data)

This command resets the device and clears all bits of all registers. The General Reset command places the device into Power save mode.

Whenever power is applied to the DV_{DD} pin, a built in power-on-reset circuit ensures that the device powers up into the same state as follows a General Reset command. The RESET pin on the device will also reset the device to the same state.

6.2 General Control Register

6.2.1 General Control Register: C-BUS address $02 8-bit write-only

This register controls general features such as Powersave.
All bits of this register are cleared to 0 by a General Reset command.

Bit:	7	6	5	4	3	2	1	0
	Fwd Pwr	FB Pwr	V_{REF}	Filt Pwr	InputAmp Pwr	Error Amp Pwr	Open loop	Error Amp Gain Red.

General Control Register b7-b2: Select high input gain
These bits control power up/power down of the various blocks of the IC. In all cases '1' = power up, '0' = power down.

b7	Enable forward path and common local oscillator sections
b6	Enable feed-back path, phase shifter and common local oscillator sections
b5	Enable internal bias circuits and bandgap reference (V_{REF} and BV_{REF}).
b4	Enable filter amplifiers
b3	Enable input amplifier
b2	Enable error amplifiers

Note: Local oscillator blocks which are common between forward and feed-back paths are enabled by either b7 or b6 being set to '1'.

General Control Register b1: Open loop mode

b1 = 1	Open loop mode enabled
b1 = 0	Loop closed (Normal Operation)

General Control Register b0: Error Amplifier Gain Reduction

b0 = 1	Error amplifier gain reduction by adding 1kΩ between output and negative input.
b0 = 0	Normal Operation

6.2.2 General Control Register C-BUS address $F2
8-bit read-only

This register allows the current settings of register $02 to be read, see section 6.2.1 for details of bit functions.

6.3 Phase Control Register

6.3.1 Phase Control Register: C-BUS address $03
8-bit write-only

This register controls the loop phase shifters.
All bits of this register are cleared to 0 by a General Reset command.

Bit:	7	6	5	4	3	2	1	0
	Phase 1	Phase 2	Phase 3	Phase 4	Phase 5	Reserved	Reserved	Reserved

Phase Control Register b7-3: Phase Shift Setting

b7	b6	b5	b4	b3	
1	1	1	1	1	348.75 degrees
1	1	1	1	0	337.5 degrees
1	1	1	0	1	Other states follow binary count with steps of 11.25 degrees.
0	0	0	1	1	
0	0	0	1	0	22.5 degrees
0	0	0	0	1	11.25 degrees
0	0	0	0	0	0 degrees

Phase Control Register b2-0: Reserved for future use, set to '0'.

6.3.2 Phase Control Register: C-BUS address $F3
8-bit read-only

This register allows the current settings of register $03 to be read, see section 6.3.1 for details of bit functions.

6.4 Gain Control Register

6.4.1 Gain Control Register: C-BUS address $04
16-bit write-only

This register controls forward and feedback path gain.
All bits of this register are cleared to 0 by a General Reset .

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	F5	F4	F3	F2	F1	0	0	0	0	R7	R6	R5	R4	R3	R2	R1

Gain Control Register b10-7: Reserved for future use, set to '0'.

Gain Control Register b15-11: Forward Path Attenuation

b14	b13	b12	b11	
1	1	0	0	30dB Attenuation
1	0	1	1	27.5dB Attenuation
1	0	1	0	25dB Attenuation
1	0	0	1	22.5dB Attenuation
1	0	0	0	20dB Attenuation
0	1	1	1	17.5dB Attenuation
0	1	1	0	15dB Attenuation
0	1	0	1	12.5dB Attenuation
0	1	0	0	10dB Attenuation
0	0	1	1	7.5dB Attenuation
0	0	1	0	5dB Attenuation
0	0	0	1	2.5dB Attenuation
0	0	0	0	0dB Attenuation (Max Gain)

Gain Control Register b15: Reserved for Forward Path Attenuation, set to '0'.

Gain Control Register b5-b1: Feedback Path Attenuation

b5	b4	b3	b2	b1	
1	1	1	0	1	0dB Attenuation
1	1	1	0	0	1dB Attenuation
					Other states follow binary count with steps of 1dB
0	1	0	1	1	
0	1	0	1	0	19dB Attenuation
0	1	0	0	1	20dB Attenuation
0	1	0	0	0	21dB Attenuation
0	0	1	1	1	22dB Attenuation
0	0	1	1	0	23dB Attenuation
0	0	1	0	1	24dB Attenuation
0	0	1	0	0	25dB Attenuation
0	0	0	1	1	26dB Attenuation
0	0	0	1	0	27dB Attenuation
0	0	0	0	1	28dB Attenuation
0	0	0	0	0	29dB Attenuation

Gain Control Register b6 and b0: Reserved for Feedback Path Attenuation, set to '0'.

6.4.2 Gain Control Register: C-BUS address $F4
16-bit read-only

This register allows the current settings of register $04 to be read, see section 6.4.1 for details of bit functions.

6.5 Forward Path Gain Control Register

6.5.1 Forward Path Gain Control Register: C-BUS address $05
8-bit write-only

This register controls forward path gain. The same functions can be accessed from register $04.

Bit:	7	6	5	4	3	2	1	0
	F5	F4	F3	F2	F1	0	0	0

For functionality see section 6.4.1. Addressing this register is identical to addressing the most significant 8 bits of register $04. It is the same physical register.

Forward Path Gain Control Register b2-0: Reserved for future use, set to '0'.

6.5.2 Forward Path Gain Control Register: C-BUS address $F5
8-bit read-only

This register allows the current settings of register $05 to be read, see sections 6.4.1 and 6.5.1 for details of bit functions.

6.6 Feedback Path Gain Control Register

6.6.1 Feedback Path Gain Control Register: C-BUS address $06
8-bit write-only

This register controls feedback path gain. The same functions can be accessed from register $04.

Bit:	7	6	5	4	3	2	1	0
	0	R7	R6	R5	R4	R3	R2	R1

For functionality see section 6.4.1. Addressing this register is identical to addressing the least significant 8 bits of register $04. It is the same physical register.

Feedback Path Gain Control Register b7: Reserved for future use, set to '0'.

6.6.2 Feedback Path Gain Control Register: C-BUS address $F6
8-bit read-only

This register allows the current settings of register $06 to be read, see sections 6.4.1 and 6.6.1 for details of bit functions.

6.7 Aux Control Register

6.7.1 Aux Control Register: C-BUS address $07 8-bit write-only

Bit:	7	6	5	4	3	2	1	0
	DC On	Instab Det Enable	RFDet On	DCMEAS	IS1	IS2	DC1	DC0

Aux Control Register b7: DC On

Writing ‘b7’ = 1 will power up dc offset measuring circuits, writing ‘b7’ = 0 will place these circuits in zero power mode.

Aux Control Register b6: Instability Detector Enable

Writing ‘b6’ = 1 will power up instability detector circuits, writing ‘b6’ = 0 will place these circuits in zero power mode.

Aux Control Register b5: RFDet On

Writing ‘b5’ = 1 will power up RF Detector circuits, writing ‘b5’ = 0 will place these circuits in zero-power mode.

Aux Control Register b4: DCMEAS

Writing ‘b4’ = 1 will connect the DCMEAS pin to the output of the RF Detector circuits, writing ‘b4’ = 0 will connect the DCMEAS pin to the dc offset measuring circuits.

Aux Control Register b3-b2

Controls the gain of the instability detector.

Bit:	b3	b2	
	0	0	6dB
	0	1	12dB
	1	0	18dB
	1	1	24dB

Aux Control Register b1-b0

Bit:	b1	b0	
	0	0	DCMEAS connected to differential amplifier (gain x4) with inputs connected to MODQN and MODQN
	0	1	DCMEAS connected to differential amplifier (gain x4) with inputs connected to MODIN and MODIN
	1	0	DCMEAS connected to differential amplifier (gain x4) with inputs connected to MODIP and MODIN
	1	1	DCMEAS connected to differential amplifier (gain x4) with inputs connected to MODQP and MODQN

6.7.2 Aux Control Register: C-BUS address $F7 8-bit read-only

This register allows the current settings of register $07 to be read, see section 6.7.1 for details of bit functions.

6.8 Frequency Control Registers

6.8.1 Frequency Control Register: C-BUS address $08 8-bit write-only

Bit:	7	6	5	4	3	2	1	0
	0	0	0	DIV	0	0	F2	F1

Frequency Control Register b7-5 and b3-2: Reserved for future use, set to '0'.

Frequency Control Register b4: Local Oscillator Divider Control

Writing ‘b4’ = 1 will enable divide the local oscillator by 4 mode, writing ‘b4’ = 0 will enable divide local oscillator by 2 mode.

Frequency Control Register b1-b0

Controls the operating frequency band of the feedback loop.

Bit:

b1	b0	
0	0	Operation below 500MHz
0	1	Operation above 500MHz
1	0	Reserved
1	1	Reserved
Note: Frequencies are the operating frequency of the loop, not the local oscillator input frequency.		

6.8.2 Frequency Control Register: C-BUS address $F8 8-bit read-only

This register allows the current settings of register $08 to be read, see section 6.8.1 for details of bit functions.

7 Performance Specification

7.1 Electrical Performance

For definition of voltage and reference signal see Table 2.

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (AV_{DD} - AV_{SS}) or (DV_{DD} - DV_{SS})	-0.3	+4.0	V
Voltage on any pin to AV_{SS} or DV_{SS}	-0.3	V_{DD} + 0.3	V
Voltage between AV_{SS} and DV_{SS}	-50	+50	mV
Current into or out of DV_{SS}, AV_{DD} or DV_{DD} pins	-75	+75	mA
Current into or out of AVss (exposed metal pad)	-200	+200	mA
Current into or out of any other pin	-30	+30	mA

Q1 Package	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at T_{AMB} = 25°C	-	3500	mW
... Derating (see Note below)	-	35	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

Note: Junction-to-ambient thermal resistance is dependent on board layout and mounting arrangements. The derating factor stated will be better than this with good connection between the device and a ground plane or heat sink.

7.1.2 Operating Limits

	Notes	Min.	Max.	Units
Supply (AV_{DD} – AV_{SS}) and (DV_{DD} – DV_{SS})		3.0	3.6	V
IO Supply (VD_{IO} – DV_{SS})		1.6	3.6	V
Output Reference Supply (VD_{ref})	§	2.1	AV_{DD} + 0.3	V
Operating Temperature (see Note above)		-40	+85	°C

§ Note: Also the Output Reference (VD_{ref}) voltage must not exceed 3.6V.

7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
V_{DD} = AV_{DD} = DV_{DD} = 3.0V to 3.6V; VD_{ref} = 2.1V to V_{DD}; VD_{IO} = 1.6V to V_{DD}; V_{SS} = AV_{SS} = DV_{SS}; T_{AMB} = +25ºC; operation over specified 'Operating Frequency Range'. Note: for operation over 'Extended Frequency Range' see section 5.9.

DC Parameters	Notes	Min.	Typ.	Max.	Units
Total Current Consumption					
Powersave Mode	1, 54	-	10	70	µA
(Band Gap V_{REF} only)		-	50	-	µA
(Operating)		-	135	165	mA
Current from VD_{IO}	2a	-	-	600	µA
Current from VD_{ref}	2b	-	1.4	2.0	mA
Logic "1" Input Level		70%	-	-	VD_{IO}
Logic '0' Input Level		-	-	30%	VD_{IO}
Logic Input Leakage Current (V_{in} = 0 to DV_{DD}),		-1.0	-	+1.0	µA
Output Logic '1' Level (I_{OH} = 0.6 mA)		80%	-	-	VD_{IO}
Output Logic '0' Level (I_{OL} = -1.0 mA)		-	-	+0.4	V
Power-up Time		-	-		
Reference Voltage	2c	-	1.1	500	µs
All blocks except Voltage Reference		-	-	10	
Reference Voltage (V_{REF}, BV_{REF})		1.45	1.6	1.75	V

Notes:
1. Power save mode includes after general reset with all analogue and digital supplies applied and also in the case with V_{DD} applied but with all analogue supplies disconnected (i.e. in this later scenario, power from V_{DD} will not exceed the specified value whatever the state of the registers).
2a. Assumes 30pF on each C-BUS interface line and an operating serial clock frequency of 5MHz.
2b. Current drawn from VD_{ref} when either the DC Bias Measurement or the RF Detector circuit are enabled.
2c. No capacitance on VREF pin, in practice decoupling is recommended and rise time is proportional to the capacitance applied, see section 5.7.

AC Parameters	Notes	Min.	Typ.	Max.	Units
Operating Frequency Range		100	-	1000	MHz
Extended Frequency Range		30	-	100	MHz
Local Oscillator Frequency Range	6, 6a	60	-	2000	MHz
Local Oscillator Input Impedance (Differential)		-	50	-	Ω
Local Oscillator Input Level					
200MHz < F < 2000 MHz	6b	-20	-	-10	dBm
80MHz < F < 200MHz	6a	-15	-	-10	dBm
60MHz < F < 80MHz	6a,6c	-10	-	-5	dBm
I/Q Input Level		-	-	2.2	Vp-p
I/Q Input Common Mode Voltage		1.3	1.55	1.7	V
Forward Path					
Forward Path Output Power (PEP)	7, 8, 8a	-	+3	-	dBm
Forward Path Wideband Noise	9, 10, 60, 36	-	-148	-145	dBc/Hz
Forward Path Noise Floor	16, 10a, 60				
Forward Path Attenuation = 5dB		-	-	-153	dBm/Hz
Forward Path Attenuation = 10dB		-	-	-155	dBm/Hz
Forward Path Attenuation = 15dB		-	-	-156	dBm/Hz
Forward Path Attenuation = 20dB		-	-	-158	dBm/Hz
Forward Path Attenuation = 25dB		-	-	-159	dBm/Hz
Forward Path Image Suppression		20	-	-	dB
Forward Path Intermodulation	14	30	35	-	dB
Forward Path Output Load Impedance (Differential)	56	-	200	-	Ω
Discrete unwanted emissions (other than harmonics of the output) in the frequency range 9kHz -12.75 GHz.	57, 60, 61	-	<-95	-80	dBc
Feedback Path					
Feedback Path Max Input Power (PEP)	8, 15	-22	-	+7	dBm
Feedback Path Input Impedance	4	-	50	-	Ω
Feedback Path Image Suppression	11	30	-	-	dB
Feedback Path Gain	18	-	24	-	dB(V/V)
Feedback Path Gain Variation with Temp.	60	-	±0.6	-	dB
Feedback Path Gain Absolute Error From Nominal Gain Setting		-	-	±2	dB
Feedback Path Noise Figure	5	-	21	22	dB
Feedback Path Gain Control Range		-	29	-	dB
Feedback Path Gain Control Step Size		-	1	-	dB
Gain Switching Time	3	-	-	10	µs
Feedback Path Bandwidth	12	10	50	-	MHz
Feedback Path Output Load	17	-	1	-	kΩ
Feedback Path Second Order Intermodulation	13,	65	-	-	dB
Feedback Path Third Order Intermodulation	13	65	-	-	dB
Feedback Path Fifth Order Intermodulation	13	75	-	-	dB

Feedback Path Phase Shift at 10MHz with 1 kΩ output load	19	-	-	50	deg
Feedback Path Open Loop Isolation		-	50	-	dB
Feedback Path DC Output (nominal)		V_{REF} - 0.15	V_{REF}	V_{REF} + 0.15	V

AC Parameters	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
Phase Shift					
Phase Shift Range		-	348.75	-	deg
Phase Shift Step Size		-	11.25	-	deg
Phase Shift Absolute Error		-	-	10	deg
Switching Time	3	-	-	10	µs

Notes:

3. Time from rising edge of the last (8th or 16th depending on whether 8 or 16 bit registers are used) serial clock input following CSN being asserted for a write to the appropriate control register.
4. The input to the chip is differential. Specified input impedance is measured using a 1:1 balun transformer.
5. Measured at 100kHz with minimum feedback path attenuation, Noise figure as measured in I or Q path.
6. Local oscillator input frequency is twice or four times the required operating frequency, selectable with DIV bit (see section 6.8.1).

6a. LO divide by 4 mode is not recommended for output frequencies below 50MHz.

6b. For operation with a modulator output above 600MHz optimum performance will typically be achieved with the LO input level in the range -15dBm to -20dBm.

6c. LO divide by 2 mode operation only

7. Output power reduced dB for dB with forward path attenuation.
8. Peak power: PEP measured with 2-tone signal (two equal amplitude tones).

8a. Gain and Output Power will reduce below 100MHz. Values are typically 4dB lower at 30MHz.

9. Measured between noise floor and mean power in TETRA π/4-DQPSK modulated wanted signal.
10. Measured at 400MHz, 5MHz offset over specified Forward Path Output Power range and with forward path attenuation between 0dB and –5dB, NB: typical noise performance is achieved at typical output power and above.

10a. Measured at 400MHz, 5MHz offset with specified Forward Path Output Power for the relevant attenuation level.

11. Combination of amplitude and phase balance of I/Q paths.
12. With specified typical output load impedance.
13. Two-tone test, intermodulation product level is measured relative to one of the wanted tones, specification is met for the following conditions:
    - minimum feedback path attenuation and minimum input signal level
    - maximum feedback path attenuation and maximum input signal level
    - All combinations of attenuation and signal level that achieve the same signal level at the output of the feedback path as in the above conditions
14. Two tone test, limit is met at all gain steps for 'Forward Path Output Power Level (PEP)' of: +6 dBm below 600 MHz, +3 dBm 600-900MHz, and 0 dBm above 900 MHz.
15. Specification for 'min.' valid at minimum attenuation and 'max.' at maximum attenuation.
16. Measured with modulated output signal at relevant output power for forward path attenuations, as specified.

17. Operating into a virtual earth (not ground).
18. Measured as peak-to-peak voltage from c.w. 50 ohm source at input to down converter path, single ended, before balun to peak-to-peak voltage at the output of I or Q paths (DOI, SOI, DOQ or SOQ pins), feedback path gain setting = 0dB attenuation.
19. Equivalent to 13.89ns delay.

DC Calibration	Notes	Min.	Typ.	Max.	Units
Differential Gain to DCMEAS pin	20	-	4	-	V/V
Vdco	22	-	$VD_{ref}/2$	-	V
Output Switching Time	21	-	-	2	µs

Notes: An application note on DC Calibration of the CMX998 is available at www.cmlmicro.com.

20. Gain of the differential amplifier described in section 5.5 and Figure 9. For detail of circuit control see section 6.7.1.
21. Time for output to change between measurement modes, measured from the rising edge of CSN.

I/Q Modulator	Notes	Min.	Typ.	Max.	Units
Minimum Input Bandwidth		-	50	-	MHz
Input Signal		-	0.5	-	Vp-p
DC Bias Input	22	-	1.6	-	V
Voltage Gain	23, 8a	-	-2	-	dB
Nominal Forward Path Gain Control Range	23a	-	30	-	dB
Forward Path Gain Control Step Size		1.0	2.5	4.0	dB
Gain Switching Time	3	-	-	10	µs
Other Parameters see 'AC Parameters' table					

Notes: 22. Normally connected to BVREF pin via an RC filter, the tolerance of BV_{REF} is specified in the DC Parameter table and these same tolerance limits apply here.
23. Voltage gain measured from the modulator input (MODIN or MODQN) to the output of a 4:1 balun (see section 4.2), using 7kHz sine / cosine waves on MODIN / MODQN.
23a Typical range 28.2 dB, standard deviation 0.3.

Error Amplifier	Notes	Min.	Typ.	Max.	Units
Supply Current (Enabled)		-	2.3	3.0	mA
Supply Current (Standby)	54	-	-	1	µA
Gain Bandwidth Product	25	-	65	-	MHz
Input Offset Voltage	35	-	3	4	mV
Input Common Mode Range	26	1.1	1.6	2.5	V
Input Bias Current		-	1.6	4.5	µA
Input Resistance		-	38	-	kΩ
Slew Rate	25	-	32	-	V/µs
Differential Input Voltage	27	-	-	1.2	V
Input Referred Noise Voltage	28	-	5	10	nV/√Hz
Intermodulation Products	24, 29a, 31	-	-90	-	dBc
Intermodulation Products	24, 29b, 31	-	-90	-	dBc
Output Voltage	24	AV_{SS} + 0.2	-	AV_{DD} – 0.8	V

Notes:
24. Typical loads are 150 ohms and 33nF in series or 150 ohms and 100nF in series.
25. With a load of 150 Ohms in series with 100 nF. (Note 17 also applies).
26 For small signal operation. It is recommended that for this application the input levels be restricted to +/-0.4V about a defined reference voltage of 1.6V (nominal); this will allow for some tolerance in components and for the precision of the reference voltage setting.
27 The inputs are protected with diodes. These diodes prevent the inadvertent application of voltages that may cause damage to the input transistors.
28 Measured at 10kHz.
29a Measured with respect to an output signal level of 0.4V pk-pk for each tone of a two-tone signal with 7kHz and 9kHz tones and with a load of 150 Ohms in series with 33nF. Amplifier configured as a voltage follower. (Note 17 also applies).
29b Also measured with the same conditions, but with 70kHz and 90kHz tones and with a load of 100 Ohms in series with 10nF. (Note 17 also applies).

Input Amplifiers and Filter Amplifiers	Notes	Min.	Typ.	Max.	Units
Supply Current (Enabled) per amplifier		-	0.7	0.9	mA
Supply Current (Standby) per amplifier	54	-	-	1	µA
Gain Bandwidth Product	30	-	10	-	MHz
Input Offset Voltage	35	-	3	4	mV
Input Common Mode Range	32	1.0	1.6	2.5	V
Input Bias Current		-	0.4	1	µA
Input Resistance		-	160	-	kΩ
Slew Rate	30	-	6	-	V/µs
IMD	30, 31, 34	-	-85	-	dB
Differential Input Voltage	33	-	-	1.2	V
Input Referred Noise at 1kHz		-	15	-	nV/√Hz
Output Load	17	-	1kΩ //100pF	-	
DC Output Range		AV_{ss}+0.1	-	AV_{DD}-0.1	V

Notes:
30. With a load of 1kΩ in parallel with 100pF. (Note 17 also applies).
31. Includes all IMD products up to and including the7 th order products e.g. 2nd, 3rd, 5th etc. Specification limit applies to each IMD product, not the composite power of all products.
32. For small signal operation. It is recommended that for this application the input levels be restricted to +/-0.4V about a defined reference voltage of 1.6V (nominal); this will allow for some tolerance in components and for the precision of the setting of the reference voltage.
33. The inputs are protected with diodes. These diodes prevent the inadvertent application of voltages that may cause damage to the input transistors.
34. Two-tone test with value measured relative to power in either tone, unity gain, 0.8V p-p signal, with two tones at 70kHz and 90kHz (400mV p-p each tone).
35. The maximum value is derived from analysis of statistical evaluation results and is not guaranteed by 100% testing.
36. A typical figure at 40MHz or 50 MHz is –146dBc/Hz at a 5MHz offset.

Instability Detector	Notes	Min.	Typ.	Max.	Units
Supply Current from VCC (Enabled)		-	1.6	-	mA
Supply Current from VDREF (Enabled)		-	120	-	µA
Supply Current from BVREF (Enabled)		-	50	-	µA
Supply Current (from all sources) (Standby)	54	-	-	1	µA
Ist stage (Filter amplifier)					
Gain (internally configured as voltage follower)		-	0	-	dB
All other characteristics (see section "Input Amplifiers and Filter Amplifiers)					
2nd Stage (Detector)	40				
Attack Time to 90%	44	-	100	-	µs
Input Offset Voltage		-20	-	+20	mV
Input Common Mode Range	41	1.1	1.6	2.1	V
Input Bias Current		-	10	-	nA
Input Resistance		-	100	-	MΩ
AC Gain	42, 44	-	6, 12, 18, 24	-	dB
Voltage out when no signal present		-	$VD_{ref}/2$	-	V
Maximum voltage out		-	VD_{ref}	-	V
Output Load	43	-	470kΩ //47nF	-	

Notes: 40. The function of the detector is to follow the maximum peaks of the input voltage waveform. The ability to do this is frequency dependent which, in turn, is dependent on the choice of external capacitor.

41. For small signal operation. It is recommended that for this application the input levels be restricted to +/-0.4V about a defined reference voltage of 1.6V (nominal); this will allow for some tolerance in components and for the precision of the setting of the reference voltage.

42. Amplifier gain configurable in 4 nominal steps.

43. The time constant of the peak detector can be controlled by a parallel resistor and capacitor on the output (Pin PDO). If a purely resistive load is used, the minimum resistor value is 10kΩ.

44. Measured at 1MHz. The attack time is dependant on external component values. This specified time is based on the use of typical configurations, shown in section 4.5.

RF Detector	Notes	Min.	Typ.	Max.	Units
Input Power Range	58	-	+10, -6	-	dB
Nominal Input Power (PEP)	51	-	-22	-	dBm
Scale	50	-	10	-	V/V p-p
Vdco	59	-	$VD_{ref}/2$	-	V
Frequency Range	52	30	-	1000	MHz
Output SINAD	53	30	-	-	dB
Output Bandwidth (3dB)		12	-	-	kHz
Output Load		-	100	-	kΩ

Notes:
50. With feedback path attenuator set to 0dB.
51. PEP Input level assuming TETRA π/4-DQPSK modulation or 2-tone signal.
52. Operation to 30MHz, but RF Detector performance parameters are not guaranteed between 30MHz and 300MHz.
53. Measured with 400MHz signal having 1kHz, 30% AM modulation at –15dBm input to the down-converter, 0dB feedback path attenuation, 300Hz to 3.4kHz measurement bandwidth.
54. At Tamb = 25ºC, not including any current drawn from the CMX998 pins by external circuitry.
55. Void.
56. This is the impedance that should be presented to the output of the CMX998 up-converter, e.g. using a balun, as shown in Figure 3. The precise load impedance may be optimised for a given operating frequency, or band of frequencies, to achieve improved output level and signal-to-noise.
57. With a spurious-free LO input and specified output level.
58. The typical input power range is –12dBm PEP (i.e. *–22dBm* + *10dB*) to –28dBm PEP (i.e. –22dBm – *6dB*).
59. Vdco is the nominal voltage that would be measured at the detector output with no RF input applied.
60. Full Operating Temperature range (see section 7.1.2)
61. Discrete Spurious typically below detectable levels

C-BUS Timings (See Figure 15)		Notes	Min.	Typ.	Max.	Units
t_{CSE}	CSN-Enable to Clock-High time		100	-	-	ns
t_{CSH}	Last Clock-High to CSN-High time		100	-	-	ns
t_{LOZ}	Clock-Low to Reply Output enable time		0.0	-	-	ns
t_{HIZ}	CSN-High to Reply Output 3-state time		-	-	1.0	µs
t_{CSOFF}	CSN-High Time between transactions		1.0	-	-	µs
t_{NXT}	Inter-Byte Time		200	-	-	ns
t_{CK}	Clock-Cycle time		200	-	-	ns
t_{CH}	Serial Clock (SCK) - High time		100	-	-	ns
t_{CL}	Serial Clock (SCK) - Low time		100	-	-	ns
t_{CDS}	Command Data (SDI) - Set-Up time		75.0	-	-	ns
t_{CDH}	Command Data (SDI) - Hold time		25.0	-	-	ns
t_{RDS}	Reply Data (SDO) - Set-Up time		50.0	-	-	ns
t_{RDH}	Reply Data (SDO) - Hold time		0.0	-	-	ns

Maximum 30pF load on each C-BUS interface line.

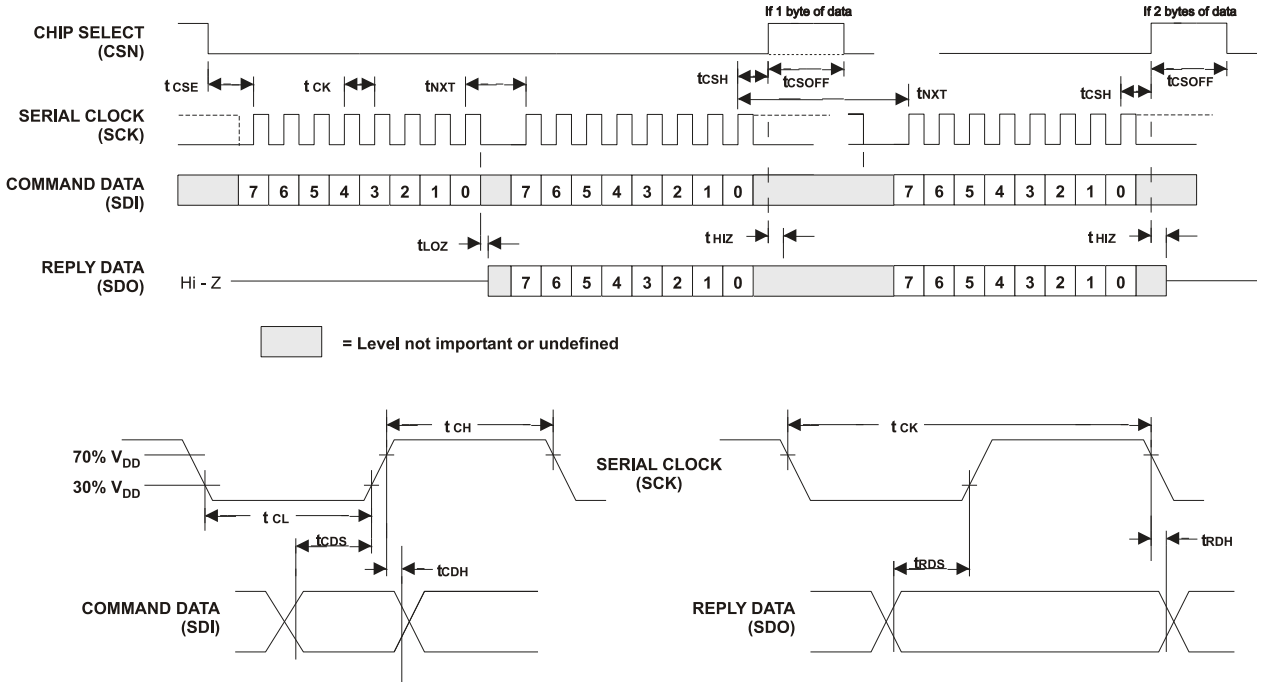
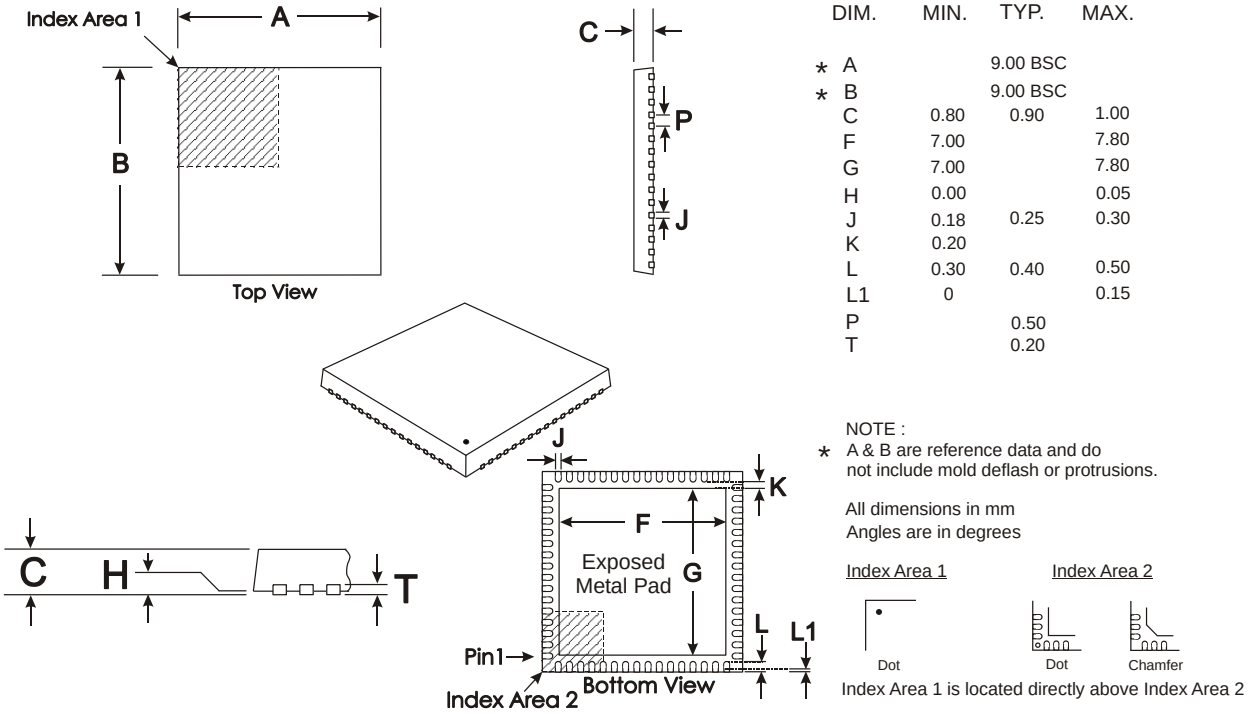


Figure 15 C-BUS Timing

7.2 Packaging



	DIM.	MIN.	TYP.	MAX.
*	A		9.00 BSC	
*	B		9.00 BSC	
	C	0.80	0.90	1.00
	F	7.00		7.80
	G	7.00		7.80
	H	0.00		0.05
	J	0.18	0.25	0.30
	K	0.20		
	L	0.30	0.40	0.50
	L1	0		0.15
	P		0.50	
	T		0.20	

NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Note:

In this device, the underside of the Q1 package must be electrically connected to the analogue ground. The circuit board should be designed so that no unwanted short circuits can occur.

Figure 16 Q1 Mechanical Outline: *Order as part no.* CMX998*Q1*

Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.

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