(SP4T) SWITCH, 0.1 GHz to 44 GHz

Model: LF-SP4T-44-LGA

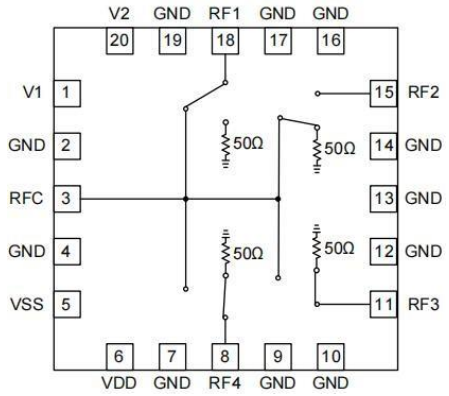
PRODUCT OVERVIEW:

The **LF-SP4T-44-LGA** is a wideband, high isolation, low insertion loss, absorptive, four-throw (SP4T) switch, it operates from 0.1 GHz to 44 GHz (10kHz is available) with an insertion loss of lower than 3.0 dB and isolation of around 39 dB. The **LF-SP4T-44-LGA** comes in a 20-terminal, 3 mm x 3 mm, RoHS-compliant, land grid array (LGA) package.

KEY FEATURES:

- Ultrawide Band: 0.1-44GHz (10kHz is available)
- Insertion Loss:
  1.6dB@100MHz-18GHz
  2.1dB@18GHz-26GHz
  3.0dB@26GHz-44GHz
- Isolation:
  59dB@100MHz-18GHz
  50dB@18GHz-26GHz
  39dB@26GHz-44GHz
- Compliant 20-terminal,3x3 mm LGA package

FUNCTIONAL BLOCK DIAGRAM:



ELECTRICAL SPECIFICATIONS: (TA=+25℃, Vdd=3.3V, Vss=-3.3V, v1=v2=0/3.3v):

Parameter		Min	Typ	Max	Units
Frequency range			0.1-44		GHz
Insertion Loss	100MHz-18GHz		1.6		dB
	18GHz-26GHz		2.1		
	26GHz-44GHz		3		
Isolation	100MHz-18GHz		59		dBm
	18GHz-26GHz		50		
	26GHz-44GHz		39		
Input Return Loss			-16		dB
Output Return Loss	Isolation state		-15		dB
	Insertion loss state		-14		
Input P1dB			24.5		dBm
Input IP3			38		dBm
VDD		3		5	V
IDD			0.5		mA
VSS		-3.6		-3	V

ELECTRICAL SPECIFICATIONS: (TA=+25℃, Vdd=3.3V, Vss=-3.3V, v1=v2=0/3.3v):

Parameter		Min	Typ	Max	Units
V1、V2	Low	0		0.3	V
	High	3		3.6	
	Lin		15		μA
Rise/Fall Time	10% to 90% RF output		0.4		μs
Switch Time	50% VCTRL to 10%/90% RF output		1.5		μs
Input Power	Insertion loss state			25	dBm
	Isolation state			24	
Phase Consistency			2		°
Amplitude Consistency			0.1		dB

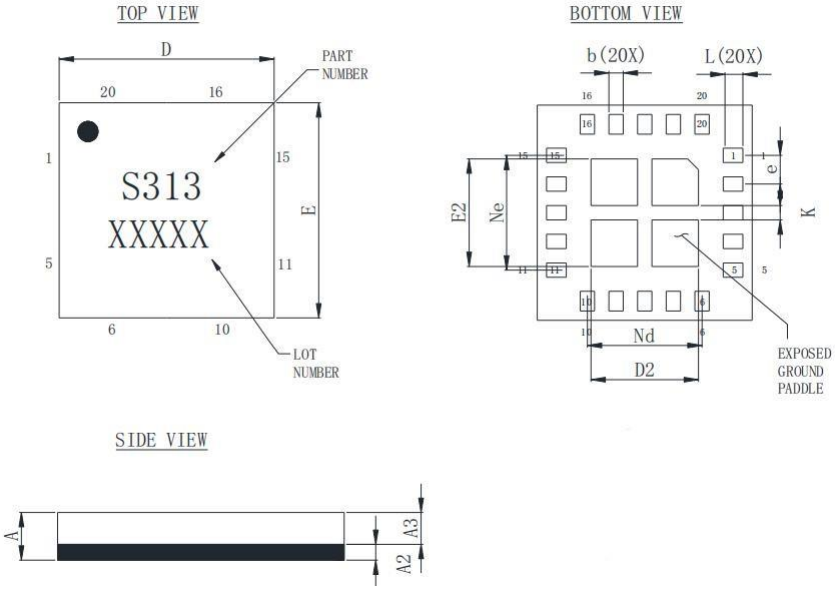
Note:

1. The minimum frequency of the test instrument is 10KHz, so only the test data above 10KHz is displayed.
2. There is no integrated DC/DC conversion module inside the chip, so the positive/negativepower supply (VDD/VSS) of the chip must be turned on, and the range of VSS is -3.6~-3.0 (V).

ABSOLUTE MAXIMUM RATINGS:

Parameter	Value
Input Power (Insertion loss state)	25.5 dBm
Input Power (Isolation state)	25 dBm
VDD	-0.3-5.6V
V1、V2	-0.5-3.6V
T jmax	135℃
R jc	110℃/W
Operating Temperature	-40℃～+85℃
Non-operating Temperature	-65℃～+150℃
ESD(HBM)	Class 1B V
ESD(CDM)	Class C3 V

OUTLINE AND PORT SIZE: Unit mm



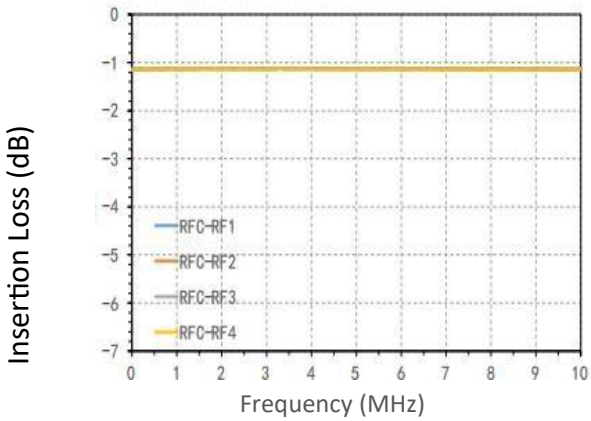
SL3-2 Dimension Table (unit: mm)			
Symbol	Min	Nom	Max
A	0.565	0.665	0.765
A2	0.19	0.22	0.25
A3		0.445	
b	0.15	0.2	0.25
D	2.9	3	3.1
D2	1.4	1.5	1.6
e		0.40BSC	
Ne		1.60BSC	
Nd		1.60BSC	
E	2.9	3	3.1
E2	1.4	1.5	1.6
K	0.5	0.6	0.7
L	0.2	0.25	0.3

Truth Table		
TTL Control Input		**Signal Path State**
Low	Low	RFC-RF1
High	Low	RFC-RF2
Low	High	RFC-RF3
High	High	RFC-RF4

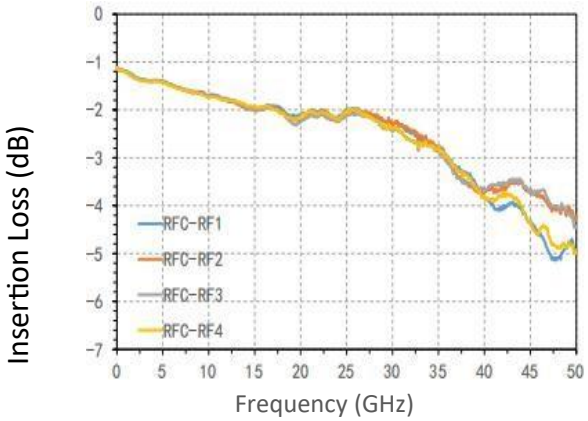
TYPICAL PERFORMANCE DATA:

Test Curves: (TA=+25℃, Vdd=+3.3V, Vgg=-3.3V, v1=v2=0/3.3v)

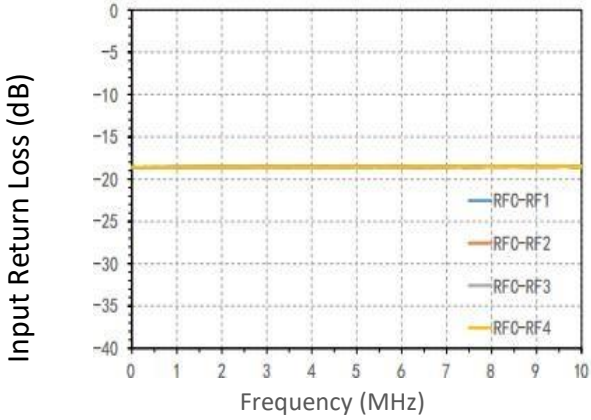
Insertion Loss vs Frequency



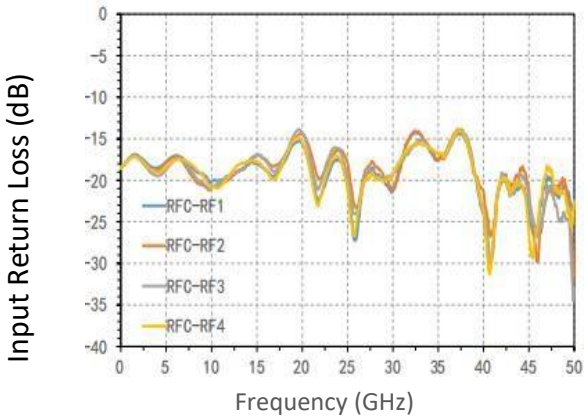
Insertion Loss vs Frequency



Input Return Loss vs Frequency

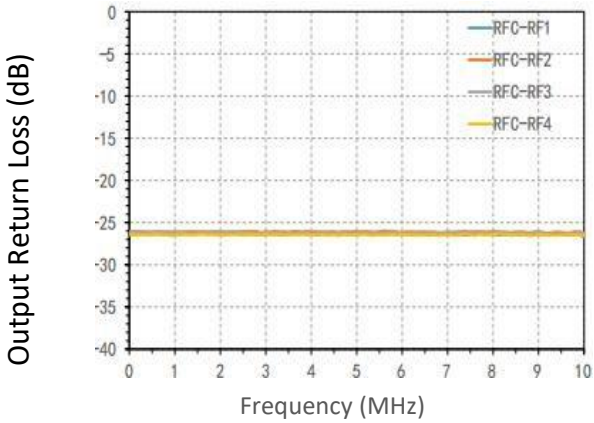


Input Return Loss vs Frequency

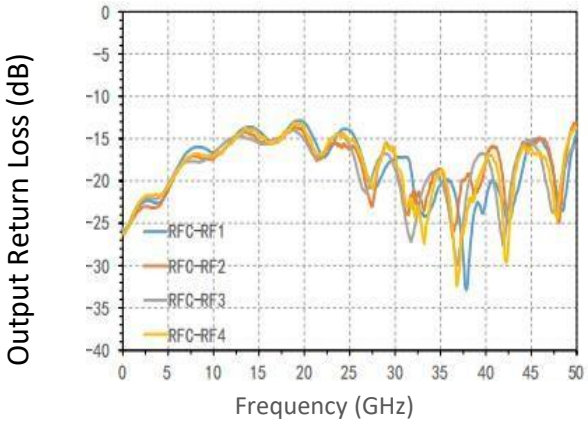


Isolation state

Output Return Loss vs Frequency



Output Return Loss vs Frequency



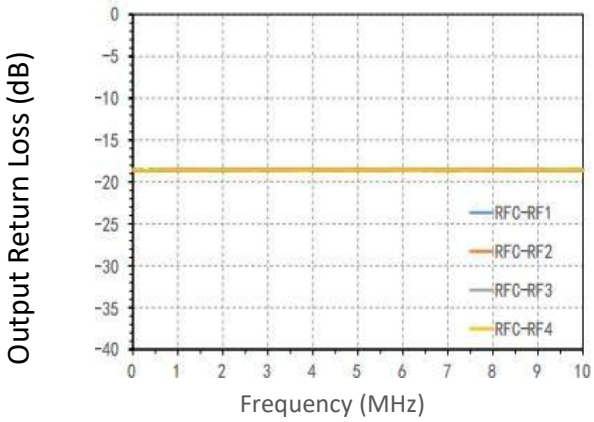
Note: Above data is for ref only, actual data may vary from unit to unit depending on operating environmentand other factors like material lots etc.

TYPICAL PERFORMANCE DATA:

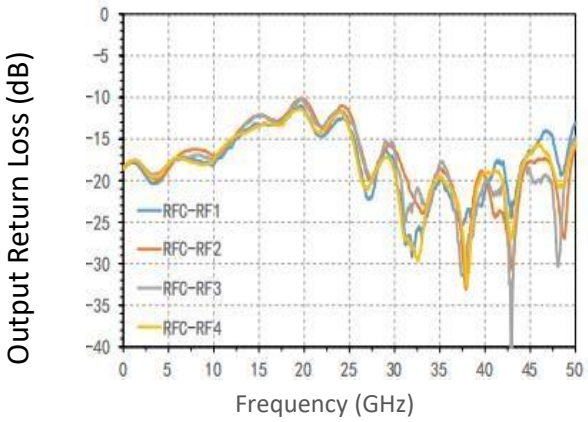
Test Curves: (TA=+25℃, Vdd=3.3V, Vgg=-3.3V, v1=v2=0/3.3v)

Insertion loss state

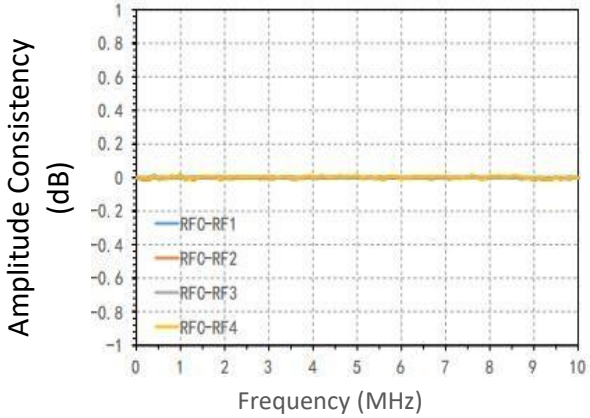
Output Return Loss vs Frequency



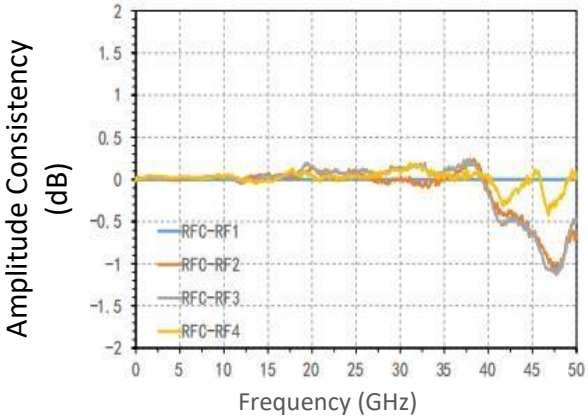
Output Return Loss vs Frequency



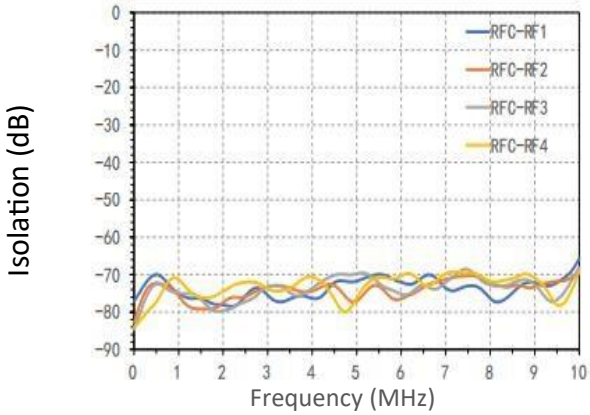
Amplitude Consistency vs Frequency



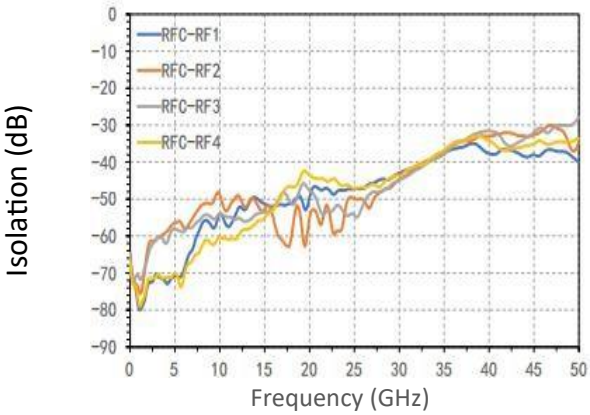
Amplitude Consistency vs Frequency



Isolation vs Frequency



Isolation vs Frequency



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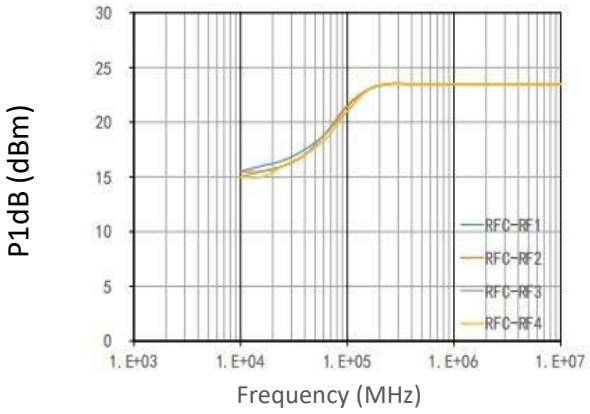
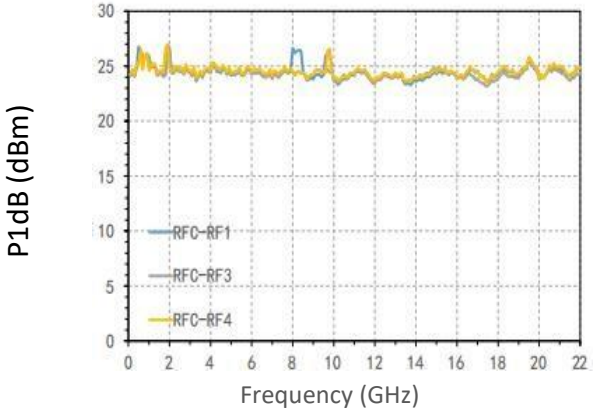
TYPICAL PERFORMANCE DATA:

Test Curves: (TA=+25℃, Vdd=3.3V, Vgg=-3.3V, v1=v2=0/3.3v)

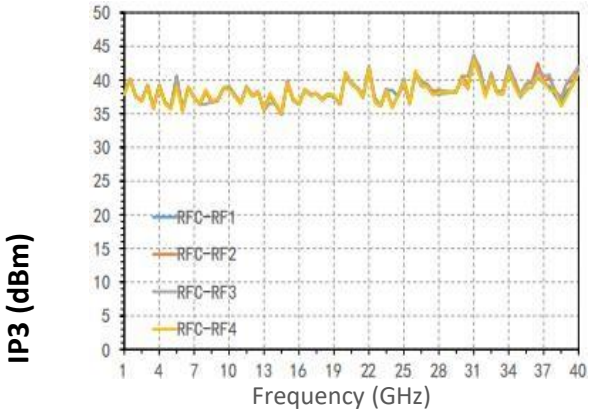
P1dB vs Frequency



P1dB vs Frequency



IP3 vs Frequency



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APPLICATION INFORMATION:

1. Storage: The chip must be placed in a container with electrostatic protection function andstored in nitrogen environment.
2. Cleaning: The bare chip must be operated and used in a purified environment. It is forbidden touse liquid detergent to clean the chip.
3. Electrostatic protection: Please strictly comply with ESD protection requirements to avoidelectrostatic damage.
4. Routine operation: Please use vacuum chuck or precision pointed tweezers to take the chip.Avoid touching the chip surface with tools or fingers during operation.
5. Power on sequence: when power on, apply gate voltage first and then Drain voltage; When de energizing, remove the Drain voltage first and then the gate voltage.
6. Mounting operation: The chip can be installed by AuSn solder eutectic sintering or conductive adhesive bonding process. The installation surface must be clean and flat, and the gap between the chip and the input / output RF connecting line substrate shall be as small as possible.
7. Sintering process: 80 / 20 AuSn shall be used for sintering. The sintering temperature shall not exceed 300 ℃, the sintering time shall be as short as possible, not more than 20 seconds, and the friction time shall not exceed 3 seconds.
8. Bonding process: The dispensing amount of conductive adhesive shall be minimized during bonding, and the curing conditions shall refer to the data provided by the conductive adhesive manufacturer.
9. Bonding operation: Unless otherwise specified, two bonding wires (diameter 25um gold wire) are used for RF input and output, and the bonding wire shall be as short as possible. The thermal ultrasonic bonding temperature is 150 ℃, and the ultrasonic energy is as small as possible. The pressure of spherical bonding cleaver is 40 ~ 50gf, and the pressure of wedge bondingcleaver is 18 ~ 22gf.
10. If you have any questions, please contact the supplier.