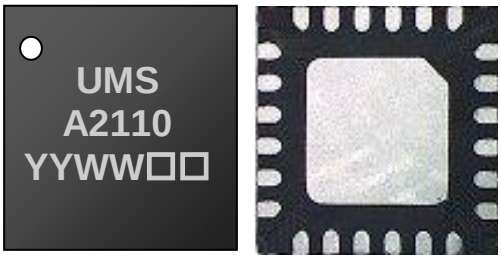
CHA2110-QDG

7-12 GHz LNA

GaAs Monolithic Microwave IC in SMD leadless package

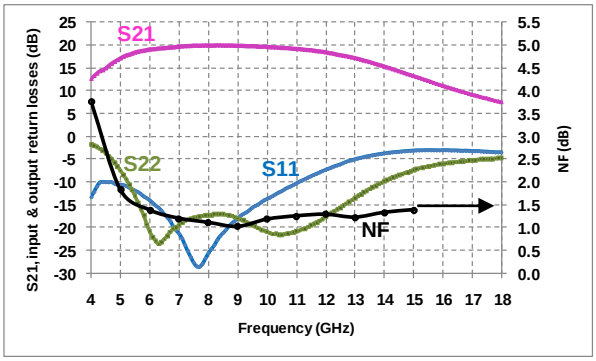
Description

The CHA2110-QDG is a monolithic two-stage wide band, self-biased Low Noise Amplifier.
It is designed for a wide range of applications, from military to commercial communication systems.
The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, and air bridges.
It is supplied in RoHS compliant SMD package.



Main Features

- Broadband performances: 7-12GHz
- Linear gain: 19dB
- Noise Figure: 1.2dB
- Output power @ 1dB comp.: 10dBm
- DC bias: Vd=4V @ Id=45mA
- 24L-QFN4x4
- MSL1



Typical gain, input return losses, output return losses and Noise Figure (dB) versus frequency

Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	7		12	GHz
Gain	Linear Gain		19		dB
NF	Noise Figure		1.2		dB
Pout	Output Power @1dB comp. (Freq.=10GHz)		10		dBm

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Electrical Characteristics

Tamb.= +25°C, Vd = +4V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	7		12	GHz
Gain	Linear Gain	18 (7-10.5GHz) 16.5 (10.5-12GHz)	19	21	dB
NF	Noise Figure		1.2	1.5	dB
RL_in	Input return losses		-12	-5	dB
RL_out	Output return losses		-15	-12	dB
P1dB	Output power at 1dB comp (f=10GHz)	8.5	10	11.5	dBm
IP3	3rd order interception point (f=10GHz)		21		dBm
Vd	Drain supply voltage (self biased)		4		V
Id	Drain supply current		45	55	mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Max Pin ON	No damage maximum input power	15	dBm
Max Pin OFF	No damage maximum input power (Vd=0V)	18	dBm
Max Pin for 1 hour	No damage maximum input power for 1 hour duration	20	dBm
Vd	Drain bias voltage	5V	V
Id	Drain bias current	70	mA
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C; pads 1A, 1B, 2A and 2B are non-connected

Symbol	Pad N°	Parameter	Values	Unit
Vd	VD1,VD2	Drain supply voltage	4	V

The circuit is self-biased.

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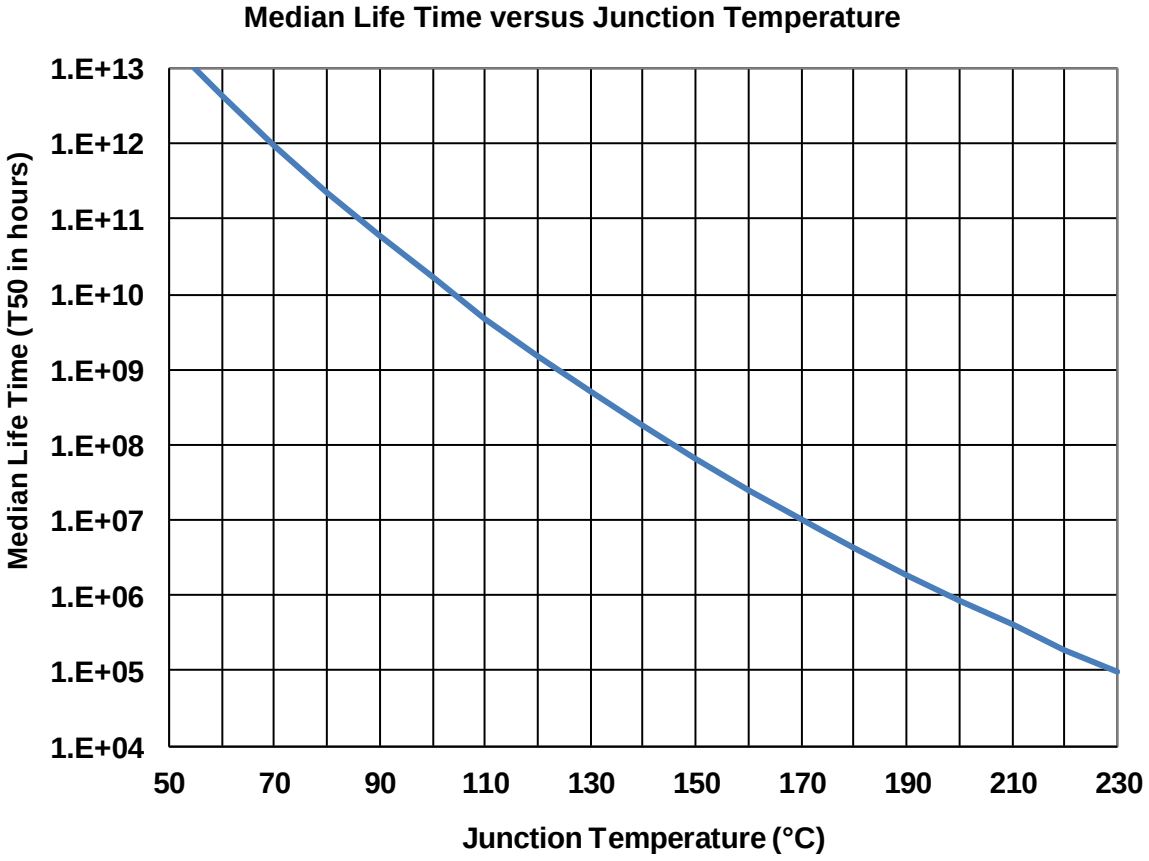
Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tb) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below the maximum value specified in the next table. So, the PCB system must be designed to comply with this requirement.

The thermal performances of the device given below are based on UMS rules to evaluate the junction temperature.
This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHA2110-QDG is fabricated (AsGa Power PHEMT 0.25µm).
The thermal resistance (Rth_eq) is given for the full circuit and assumes CW operation mode as given in the table.

Parameters	Symbol	Conditions	Value	Unit
Thermal Resistance	Rth_eq	**Tb=85°C**, Vd=4V, Id_drive=0.041A Pin=-20dBm Pout=-2dBm Pdiss=0,164W **CW mode**	105	°C/W
Junction Temperature	Tj		104	°C
Median Life	T50		$1x10^{10}$	Hrs



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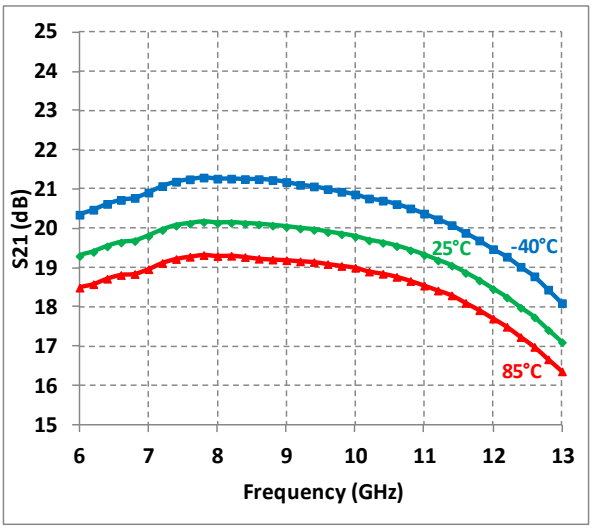
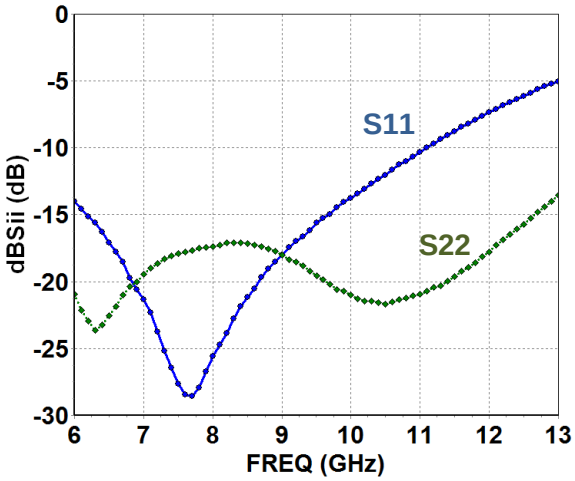
Typical Board Measurements

Vd = +4V, Id = 45mA; pads 1A, 1B, 2A and 2B are non-connected
Measurements are given in the QFN's Sij reference planes.

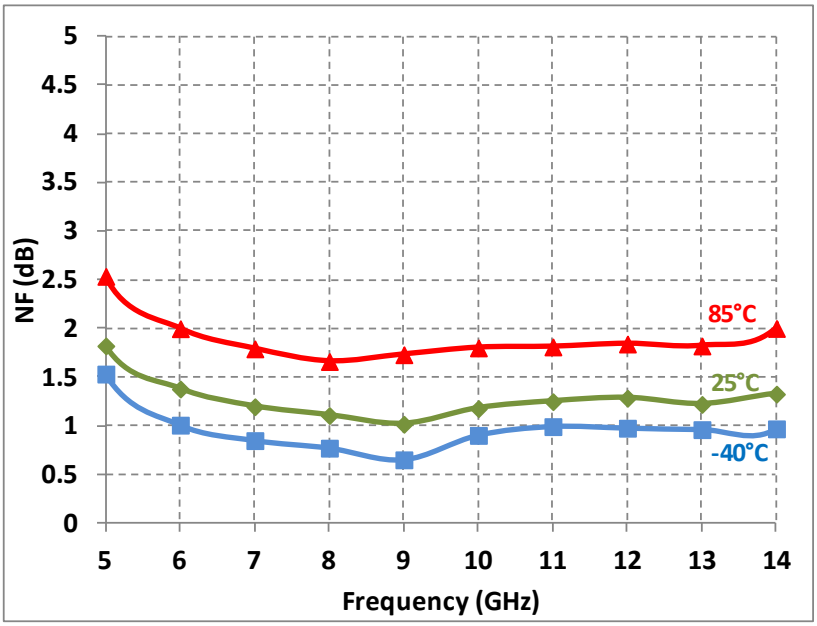
Linear Gain versus frequency and for 3 temperatures



Input/Return losses versus frequency for T=+25°C



NF versus frequency and for 3 temperatures



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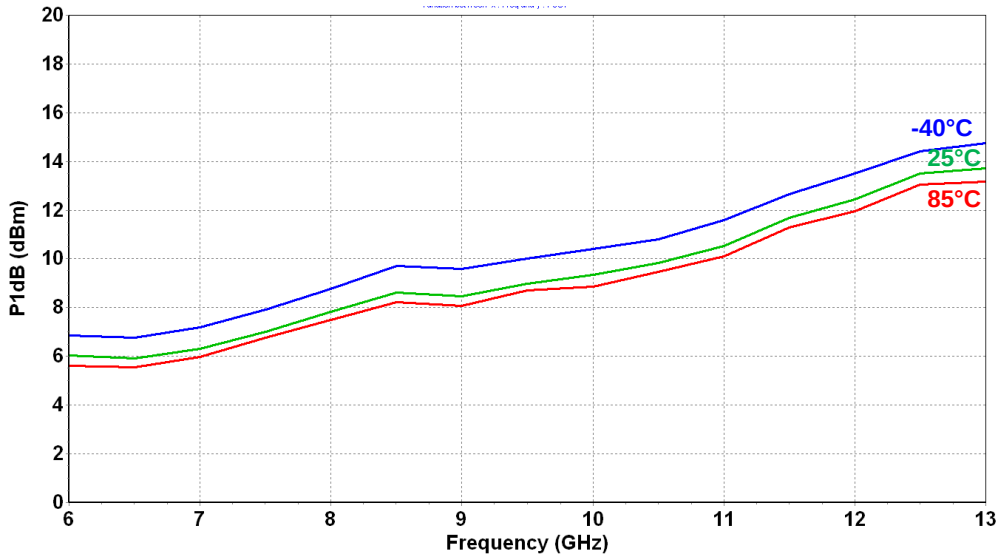
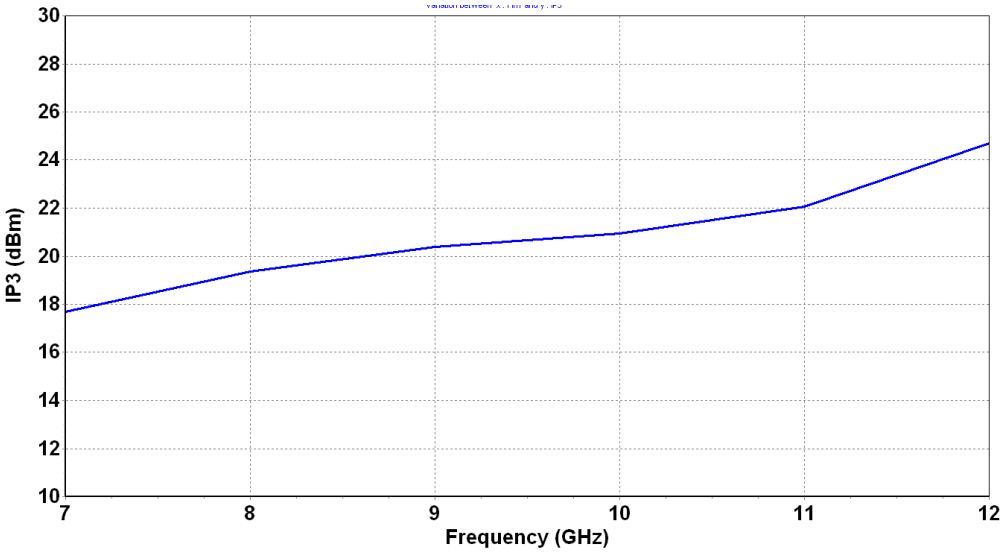
Typical Board Measurements

Vd = +4V, Id = 45mA; pads 1A, 1B, 2A and 2B are non-connected
Measurements are given in the QFN's Sij reference planes.

P1dB versus frequency and for 3 temperatures



IP3 versus frequency for T=25°C



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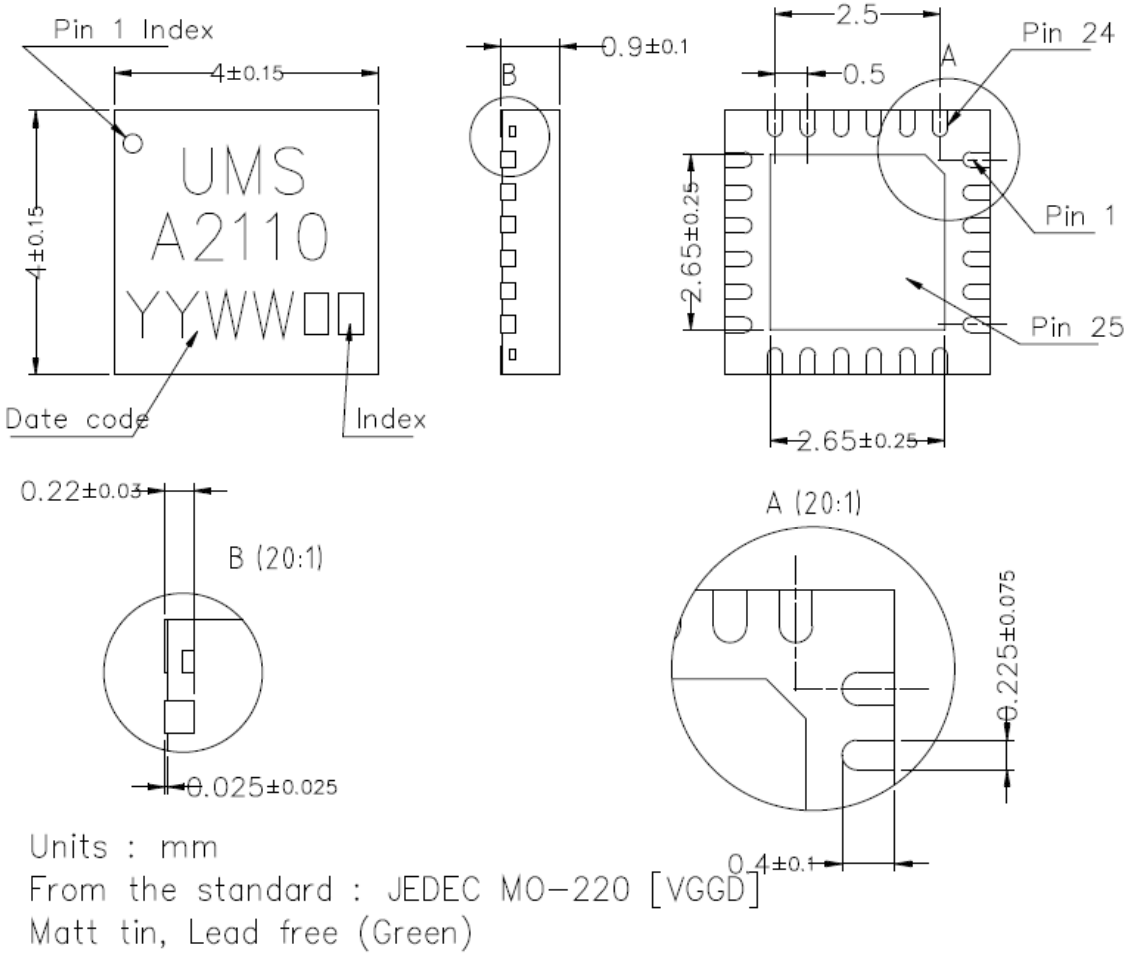
Package outline [1]



Matt tin, Lead Free	(Green)	1- Nc	11- 2B	21- VD2
Units :	mm	2- Gnd[2]	12- Nc	22- VD1
From the standard :	JEDEC MO-220	3- Gnd[2]	13- Gnd[2]	23- Gnd[2]
	(VGGD)	4- RF in	14- Gnd[2]	24- Nc
25-	GND	5- Gnd[2]	15- RF out	
		6- Gnd[2]	16- Gnd[2]	
		7- 1A	17- Gnd[2]	
		8- 1B	18- Nc	
		9- Nc	19- Nc	
		10- 2A	20- Nc	

[1] The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

[2] It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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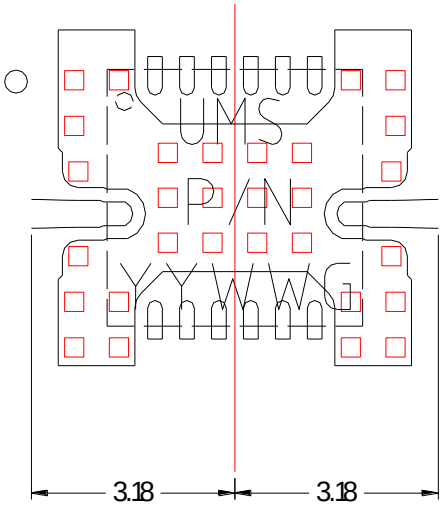
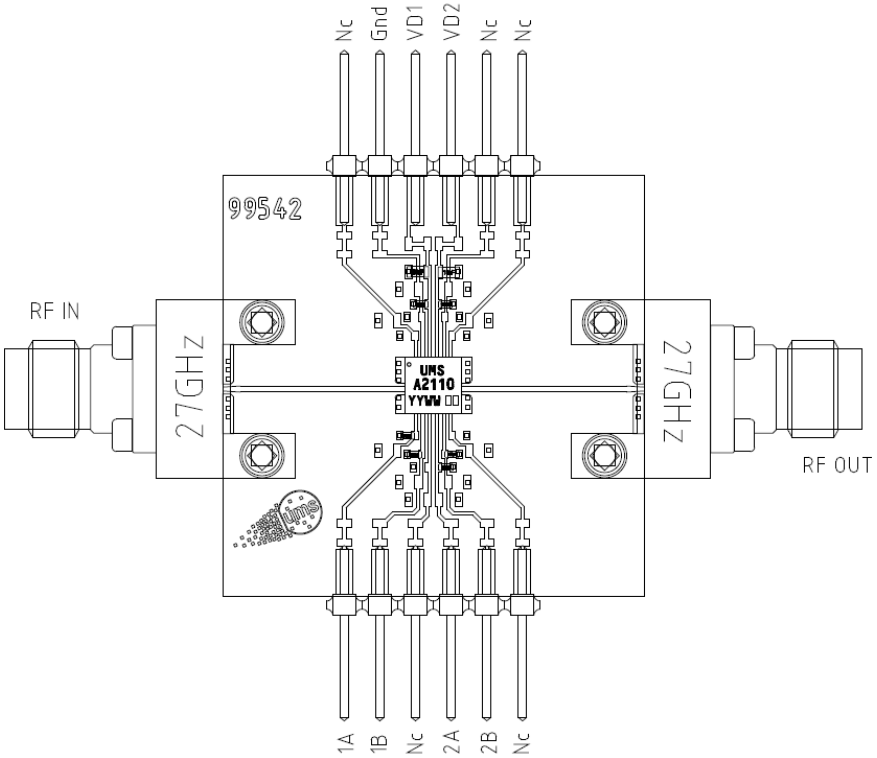
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF and 10nF ±10% are recommended for all VD1 and VD2 accesses.
- See application note AN0017 for details.



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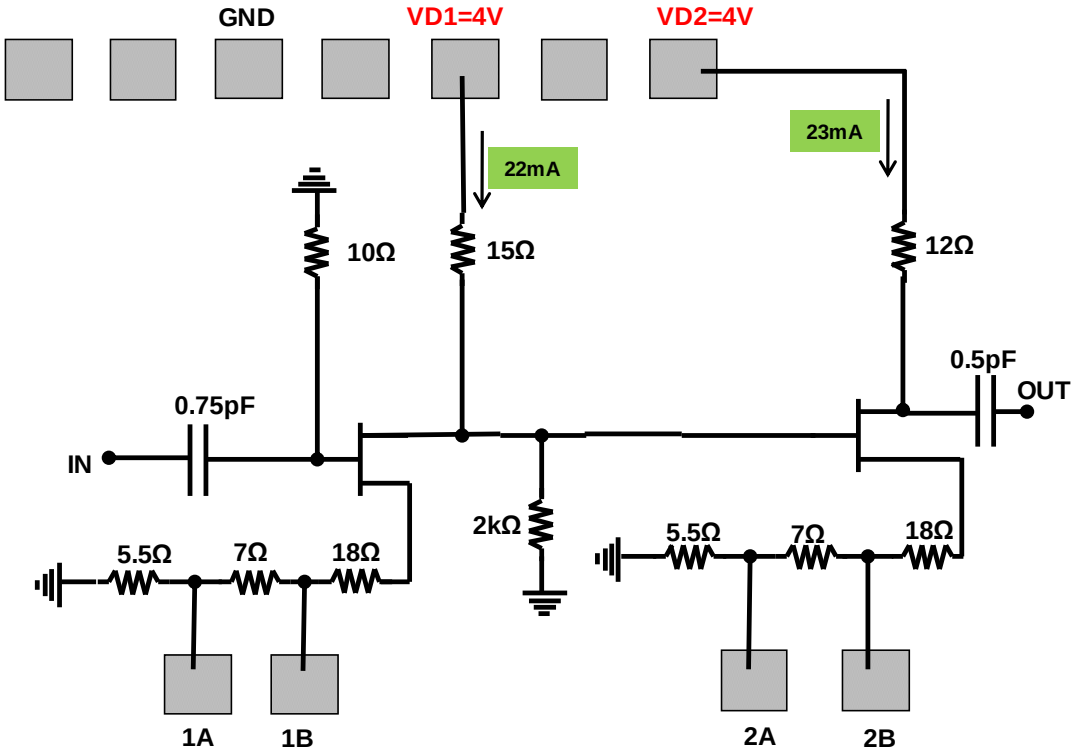
DC Schematic

LNA: 4V, 45mA

This chip is self-biased, and flexibility is provided by the access to number of pads. The internal DC electrical schematic is given in order to use these pads in a safe way.



Requirement:

Not exceed Vds = 3.5Volt (internal Drain to Source voltage).

We propose three standard biasing:

Low Noise / low consumption:	Vd = 4V. The pads 1A, 1B, 2A and 2B are non-connected (NC). Idd = 45mA & Pout-1dB = +10dBm (Typical @f=10GHz)
Low Noise / higher gain:	Vd = 4V and 1A or 1B grounded. All the other pads non-connected (NC). Idd = 55mA & Pout-1dB = +10dBm (Typical @f=10GHz)
Low Noise / higher output power:	Vd = 4V and 2A or 2B grounded. All the other pads non-connected (NC). Idd = 55mA & Pout-1dB = +13dBm (Typical @f=10GHz)

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Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte tin (Sn)
MSL Rating	MSL1

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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 package:	CHA2110-QDG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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