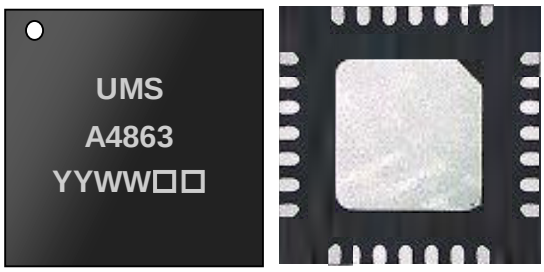
17-24GHz Variable Gain Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

Description

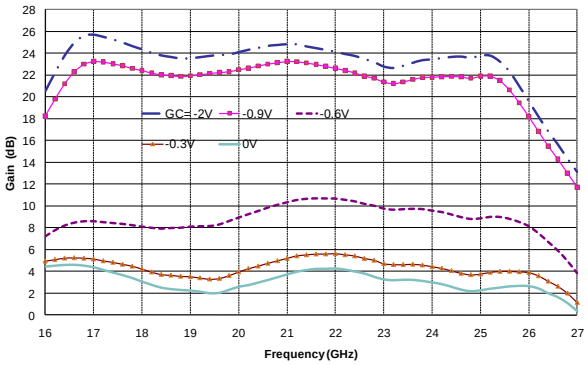
The CHA4863-QGG is a variable gain broadband four stage monolithic amplifier.
It is designed for a wide range of applications, typically commercial communication systems.
The circuit is manufactured with a power pHEMT process, 0.15µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is supplied in RoHS compliant SMD package.



Main Features

- Broadband performances: 17-24GHz
- 24dB gain
- 28dBm Output IP3
- 20dB Gain control range
- DC bias: Vd=4.5V @ Id=200mA
- 28L-QFN5x5

Linear gain versus gain control



Main Characteristics

Tamb.= +25°C, Vd = +4.5V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17		24	GHz
Gain	Linear Gain		24		dB
ΔG	Gain control range		20		dB
OIP3	3rd order intercept point		28		dBm

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Electrical Characteristics

Tamb.= +25°C, Vd = +4.5V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17		24	GHz
Gain	Linear Gain at maximum gain		24		dB
ΔG	Gain control range		20		dB
RLin	Input return loss		-10		dB
RLout	Output return loss		-10		dB
OIP3	Output 3rd order intercept point @ all gain		28		dBm
P1dB	Power at 1dB compression @ max. gain		22		dBm
NF	Noise Figure at maximum gain		11		dB
G12, G34	DC gate voltage stage 1,2, 3 & 4		-1.2		V
GC	DC gain control voltage (GC1 & GC2)	-2.0		0	V
Id	Quiescent drain current (1)		200		mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".
(1) Id not affected by GC

Note: Electrostatic discharge sensitive device observe handling precautions!

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	5	V
Id	Drain bias current	230	mA
G12-G34	Gate bias voltage	-2.0 to +0.4	V
GC1- GC2	Gain control voltage	-2.5 to +0.6	V
Pin	Maximum peak input power overdrive (2)	+10	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.

Device thermal performances

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All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (Tcase) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

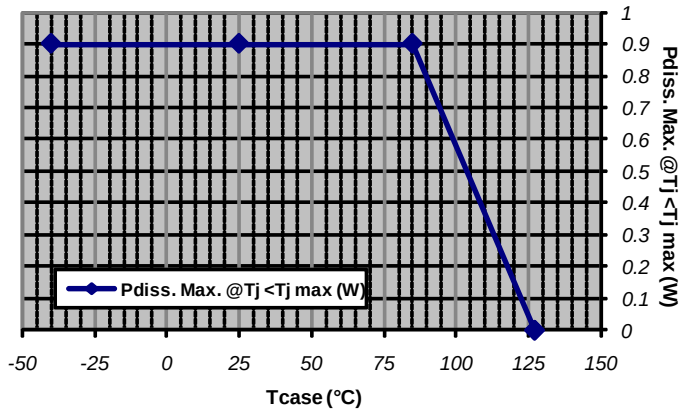
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below than the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

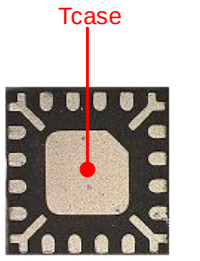
DEVICE THERMAL SPECIFICATION : CHA4863-QGG				
Recommended max. junction temperature (Tj max)			:	127 °C
Junction temperature absolute maximum rating			:	175 °C
Max. continuous dissipated power (Pdiss. Max.)			:	0.9 W
=> Pdiss. Max. derating above Tcase(1)=	85	°C	:	21 mW/°C
Junction-Case thermal resistance (Rth J-C)(2)			:	<47 °C/W
Minimum Tcase operating temperature(3)			:	-40 °C
Maximum Tcase operating temperature(3)			:	85 °C
Minimum storage temperature			:	-55 °C
Maximum storage temperature			:	150 °C

(1) Derating at junction temperature constant = Tj max.

(2) Rth J-C is calculated for a worst case considering the ***hottest junction*** *of the MMIC and all the devices biased.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example: QFN 16L 3x3
Location of temeprature reference point (Tcase) on package's bottom side

6.1

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Typical Package Sij parameters for maximum gain

Tamb.= +25°C, Vd = +4.5V, Id = 200mA, GC= -2V

Freq (GHz)	dB (S11)	Ph (S11)	dB (S21)	Ph (S21)	dB (S12)	Ph (S12)	dB (S22)	Ph (S22)
2	-0.5	137	-79.6	54	-70	51	-0.6	136
3	-0.6	117	-71.8	28	-86.3	64	-0.6	114
4	-0.6	97	-75.7	11	-68	-11	-0.7	90
5	-0.8	74	-70.1	-15	-70.3	3	-0.9	68
6	-0.8	50	-72.2	-38	-73.4	-43	-1	42
7	-1	28	-73.2	-65	-79	-172	-1.1	13
8	-1.1	3	-67.9	138	-71.7	100	-1.4	-19
9	-1.2	-24	-62.7	4	-60.8	15	-1.5	-53
10	-1.3	-52	-58.2	-85	-58.2	-69	-1.7	-88
11	-1.1	-80	-38.8	108	-56.4	-148	-2.2	-124
12	-1.1	-108	-24.8	-21	-51.7	170	-3.9	-162
13	-1.1	-133	-11.6	-117	-56.4	125	-11.4	163
14	-1.1	-158	-0.4	140	-50	114	-9.5	-136
15	-1.5	174	10.1	36	-47.9	68	-7	-177
16	-3.1	137	20.4	-86	-46	33	-10.1	163
17	-9.2	88	25.5	123	-50.3	-7	-12.9	149
18	-20.2	47	24.2	1	-52.4	-10	-12.4	156
19	-24.1	-82	23.4	-94	-52.3	-29	-11.2	127
20	-15.1	-111	24.1	174	-52.4	-33	-11.6	84
21	-12.1	-137	24.6	79	-54.7	-64	-11.9	32
22	-12.2	-171	24	-16	-53.7	-60	-12	-6
23	-15.5	158	22.6	-102	-54.2	-32	-11.5	-31
24	-20.5	104	23.3	171	-55.7	-38	-10.8	-48
25	-16	33	23.6	70	-49.5	-45	-11.5	-55
26	-15.7	-27	19.9	-48	-51.8	-83	-9.5	-41
27	-9.9	-48	13.6	-140	-49.8	-80	-6	-61
28	-6.1	-89	7.4	139	-45.1	-52	-4.6	-83
29	-4	-139	2.6	60	-44.5	-89	-4.1	-106
30	-2.9	172	-4	-19	-37.8	-127	-3.9	-129
31	-2.3	130	-10.8	-91	-40.3	166	-3.6	-156
32	-2	96	-17.6	-157	-46.5	84	-3	178
33	-1.6	66	-24.4	142	-51.9	-104	-2.4	155
34	-1.7	37	-31.4	81	-50.9	-170	-1.7	133
35	-2.3	3	-40.5	13	-48.3	170	-1.3	116
36	-3.9	-45	-52	-83	-56	99	-0.9	104
37	-5.3	-120	-50.5	-134	-52.6	-132	-0.5	94
38	-3.3	167	-57.8	-145	-60.4	-155	-0.4	86
39	-1.3	125	-58.7	54	-59.6	-61	-0.3	81
40	-0.5	102	-53.9	-105	-54.5	-128	-0.1	74

Refer to the “definition of the Sij reference planes « section below

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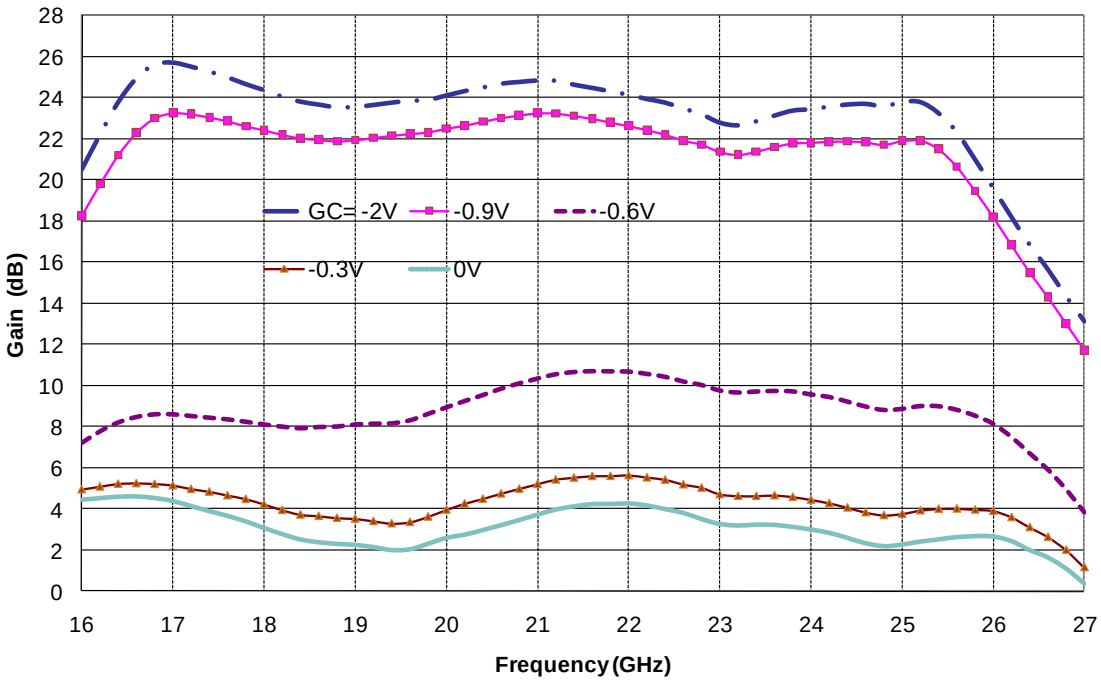
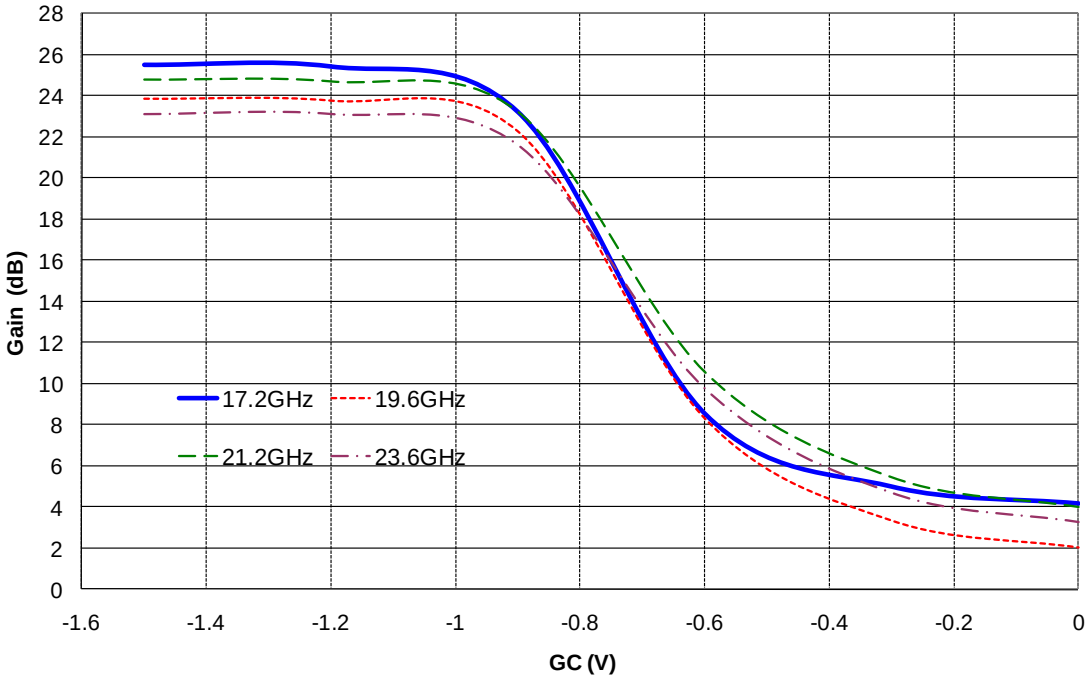
Typical Board Measurements

Tamb.= +25°C, Vd = +4.5V, Id = 200mA
These measurements are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board". Board losses are de-embedded

Linear Gain versus frequency & gain control voltage



Linear Gain versus gain control voltage



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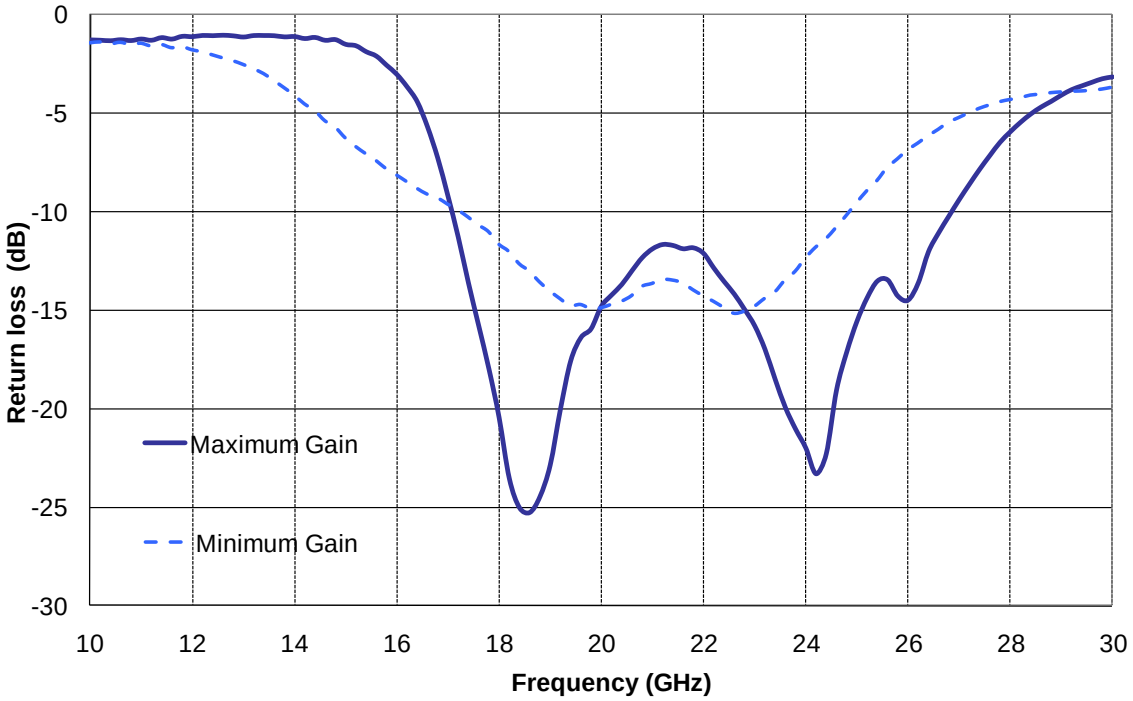
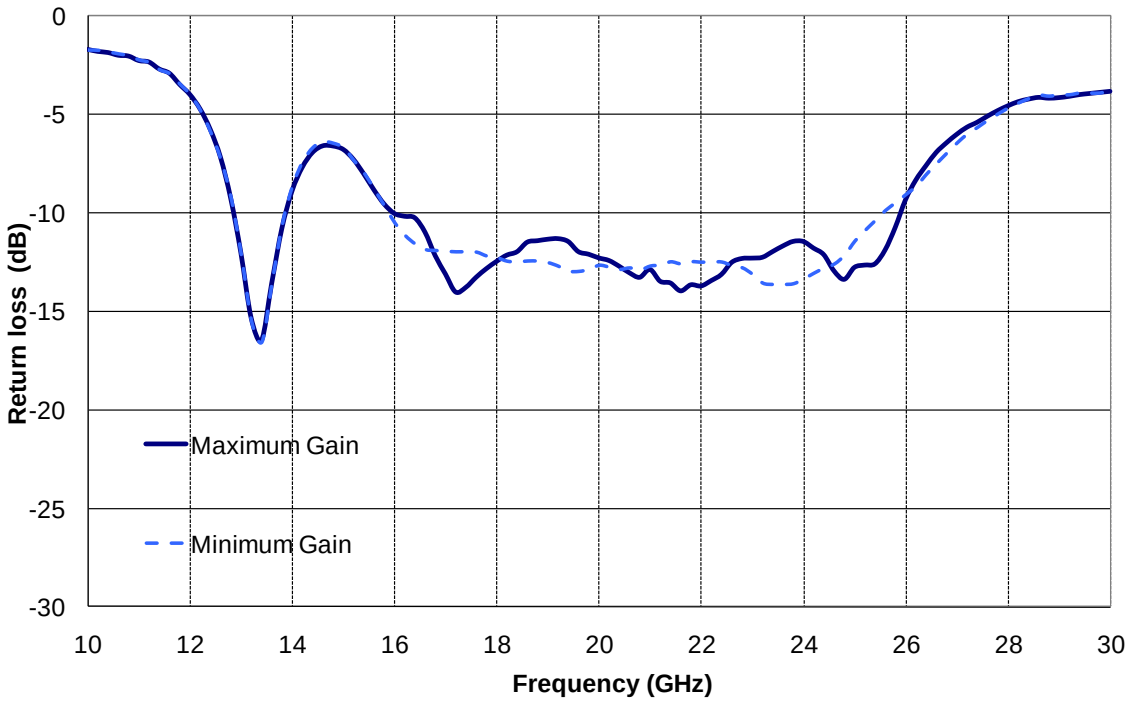
Typical Board Measurements

Tamb.= +25°C, Vd = +4.5V, Id = 200mA

Input return loss at min. & max. gain



Output return loss at min. & max. gain



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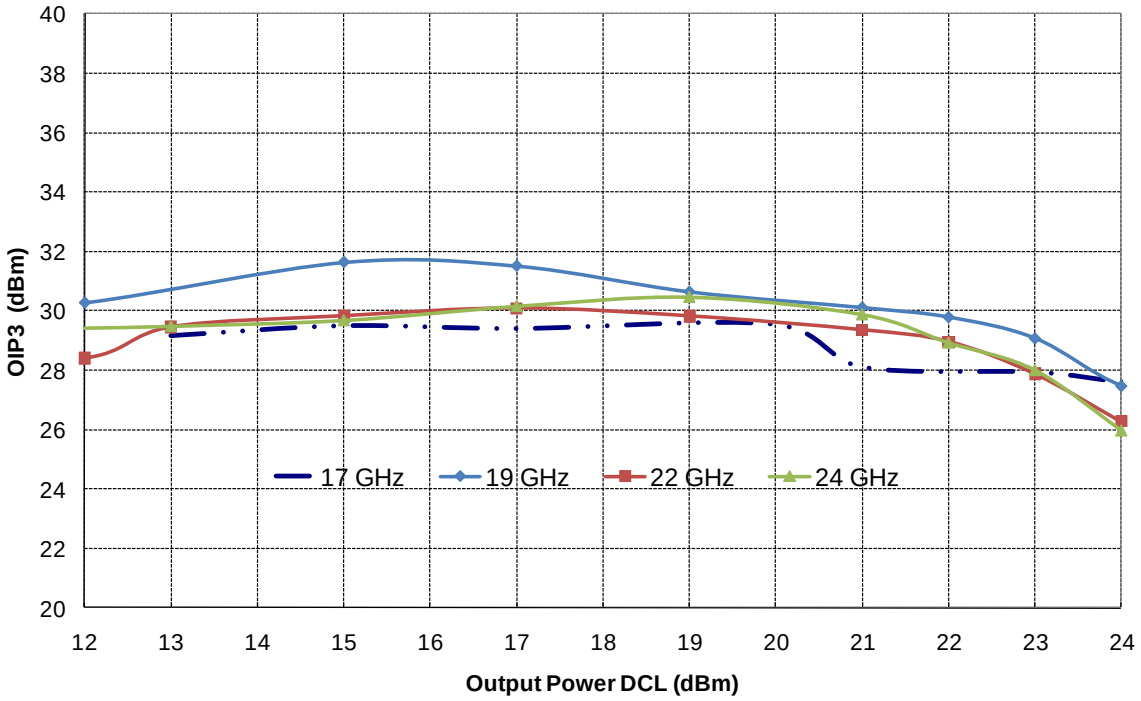
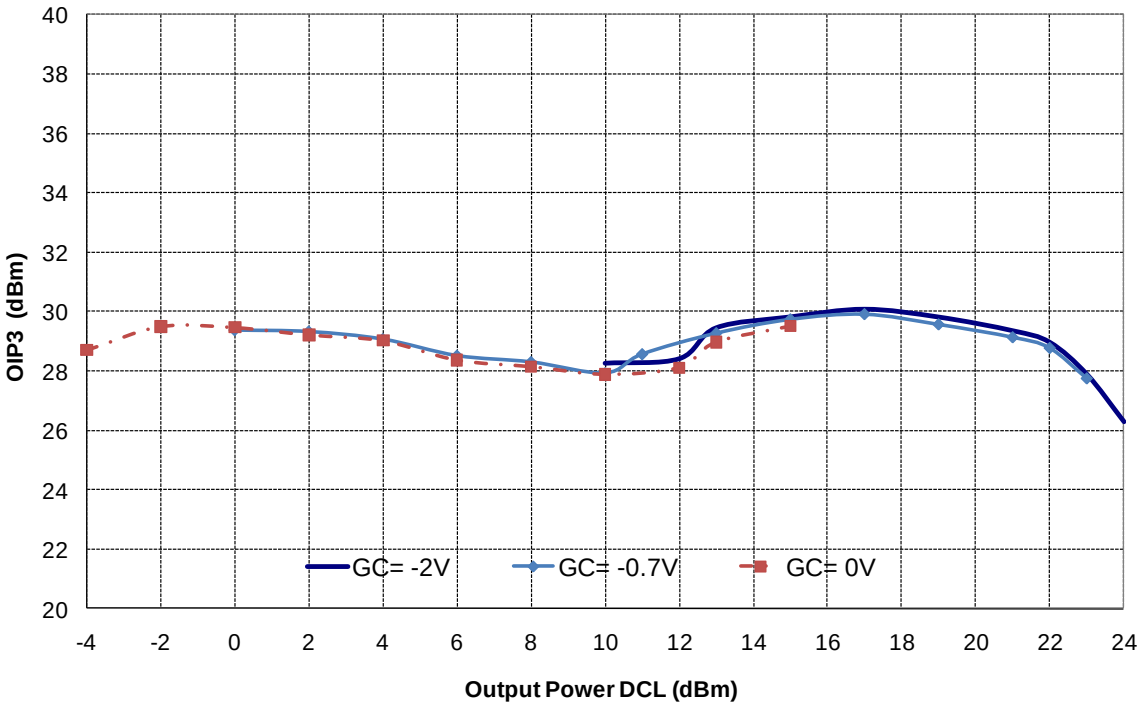
Typical Board Measurements

Tamb.= +25°C, Vd = +4.5V, Id = 200mA

Output IP3 versus frequency at maximum gain
GC= -2V



Output IP3 at 22GHz versus gain control



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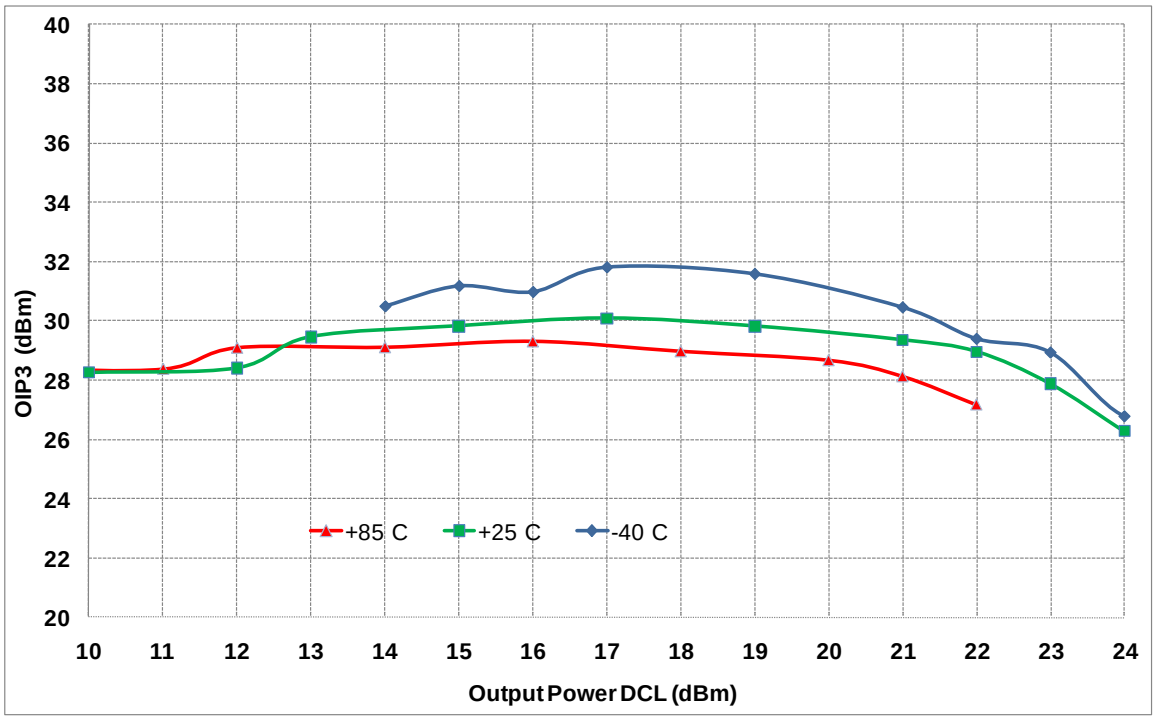
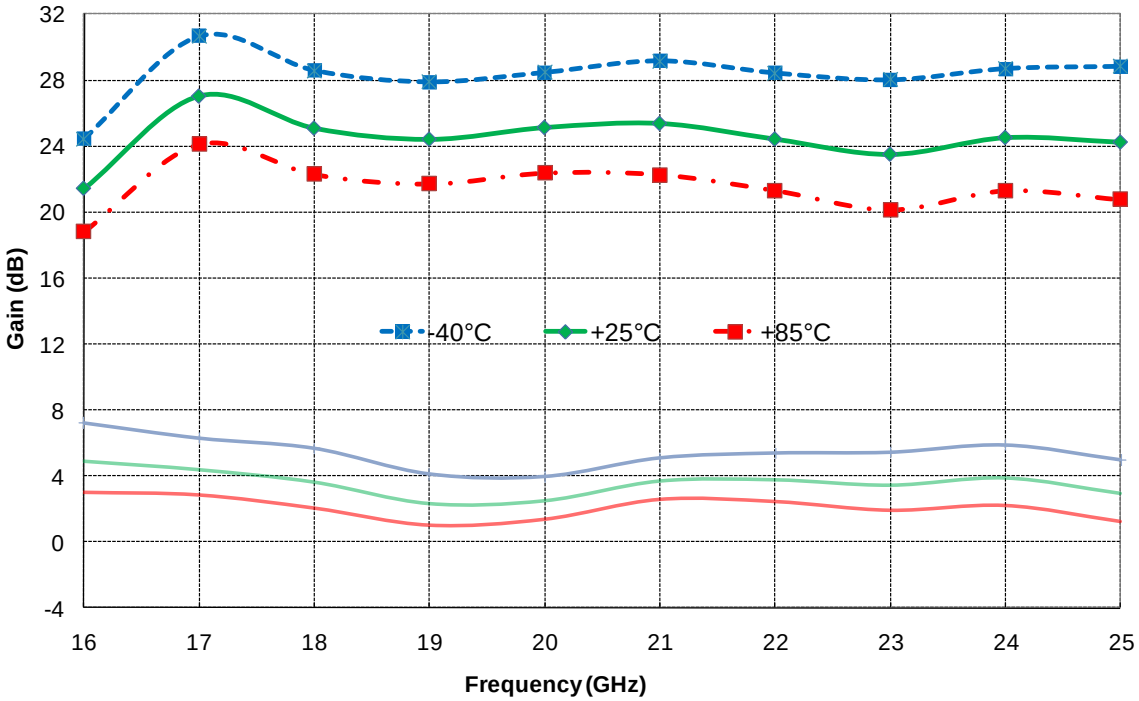
Typical Board Measurements

Tamb.= +25°C, Vd = +4.5V, Id = 200mA

Output IP3 at 22GHz, maximum gain, versus temperature



Maximum & minimum gain versus temperature



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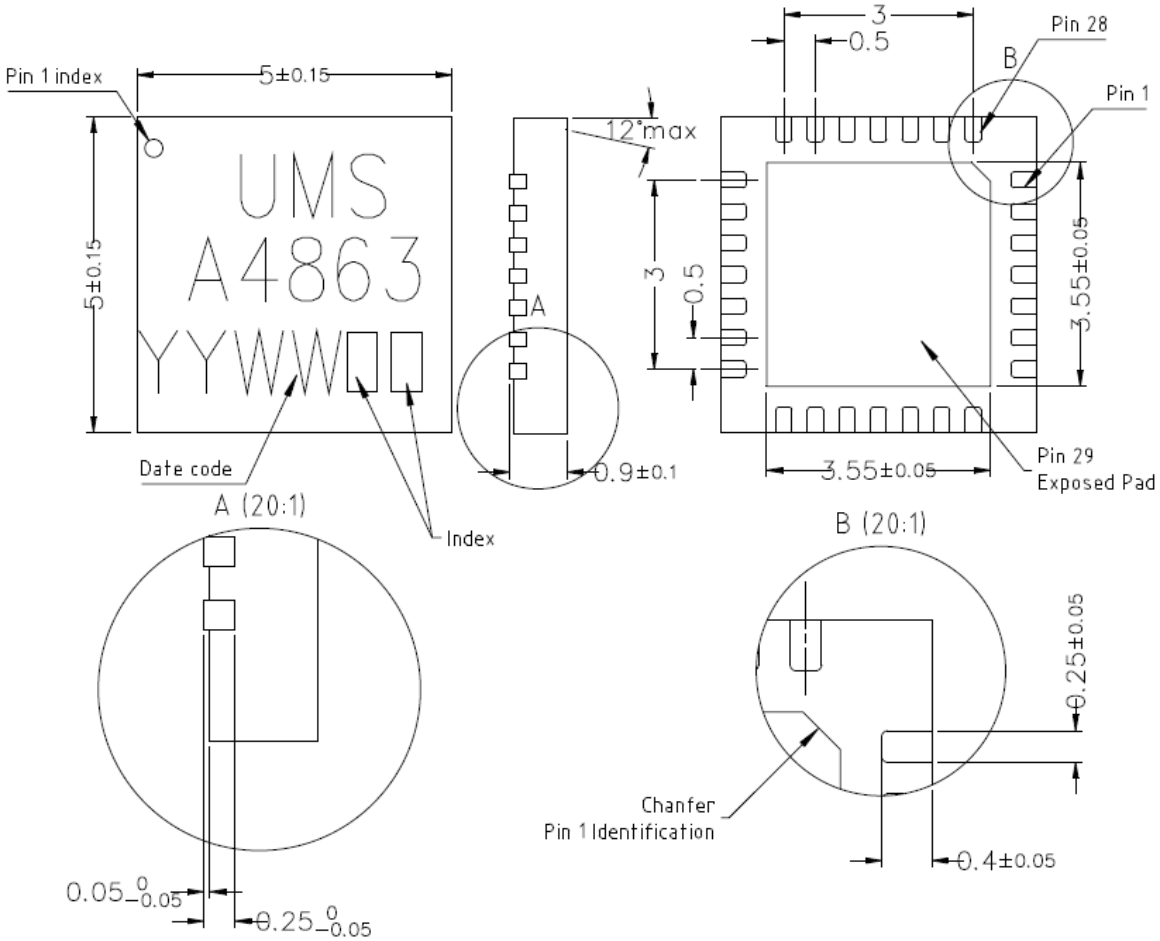
Package outline (1)



Matt tin, Lead Free	(Green)	1-	Gnd(2)	11-	Nc	21-	Gnd(2)
Units :	mm	2-	RF in	12-	Nc	22-	Gnd(2)
From the standard :	JEDEC MO-220 (VGGD)	3-	Gnd(2)	13-	Nc	23-	Nc
		4-	Gnd(2)	14-	Nc	24-	VD
29-	Gnd(2)	5-	Nc	15-	Gnd(2)	25-	Nc
		6-	Gnd(2)	16-	Gnd(2)	26-	G34
		7-	Gnd(2)	17-	RF out	27-	G12
		8-	GC1	18-	Gnd(2)	28-	Nc
		9-	GC2	19-	Gnd(2)		
		10-	Gnd(2)	20-	Nc		

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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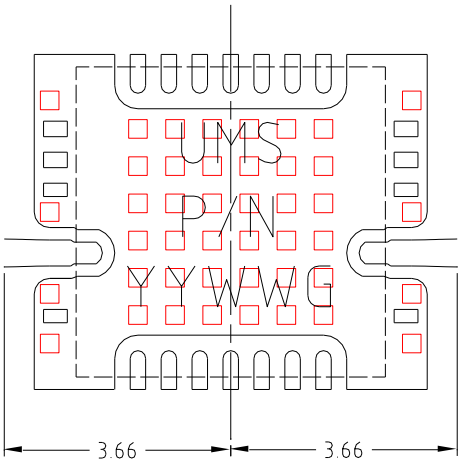
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.66mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



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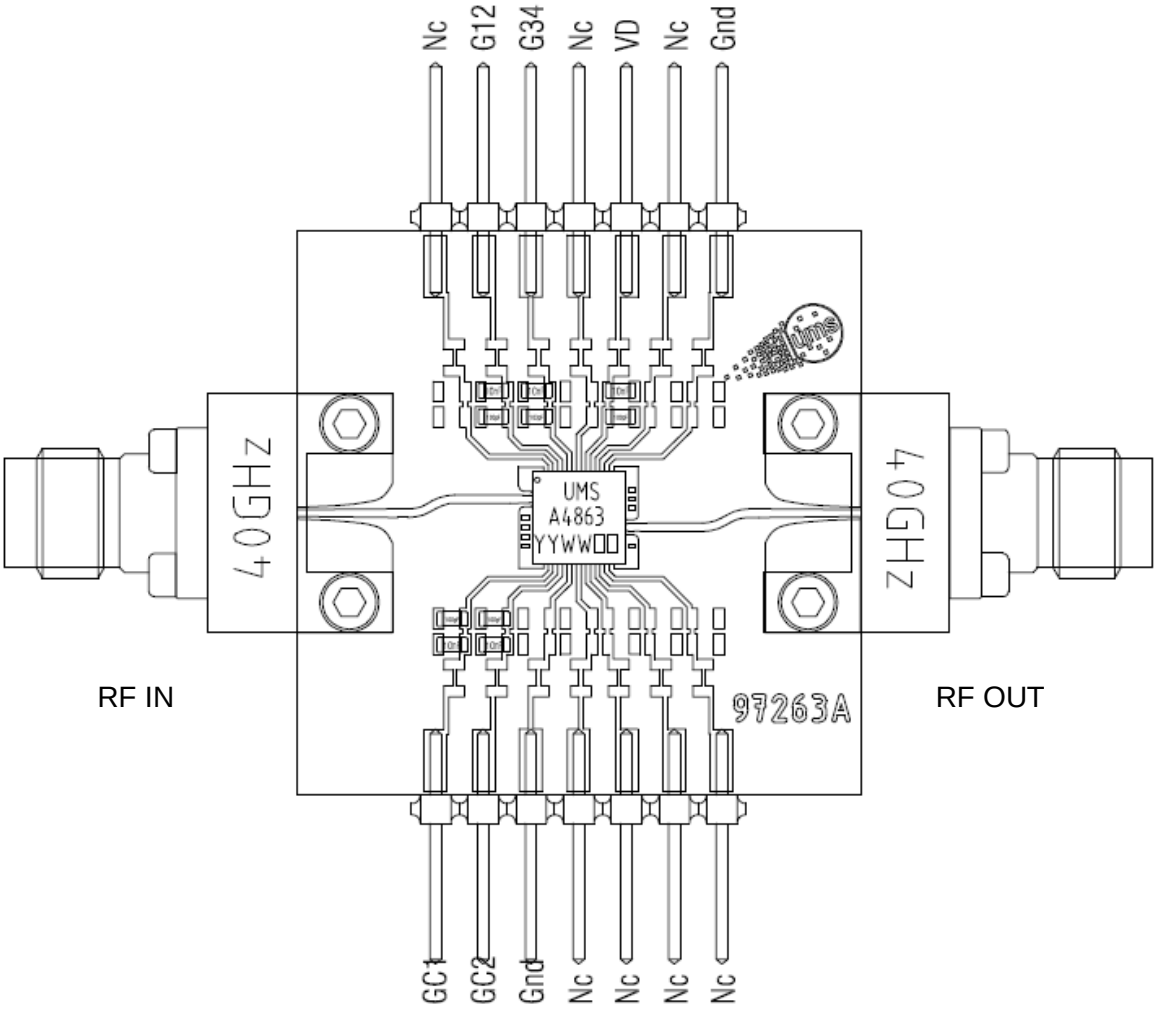
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF ±5% and 10nF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.



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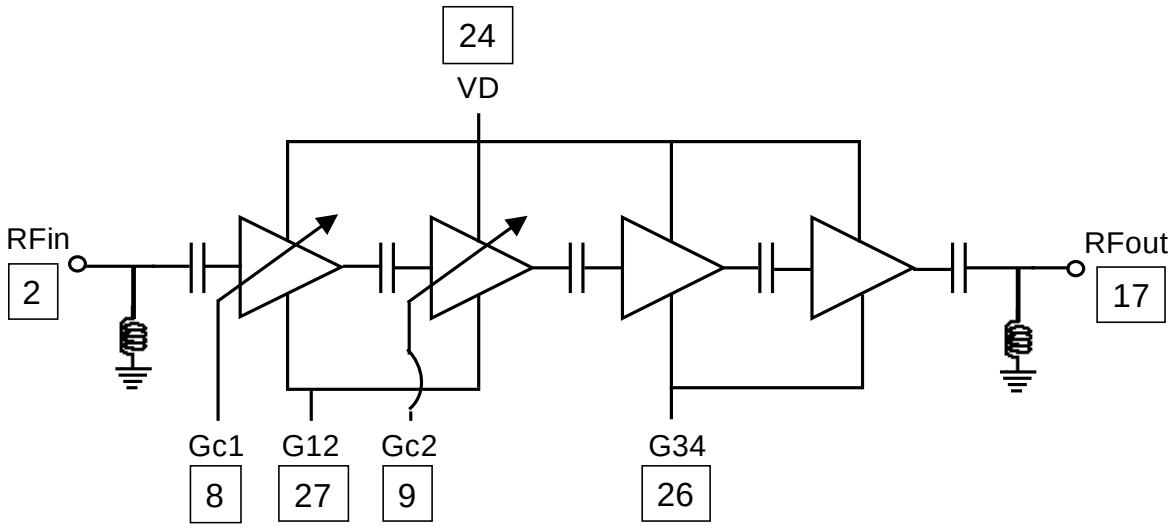
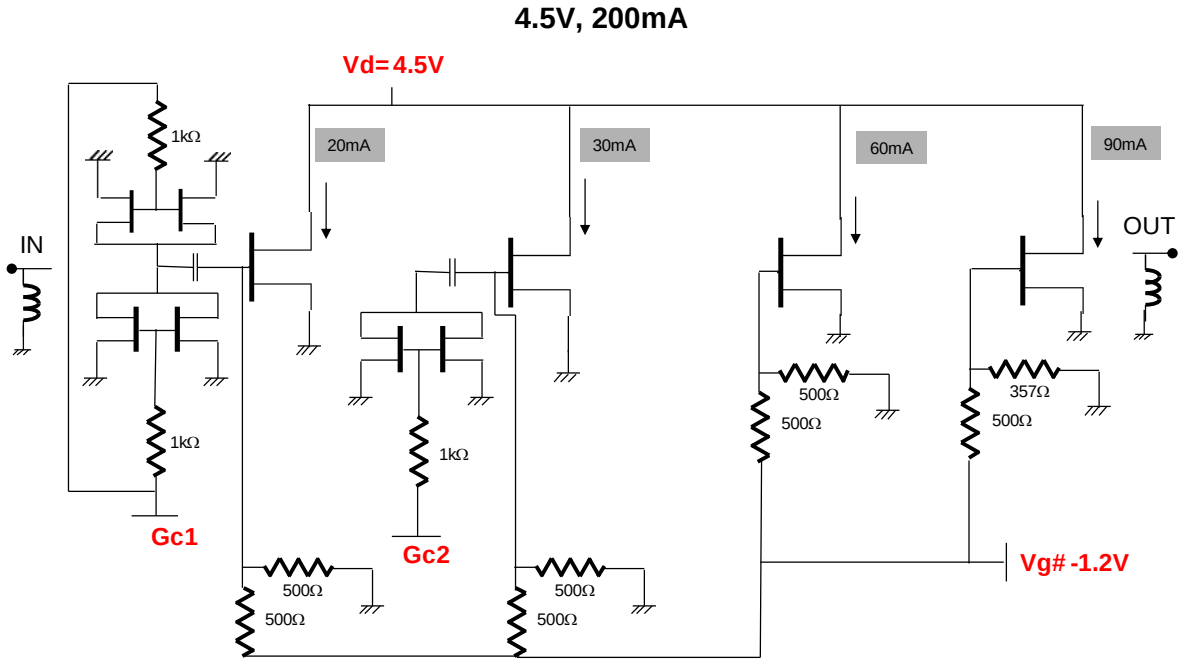
Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



ESD protections are also implemented on gate accesses.
The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (100pF + 10nF) on the PC board, as close as possible to the package.

DC Schematic



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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

Refer to the application note AN0019 available at http://www.ums-gaas.com for environmental data on UMS package products.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

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Ordering Information

QFN 5x5 RoHS compliant package:	CHA4863-QGG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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