28-32GHz HPA 2W

GaAs Monolithic Microwave IC

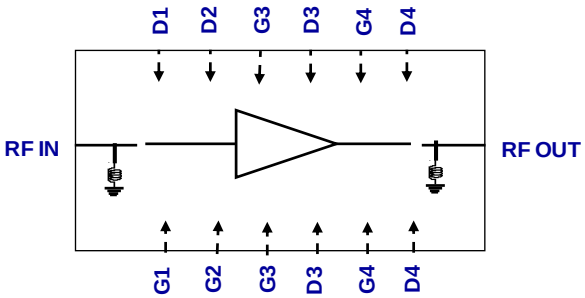
Description

The CHA6558-99F is a monolithic four stages GaAs high power amplifier, designed for Ka-Band applications.

The circuit is dedicated to telecommunication and VSAT, SATCOM and is also well suited for a wide range of microwave applications and systems.

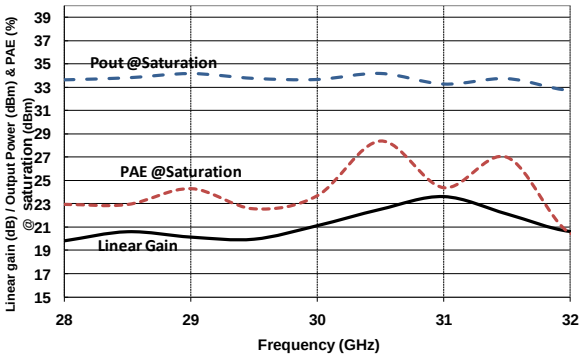
It is developed on a robust 0.15µm gate length pHEMT process, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.



Main Features

- Broadband performances: 28-32GHz
- 21dB Linear Gain
- 33dBm output power @3dB compression.
- 23% PAE@ 3dB compression
- DC bias: Vd=6Volt@Id=1.4A
- Chip size 3.46x2.71x0.07mm



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	28		32	GHz
Gain	Linear Gain		21		dB
Pout	Output Power @3dB compression		33		dBm
PAE	Power added efficiency		23		%

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

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Electrical Characteristics

Tamb = +25°C, Vd = +6V Vg adjusted for quiescent current =1.4A

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Operating frequency range	28		32	GHz
G	Small signal gain		21		dB
P1dB	Output power @ 1dB compression		33.2		dBm
Psat	Saturated output power		33.4		dBm
PAE	Power added efficiency at saturation		23		%
Rlin	Input return loss		-8		dB
Rlout	Output return loss		-6		dB
Id	Supply quiescent drain current		1.4		A
Id_sat	Drain current @ saturation		1.8		A
Vg	Negative gate voltage (G1,G2,G3,G4 pads)		≈-0.5		V

These values are representative of on test fixture measurements a bonding wire of typically 0.3nH at the RF ports.

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Cmp	Gain compression level	5	dB
Vd	Drain bias voltage (D1,D2 ,D3 ,D4)	7	V
Id	Supply quiescent current	1.6	A
Vg	Gate bias voltage	-2 to -0.2	V
Pin	Maximum peak input power overdrive (2)	+18	dBm
Tj	Junction temperature (3)	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Duration < 1s.

(3) Thermal Resistance channel to ground paddle = 6.2°C/W for T= +85°C.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
Vd	D1,D2,D3,D4	DC drain Voltage	6	V
Id		DC Drain current controlled with vg	1.4	A
Vg	G1,G2,G3,G4	DC gate Voltage	≈-0.5(1)	V

(1) To be adjusted until to obtain Id:1.4A

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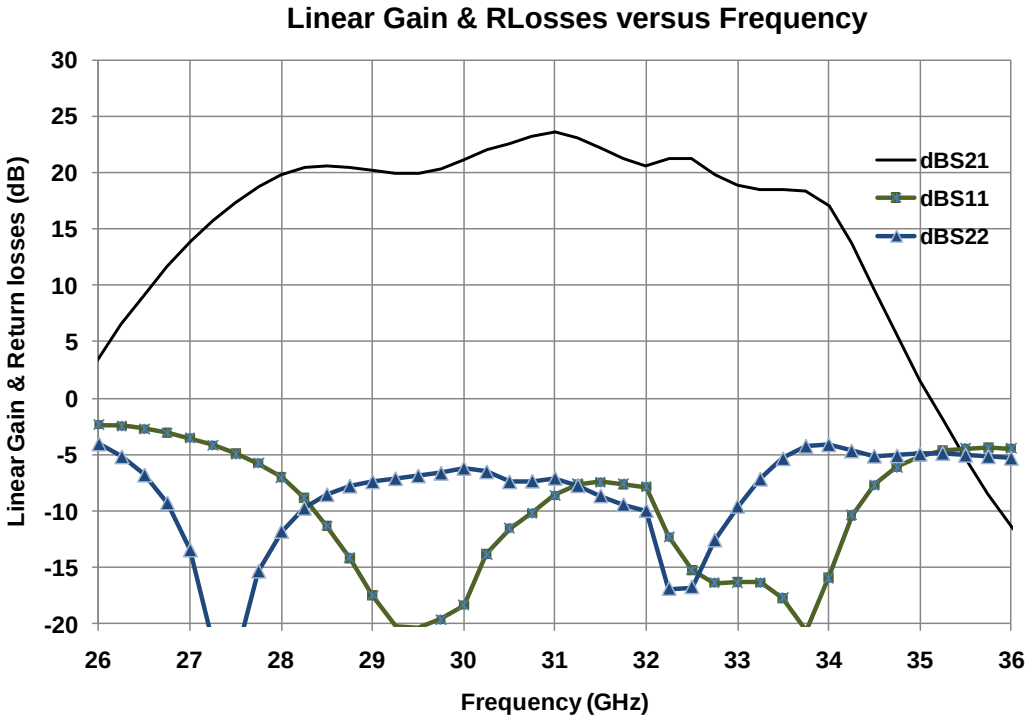
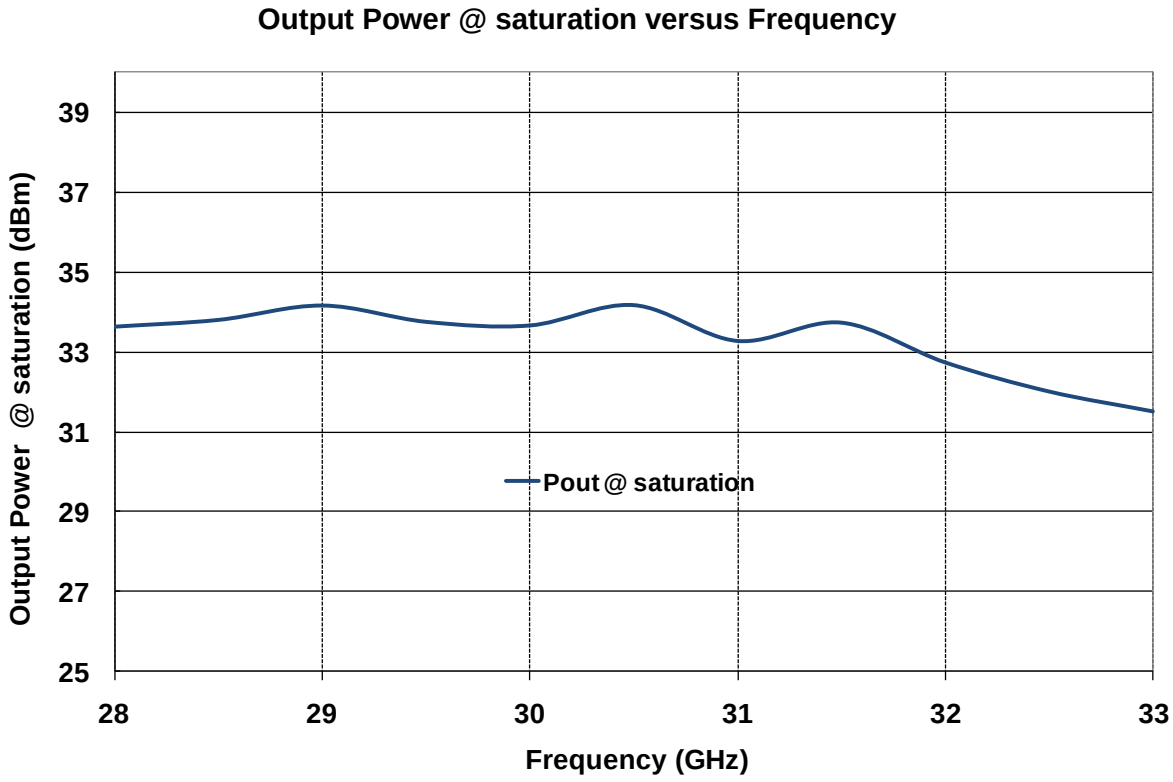
Typical S parameters in test fixture Measurements

Tamb.= +25°C, Vd = +6V, Id = 1.4A





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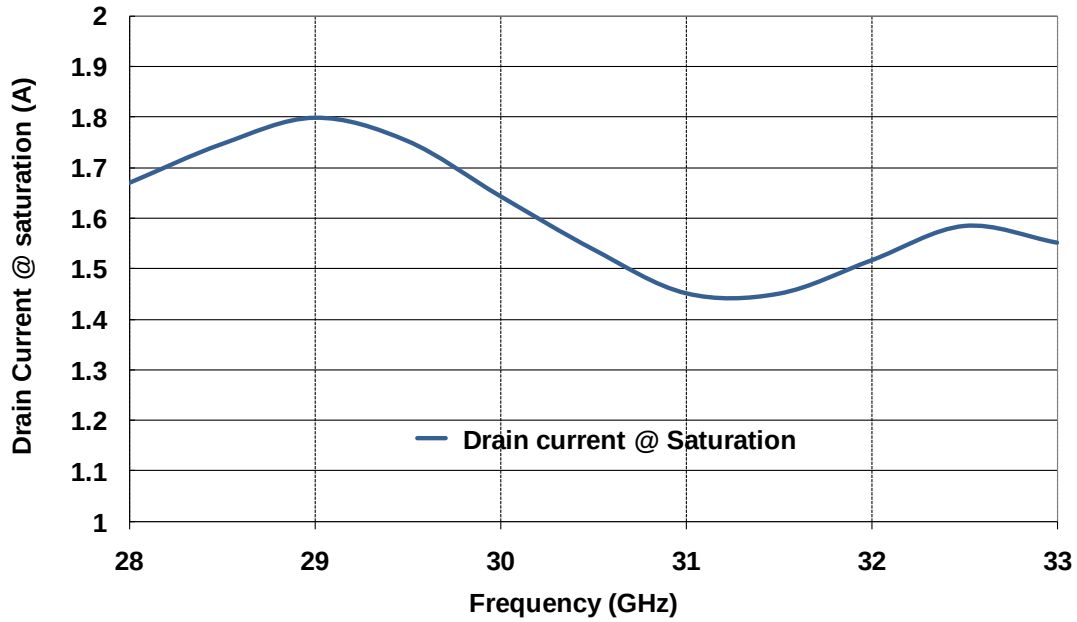
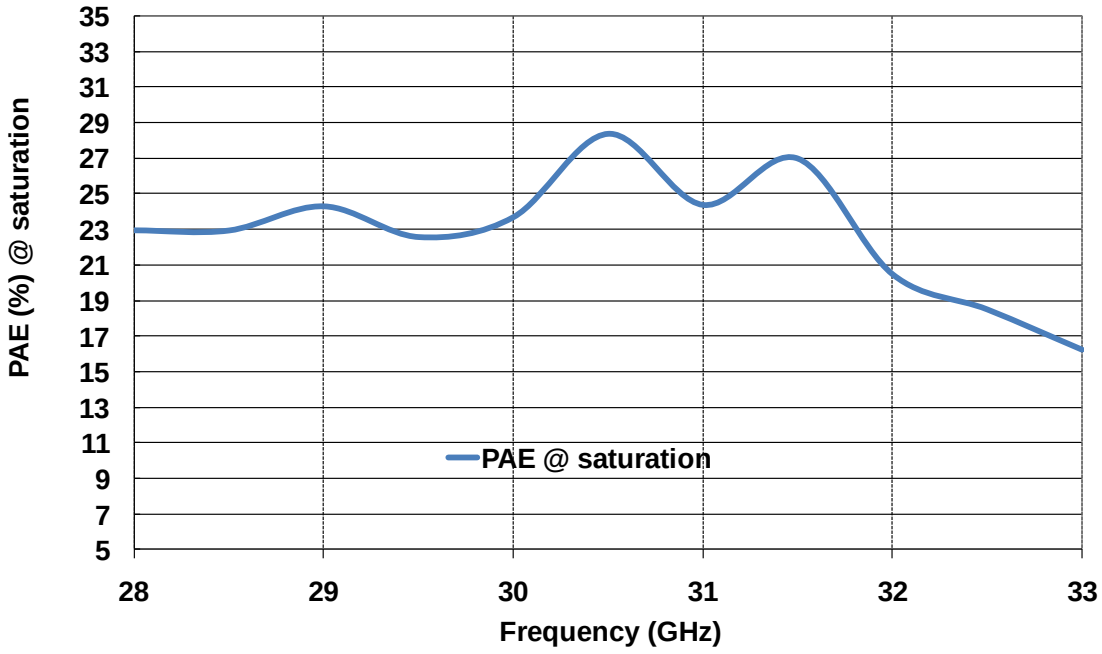
Typical S parameters in test fixture Measurements

Tamb.= +25°C, Vd = +6V, Id = 1.4A

Drain current @ saturation versus Frequency



PAE @ saturation versus Frequency



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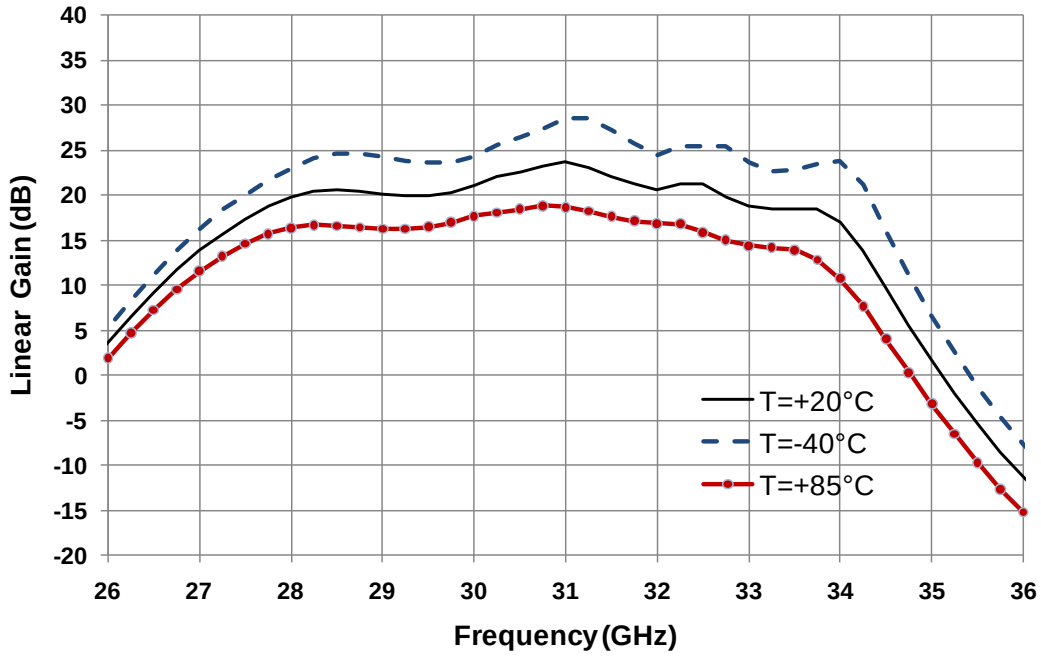
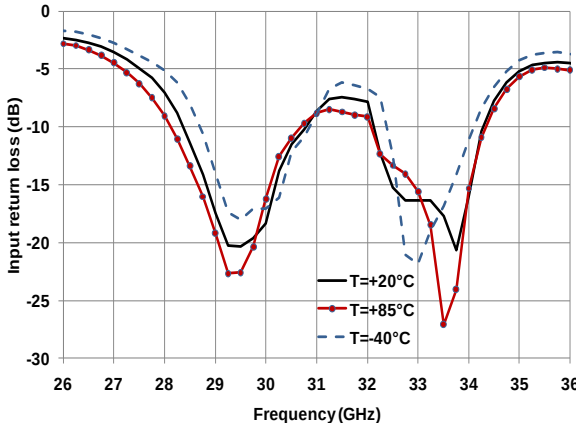
Typical Measurement in test fixture versus Temperature

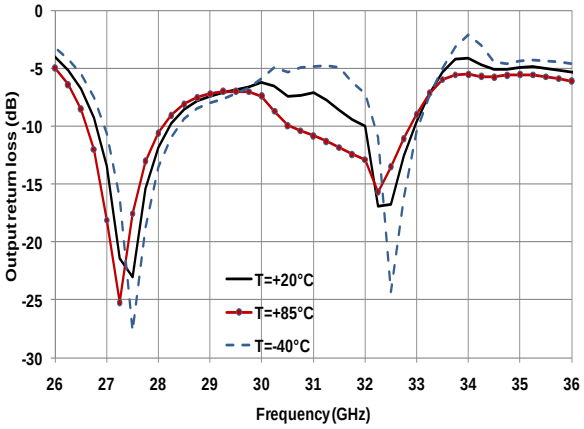
Linear gain versus Frequency & Temperature



Input Return Loss versus Frequency & Temperature



Output return loss versus Frequency & Temperature



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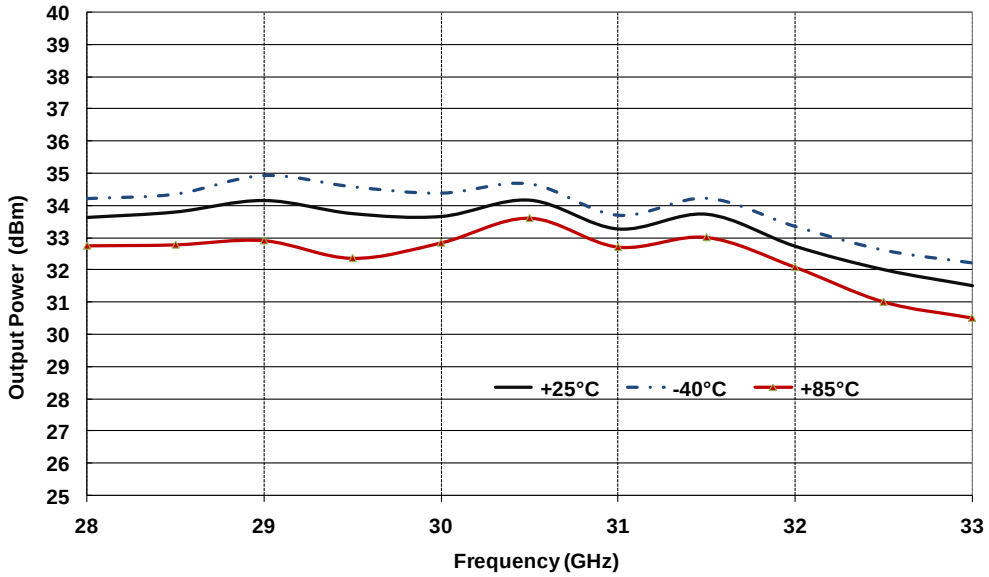
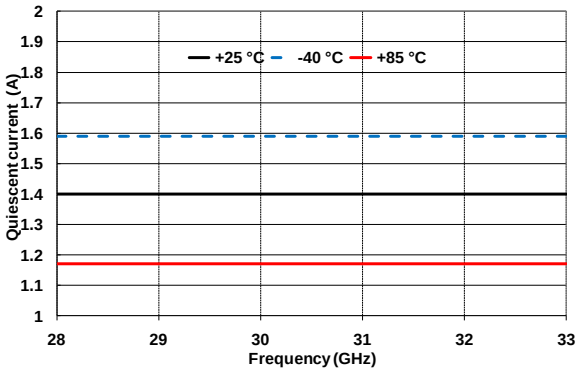
Typical Measurement in test fixture versus Temperature

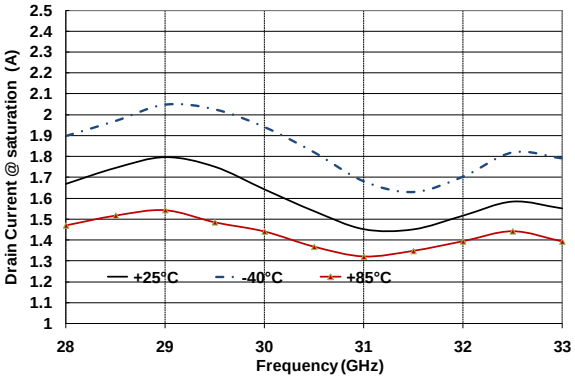
Output Power versus Frequency & Temperature



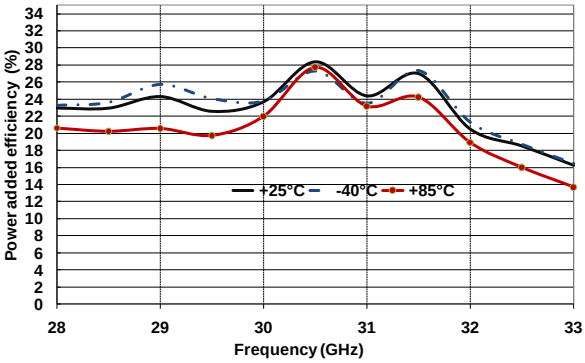
Quiescent current versus temperature



Drain current @ saturation versus temperature



PAE @saturation versus Temperature



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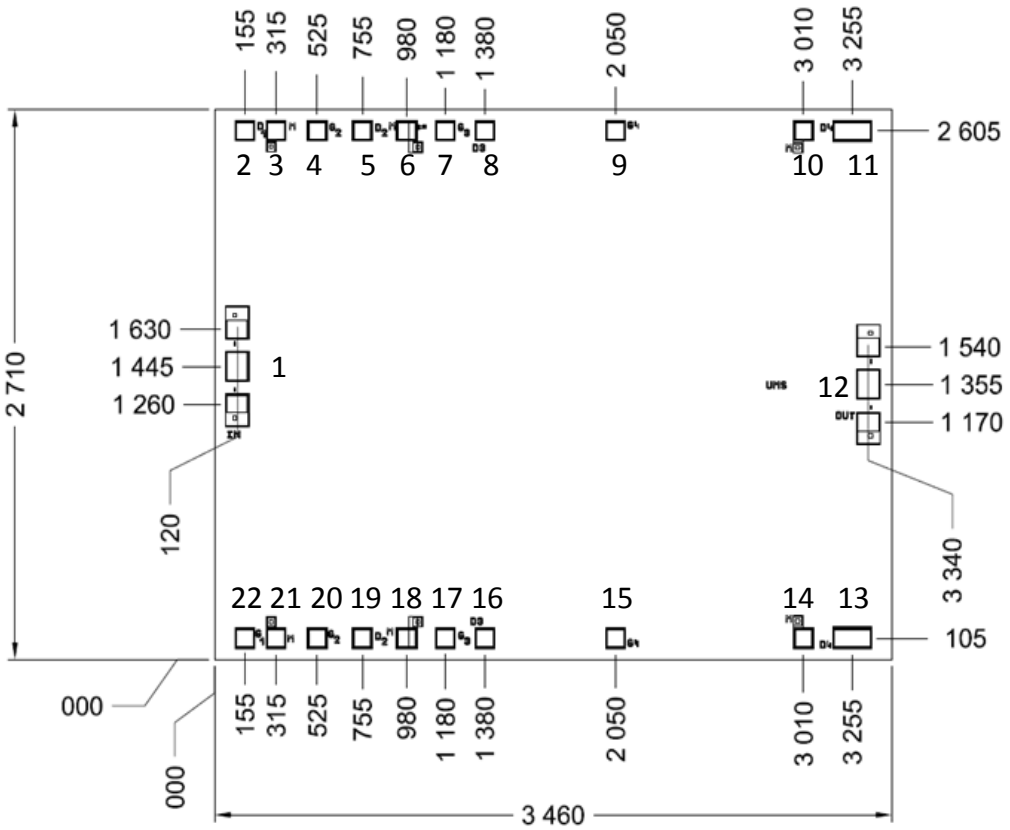
Mechanical data



Units: µm
Chip width and length are given with a tolerance of ±35µm
Chip thickness = 70µm +/- 10 µm
RF pads (1, 12) = 120 x 150µm²
DC pads (2, 3, 4, 5, 6, 7, 8, 9, 10, 14, 15, 17, 18, 19, 20, 21, 22) = 100 x 100µm²
DC pads (11, 13) = 200 x 100µm²

Pin number	Pin name	Description
1	IN	Input RF
3, 6, 10, 14,18, 21	M	Not connected
22	G1	Gate Stage1
2	D1	Drain stage1
4, 20	G2	Gate Stage2
5, 19	D2	Drain stage2
7, 17	G3	Gate Stage3
8, 16	D3	Drain stage3
9, 15	G4	Gate Stage4
11, 13	D4	Drain stage4
12	OUT	Output RF

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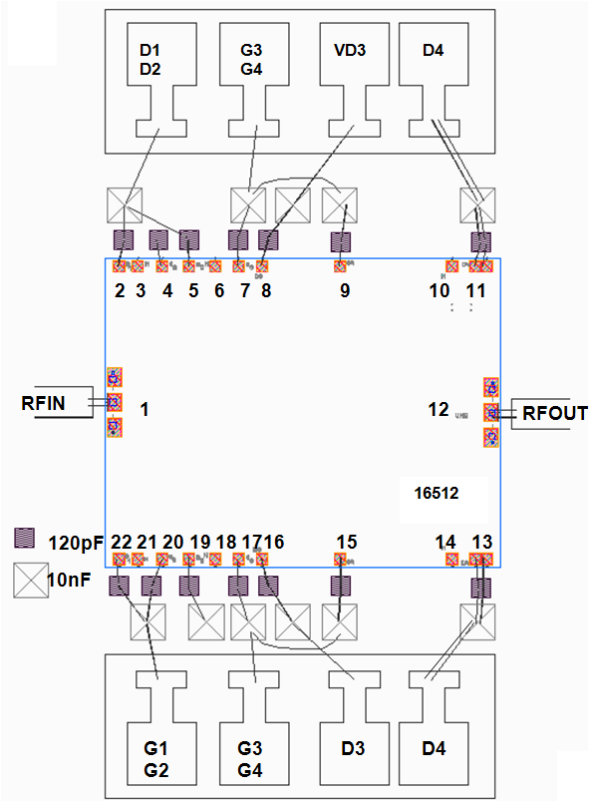
Recommended Chip assembly & Bonding Diagram



-For best thermal and electrical performances, the chip should be brazed on a metal base plate.

The RF and DC connections should be done according to the following table:

- DC drain voltage (Pads: D*): Connection of all the pads is mandatory excepted Pad D2 which can be used on one side only. (Pin number 5 or 19)

-DC gate voltage: (Pads G*): Connection of all the pads is mandatory excepted Pads G2 & G3 (Pin number 4 or 20 for G2 & Pin number 7 or 17 for G3) which can be used on one side only.

Note: Connection of the pin 19 (other possibility to connect D2) is not mandatory if connection of pin 5 has been used, nevertheless it is necessary to add the 120pF and 10nF external capacitor.

Recommended circuit bonding table

Port	Connection	External capacitor
IN	Inductance (Lbonding) = 0.3nH 2 gold wires with diameter of 25µm (550µm max)	
OUT	Inductance (Lbonding) = 0.3nH 2 gold wires with diameter of 25µm (550µm max)	
G*	Inductance ≤ 1nH	C1 ~ 120pF, C2 ~ 10nF
D* (1)	Inductance ≤ 1nH	C1 ~ 120pF, C2 ~ 10nF

(1) 2 gold wires with diameter of 25µm are necessary to connect D4

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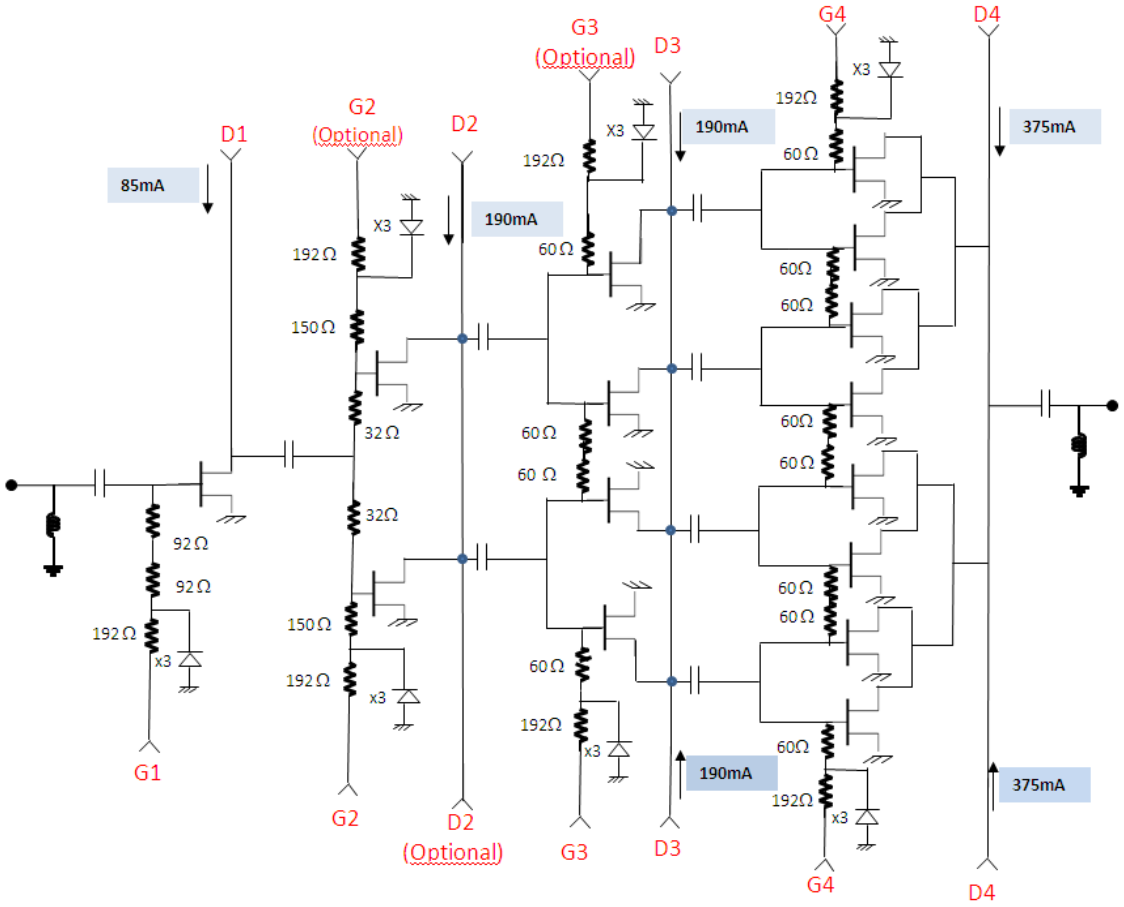
DC SCHEMATIC

HPA : 6V, 1.4A



ESD protections exist on RF accesses. Note that supply feed should be bypassed. ESD protections are also implemented on each gate access.

It is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the chip.

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Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com**.**

Ordering Information

Chip form:	CHA6558-99F/00

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