6-18GHz Low Noise Digital Variable Amplifier

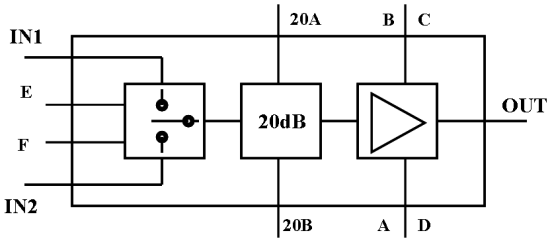
GaAs Monolithic Microwave IC

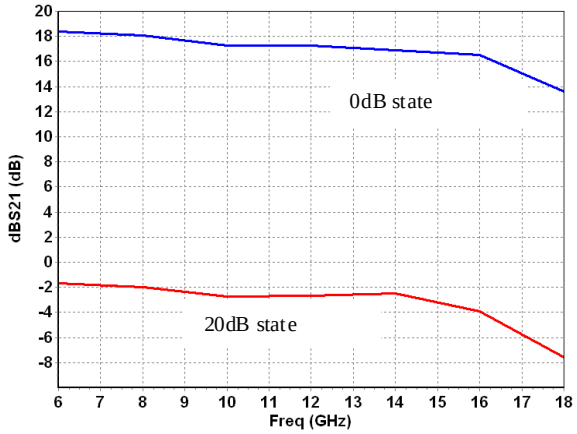
Description

The CHA3512 is composed by a Single Pole Double Through (SPDT) switch followed by a one step digital attenuator and a double stage travelling wave amplifier. It is designed for defense applications. The backside of the chip is both RF and DC grounded. This helps to simplify the assembly process.

The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.





Typical on wafer Measurements
Gain versus attenuation states

Main Features

- Performances: 6-18GHz
- 23dBm saturated output power
- 16dB gain
- 1 bit attenuator for 20dB dynamic range
- DC power consumption: 210mA @ 4.5V
- Chip size: 4.27 x 2.46 x 0.1mm

Main Characteristics

Tamb. = 25℃

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	6		18	GHz
G	Small signal gain @ Attenuator state 0dB		16		dB
Psat	Saturated Output power @ Attenuator state 0dB		23		dBm
ATT dyn	Attenuator range		20		dB

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions !

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Electrical Characteristics on wafer

Tamb = +25℃
Vd = Pads B, D = 4.5V, Vg = Pads A, C tuned for Id = 210mA

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range (1)	6		18	GHz
G	Small signal gain @ Attenuator state 0dB (1)		16		
	6-16GHz	14	16		dB
	16-18GHz	10	13		
ATT dyn	Attenuator range	19	20	22	dB
Is	Isolation @ Attenuator state 0dB & switch OFF (1)	-25	-35		dB
P1dB	Output power at 1dB compression @ Attenuator state 0dB (1)		20		dBm
Psat	Saturated Output power @ Attenuator state 0dB (1)		23		dBm
NF	Noise figure @ Attenuator state 0dB		7		dB
RL_IN	Input Return Loss all attenuator states (switch ON)		-15	-8	dB
RL_OUT	Output Return Loss all attenuator states (switch ON and switch OFF)		-20	-6	dB
Vd	Drain bias DC voltage (Pads B, D)		4.5		V
Id	Bias current @ small signal		210	250	mA
Vc	Control voltage for Attenuator bit & SPDT switch	-5		0	V

(1) These values are representative for on-wafer measurements that are made without bonding wires at the RF ports.

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Absolute Maximum Ratings

Tamb. = 25℃ (1)

Symbol	Parameter	Values	Unit
Vd	Maximum Drain bias voltage (Pads B, D)	+5	V
Id	Drain bias current with Vd=4.5V	300	mA
Vg	Gate bias voltage (Pads A,C)	-2 to +0.4	V
Vc	Attenuator bit & SPDT control voltage	-7 to +0.6	V
Pin	Maximum input power overdrive (2)	+20.0	dBm
Tch	Maximum channel temperature	+175	℃
Ta	Operating temperature range	-40 to +70	℃
Tstg	Storage temperature range	-55 to +125	℃

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.
Thermal Resistance channel to ground paddle =123℃/ W for Tamb. = +70℃.

LNA Control interface

The attenuator state is controlled by 2 voltages. The SPDT switch is controlled by 2 voltages.

state	Theoretical attenuation (dB)	Voltage CONTROL PAD		Switch control	
		20A (V)	20B (V)	E (V)	F (V)
0	0 référence	-5	0	-5	0
1	20	0	-5	-5	0
2	Isolation	-5	0	0	-5

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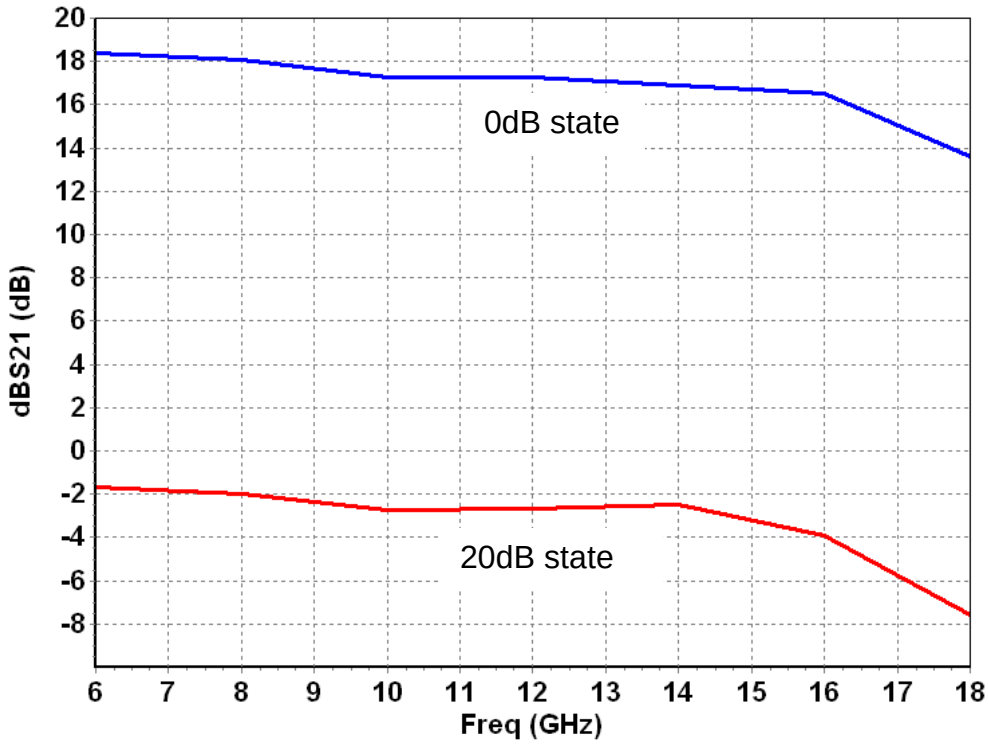
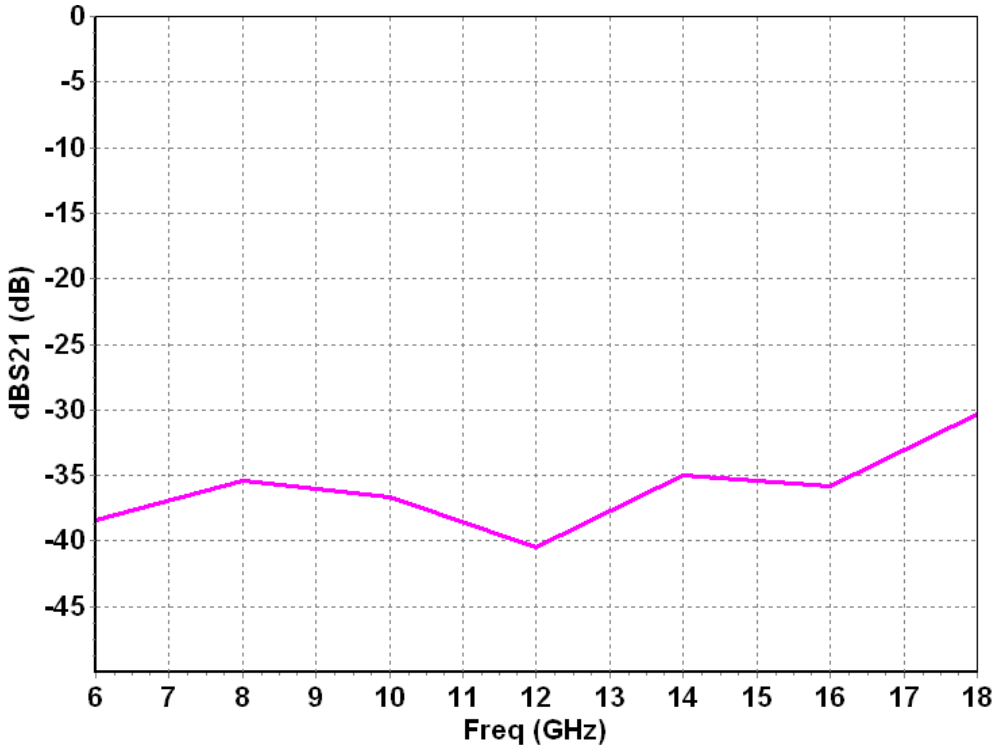
Typical on wafer Measurements @ 25°C

Bias conditions: Vd = 4.5V, Vg tuned for Id = 210mA



Linear Gain versus attenuator states



Linear Gain with SPDT switch OFF

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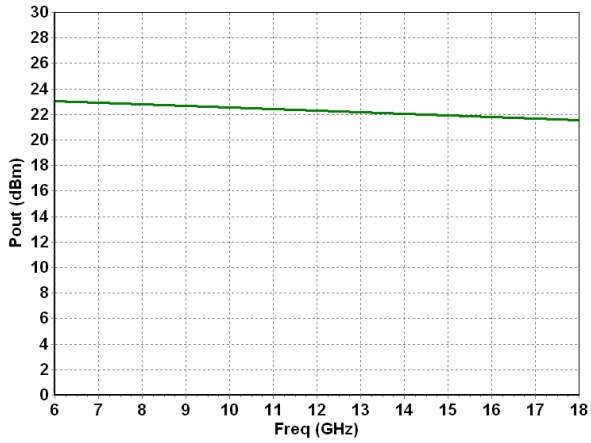
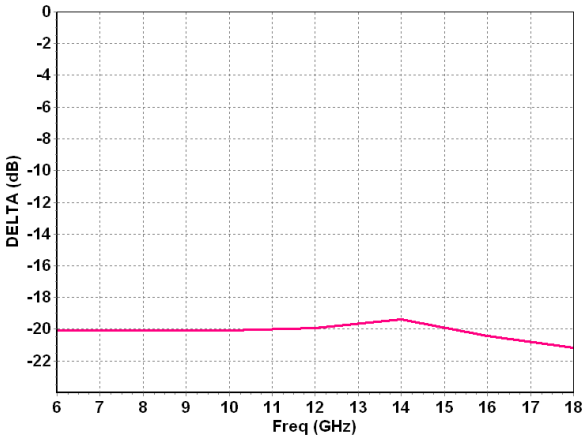
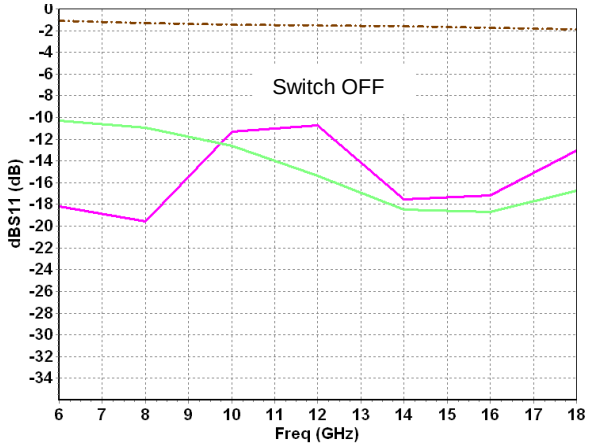


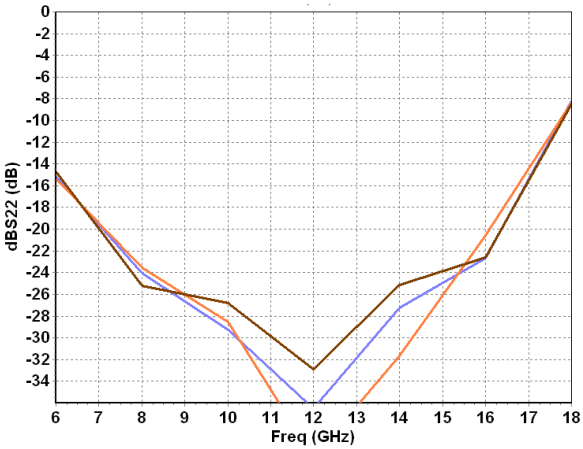
Saturated output power@nominal state



Attenuator accuracy versus frequency



dB(S11) versus frequency for all states



dB(S22) versus frequency for all states

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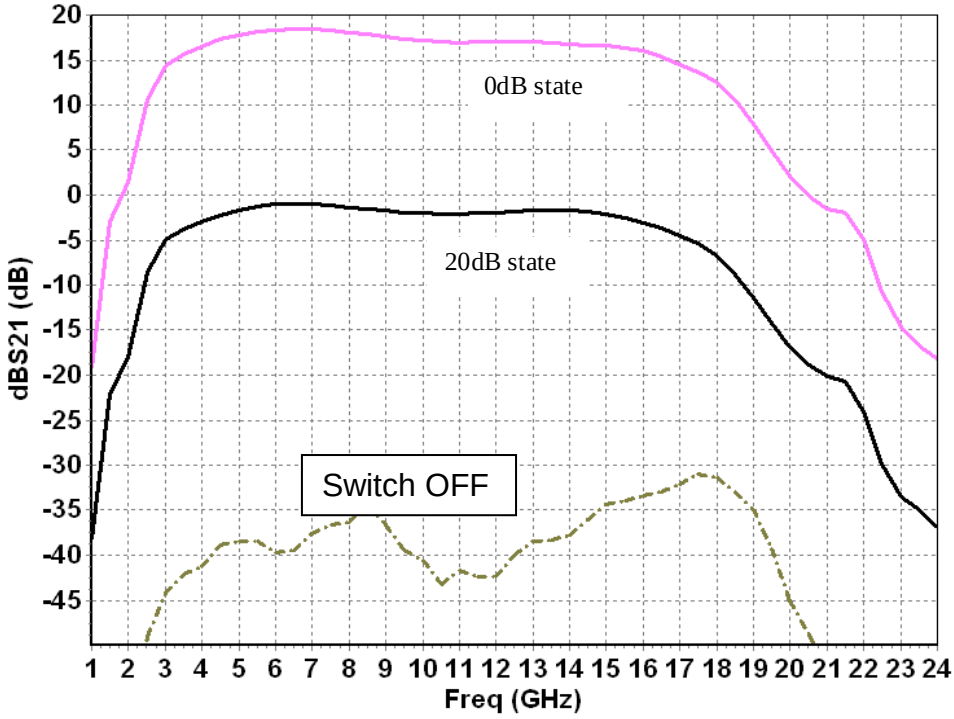
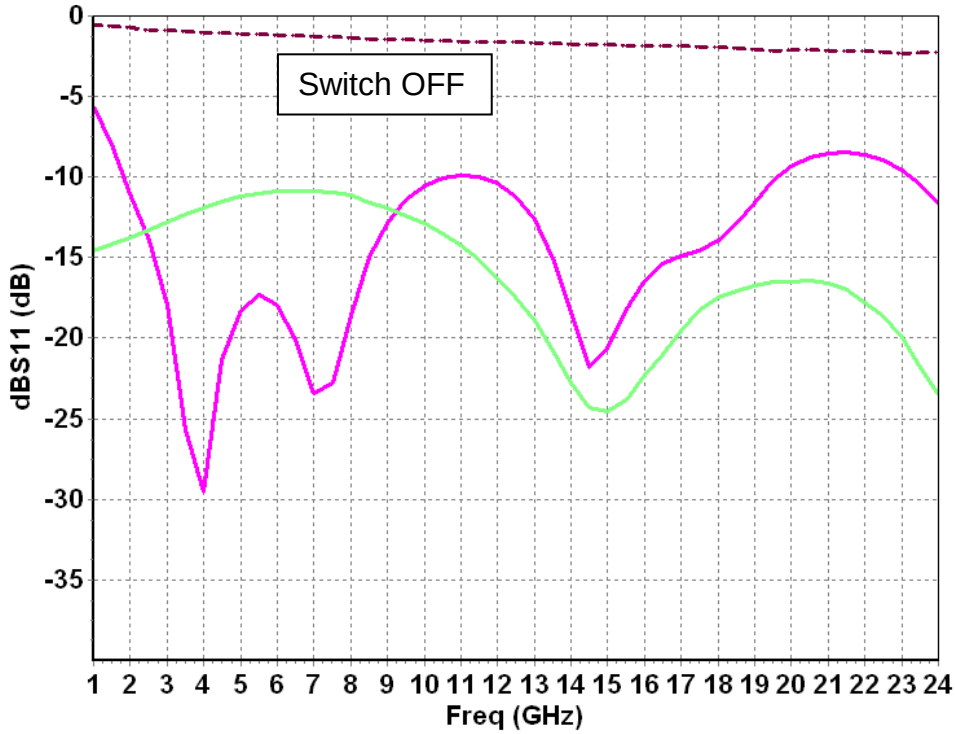
Typical test fixture Measurements @ 25℃

Bias conditions: Vd = 4.5V, Vg tuned for Id = 210mA



Linear Gain versus attenuation states



Input Return Loss versus attenuation states

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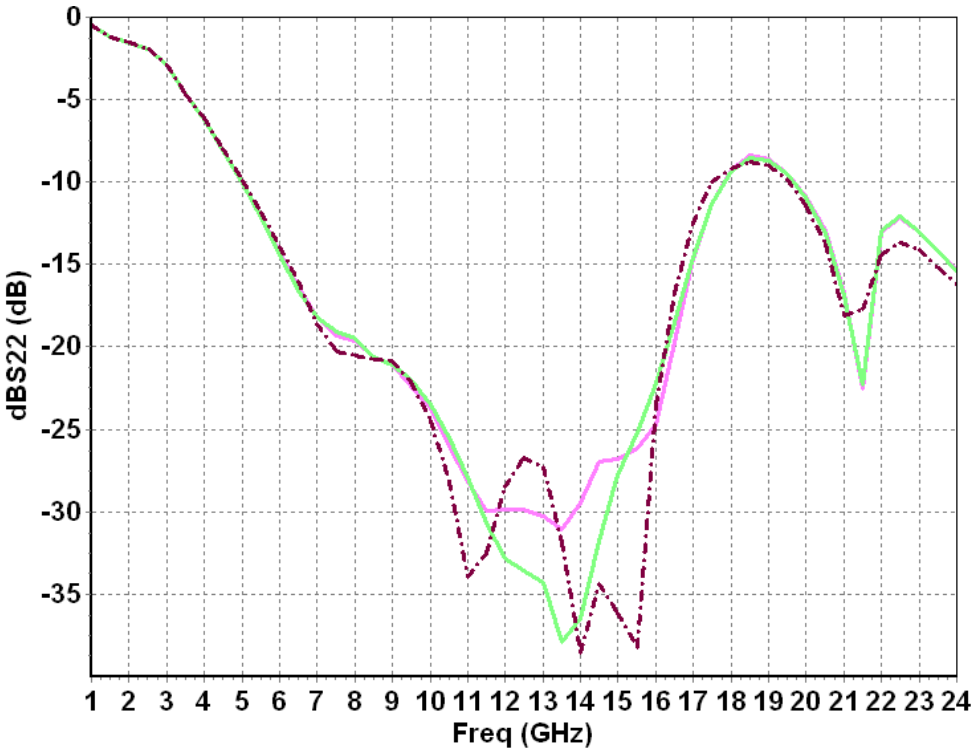

Output Return Loss versus attenuation states

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Typical Chip on wafer Sij parameters for reference state

Tamb = +25°C, Vd = +4.5 V, Id = 210 mA , 0dB state (20A = -5V, 20B = 0V).

Freq (GHz)	dB(S11)	P(S11) (°)	dB(S21)	P(S21) (°)	dB(S12)	P(S12) (°)	dB(S22)	P(S22) (°)
1.0	-5.5	-92.5	-20.7	161.9	-62.1	112.2	-0.5	-57.6
1.5	-8.0	-124.4	-2.7	69.1	-66.5	-40.1	-1.2	-85.9
2.0	-11.1	-149.5	0.3	94.1	-68.7	91.4	-1.5	-107.3
2.5	-13.9	-167.5	10.0	50.3	-64.9	14.8	-1.9	-132.8
3.0	-17.9	170.0	13.8	-2.9	-83.1	140.3	-2.8	-157.7
3.5	-25.6	167.5	15.6	-54.8	-87.8	39.6	-4.7	-175.7
4.0	-28.0	-112.8	16.3	-91.9	-73.1	116.8	-6.1	167.0
4.5	-20.8	-106.6	17.1	-127.4	-67.2	82.5	-8.0	152.1
5.0	-17.8	-121.1	17.6	-161.5	-63.8	57.4	-10.0	140.7
5.5	-16.9	-137.3	18.0	165.7	-61.5	22.6	-12.2	132.5
6.0	-17.4	-152.0	18.2	133.9	-60.0	-7.1	-14.5	127.7
6.5	-19.4	-161.4	18.3	103.0	-57.6	-33.7	-16.7	127.0
7.0	-22.7	-156.8	18.3	72.7	-56.5	-63.6	-18.7	129.8
7.5	-23.3	-123.6	18.2	43.1	-55.2	-89.9	-19.7	136.0
8.0	-19.3	-107.8	18.0	14.2	-54.0	-115.4	-20.2	140.3
8.5	-15.6	-107.5	17.8	-13.9	-53.6	-142.5	-21.1	137.2
9.0	-13.3	-118.9	17.5	-41.2	-53.7	-160.6	-21.5	132.1
9.5	-11.7	-131.3	17.3	-68.0	-52.6	-177.3	-22.9	127.6
10.0	-10.5	-147.0	17.1	-94.5	-51.6	153.2	-24.4	126.2
10.5	-10.2	-161.0	16.9	-120.6	-53.2	131.7	-26.5	125.0
11.0	-10.0	-174.3	16.9	-146.6	-53.3	114.2	-28.6	130.5
11.5	-10.1	172.0	16.9	-173.0	-53.7	99.0	-29.8	142.9
12.0	-10.4	157.6	17.0	159.8	-55.4	76.4	-29.7	148.2
12.5	-11.1	142.7	17.0	131.8	-59.3	61.7	-30.1	140.1
13.0	-12.4	125.9	17.0	102.9	-59.3	48.4	-32.0	109.0
13.5	-14.7	112.4	16.8	74.2	-62.4	-22.1	-34.9	37.3
14.0	-17.6	104.1	16.7	45.8	-59.0	-113.2	-29.6	-36.7
14.5	-20.9	107.6	16.6	16.4	-54.6	-169.8	-25.4	-71.4
15.0	-20.5	120.0	16.6	-14.5	-51.5	171.1	-24.5	-93.5
15.5	-18.4	113.6	16.4	-46.8	-48.0	149.4	-25.2	-99.5
16.0	-16.8	92.0	16.1	-80.4	-45.8	126.8	-25.9	-79.2
16.5	-15.7	63.4	15.5	-114.6	-43.8	100.8	-21.5	-60.8
17.0	-14.9	31.3	14.7	-148.5	-43.3	75.6	-15.9	-66.5
17.5	-14.5	2.8	14.0	175.9	-42.6	52.2	-12.2	-84.5
18.0	-13.8	-20.5	12.9	138.1	-42.4	25.5	-9.6	-106.7
18.5	-12.8	-39.8	11.3	98.1	-43.0	-5.1	-8.4	-131.5
19.0	-11.5	-57.4	8.9	59.2	-45.7	-39.8	-8.3	-154.4
19.5	-10.3	-75.6	6.0	23.7	-50.7	-77.9	-8.9	-174.8
20.0	-9.3	-93.4	3.2	-8.9	-60.5	-154.2	-10.2	167.0
20.5	-8.7	-110.5	0.8	-40.4	-57.9	108.5	-12.1	151.2
21.0	-8.4	-127.9	-0.9	-74.3	-50.5	78.2	-15.0	138.3
21.5	-8.4	-144.2	-1.8	-118.3	-47.7	52.1	-21.2	150.9
22.0	-8.6	-159.1	-3.7	176.5	-44.3	19.4	-15.1	-171.3
22.5	-8.9	-175.4	-8.9	108.2	-45.6	-14.4	-12.2	157.4
23.0	-9.5	167.6	-13.6	57.0	-47.3	-35.8	-12.7	134.3
23.5	-10.4	150.2	-16.4	15.7	-49.2	-46.6	-13.9	117.4
24.0	-11.6	130.5	-18.1	-17.7	-52.6	-62.7	-15.2	103.7

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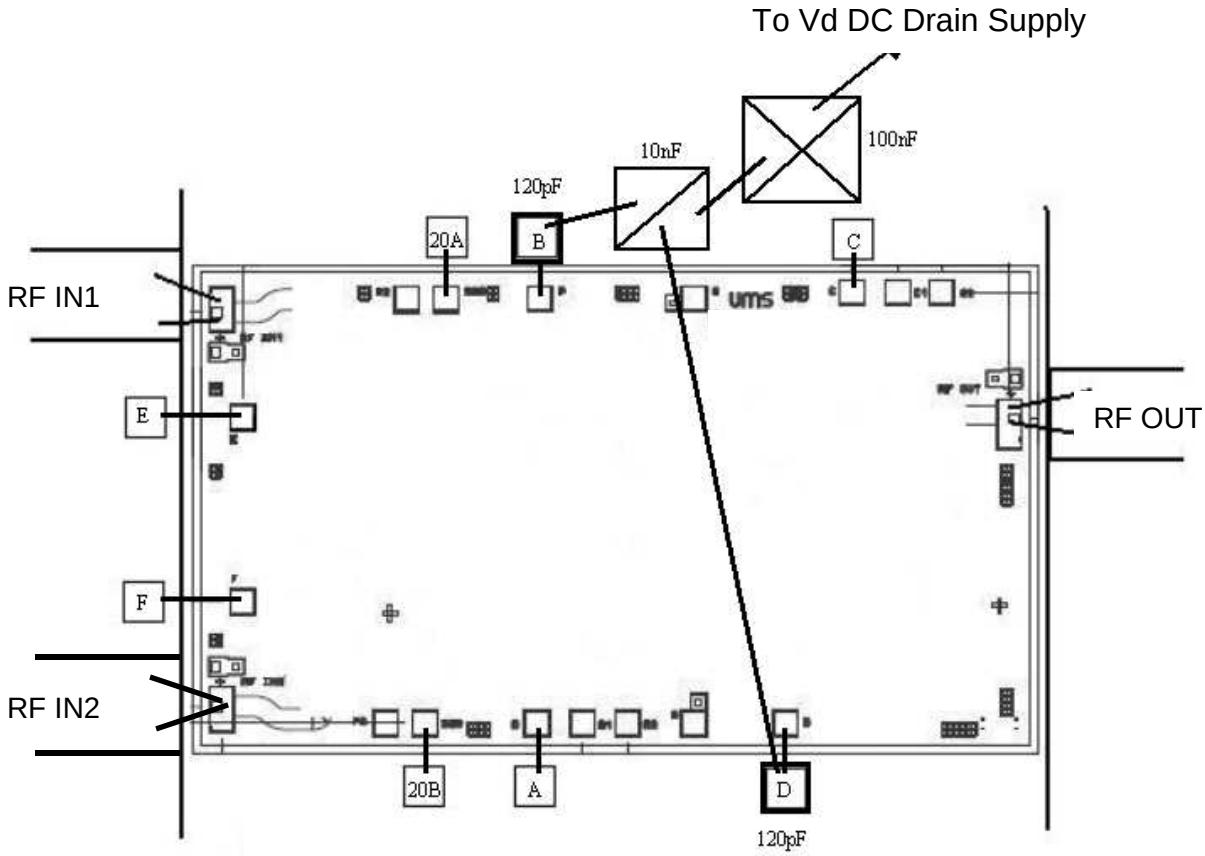
Chip Assembly and Mechanical Data



Note: RF wire bondings should be as short as possible, lower than 0.35mm.
25µm diameter gold wire is to be prefered.

Recommended circuit bonding table

Label	Type	Decoupling	Comment
20A, 20B	Vc	*Not required*	20dB attenuator control
B	**Vd**	**120pF / 10nF**	**Drain Supply**
D	**Vd**	**120pF / 10nF**	**Drain Supply**
A	Vg	*Not required*	Gate Supply
C	Vg	*Not required*	Gate Supply
E, F	Vc	*Not required*	Switch control

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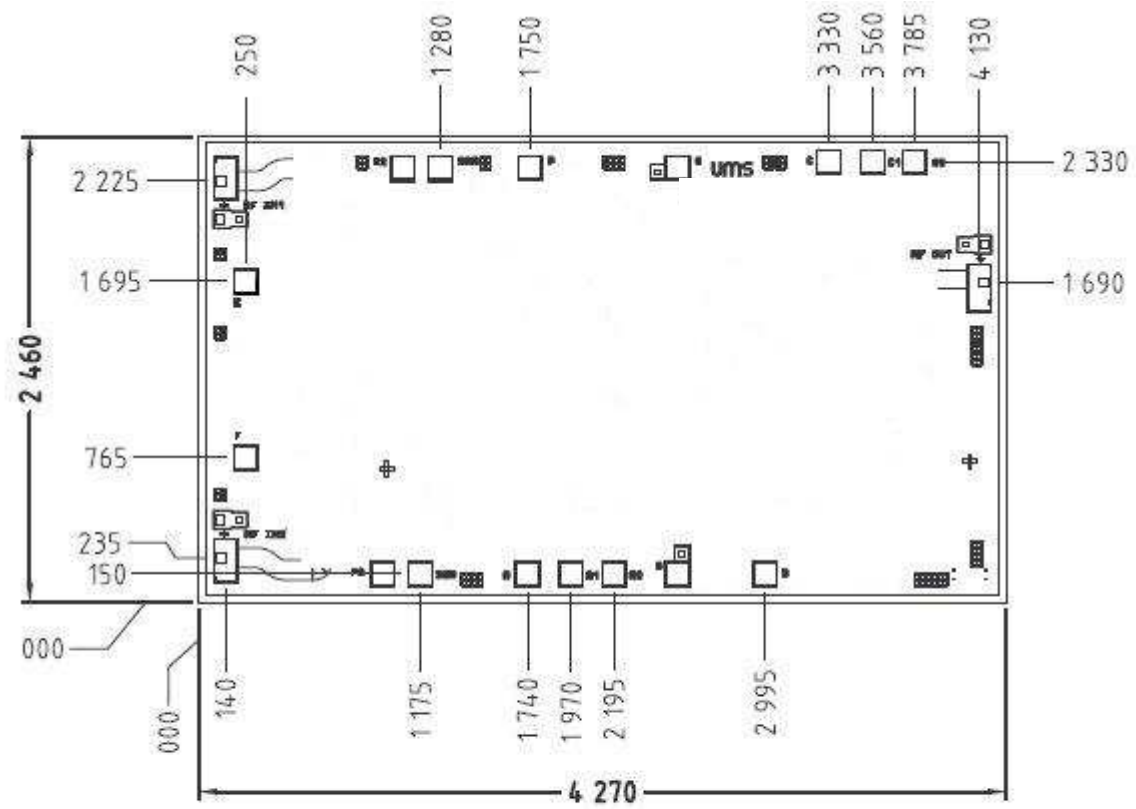
Bonding pad positions



Chip thickness: 100µm

UNITS : µm
Tol : ±35µm

Ordering Information

Chip form : CHA3512-99F/00

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