United Monolithic Semiconductors

CHA3397-QDG

36-40.5GHz Medium Power Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

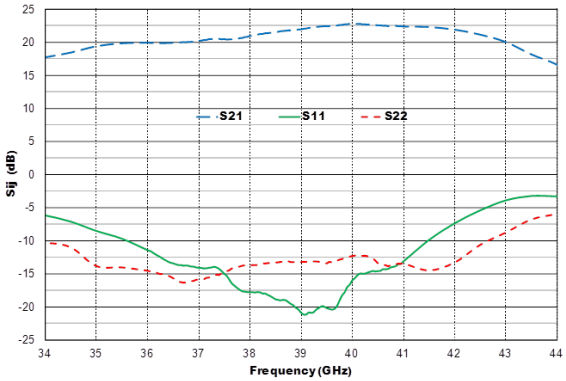
Description

The CHA3397-QDG is a 4 stage monolithic medium power amplifier, which produces 21dB gain for 18dBm output power.
It is designed for a wide range of applications, from military to commercial communication systems.
The circuit is manufactured with a pHEMT process, 0.15µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is supplied in RoHS compliant SMD package.

Main Features

- Broadband performances: 36-40.5GHz
- 18dBm Pout at 1dB compression
- 21dB gain
- 29dBm OTOI
- DC bias: Vd= 4.0V, Id= 200mA
- 24L-QFN4x4 (QDG)
- MSL1

Sij versus Frequency



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	36.0		40.5	GHz
Gain	Linear Gain		21		dB
P-1dB	Output Power @1dB comp.		18		dBm
OTOI	3rd order Intercept point		29		dBm

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Electrical Characteristics

Tamb.= +25°C, Vd = +4.0V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	36.0		40.5	GHz
Gain	Linear Gain		21		dB
ΔG	Gain variation in temperature		0.03		dB/°C
G_{CTRL}	Gain control range		15		dB
OTOI	3rd order Intercept point		29		dBm
P_{-1dB}	Output power @ 1dB		18		dBm
Psat	Saturated Output Power		20		dBm
RLin	Input Return Loss at max. gain		12		dB
RLout	Output Return Loss at min. gain		12		dB
NF	Noise figure		7		dB
Id	Quiescent Drain current		200		mA
Vg	Gate voltage		-0.4		V

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.5V	V
Id	Drain bias quiescent current	260	mA
Vg	Gate bias voltage	-2 to +0.4	V
Pin	Maximum input power	4	dBm
Tj	Junction temperature (2)	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
VG1	8	DC Gate voltage 1st stage	-0.4	V
VG2	9	DC Gate voltage 2nd stage	-0.4	V
VG3	10	DC Gate voltage 3rd stage	-0.4	V
VG4	11	DC Gate voltage 4th stage	-0.4	V
VD1	23	DC Drain voltage 1st stage	4.0	V
VD2	22	DC Drain voltage 2nd stage	4.0	V
VD3	20	DC Drain voltage 3rd stage	4.0	V
VD4	19	DC Gate voltage 4th stage	4.0	V

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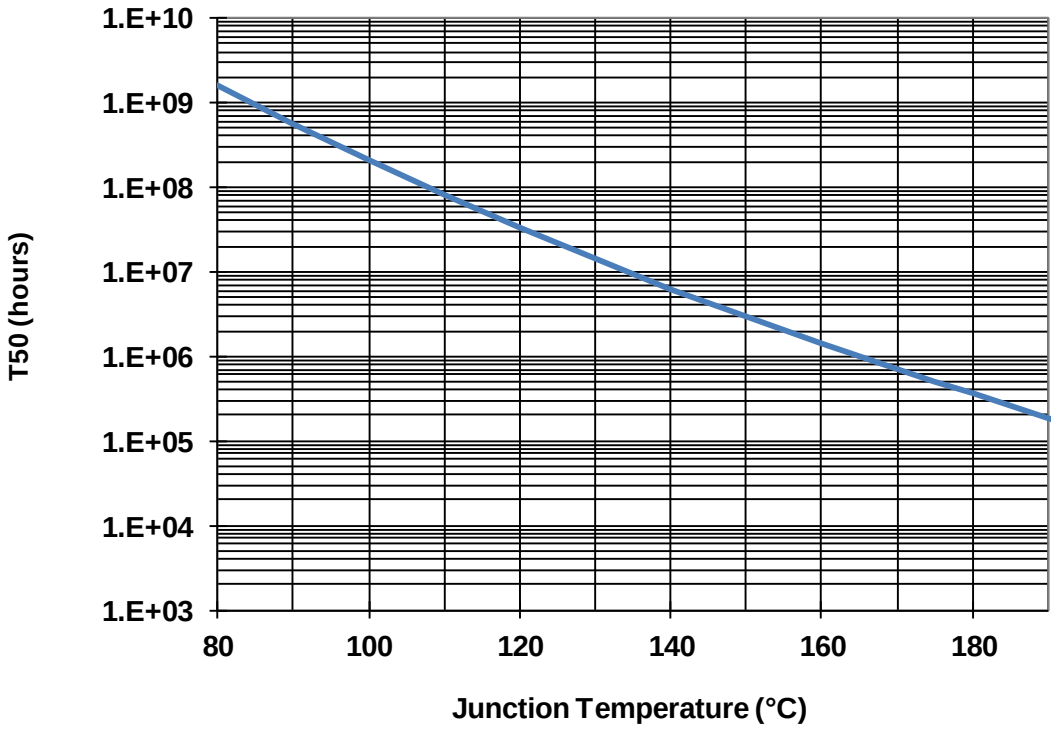
Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is only cooled down by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase).
The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.
So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} (1) Thermal Resistance (Junction to Case)	Vd= 4V Id= 200mA Pdiss= 0.8W	165	96.5	1.0E+6

(1) Assuming 85°C Tcase



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Typical Package Sij parameters

Tamb.= +25°C, Vd = +4V, Id = 200mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
5	-0.335	82.6	-69.526	-62.5	-65.971	-73.6	-3.268	21.5
6	-0.413	63.9	-68.420	60.0	-64.892	-133.7	-7.193	-31.5
7	-0.463	44.9	-61.512	32.2	-55.816	-167.6	-16.437	-128.1
8	-0.394	26.3	-57.907	-9.3	-47.932	148.3	-11.736	109.5
9	-0.382	7.4	-58.471	-39.8	-40.918	105.9	-8.050	61.3
10	-0.436	-12.4	-57.092	-74.1	-35.376	62.0	-6.820	27.5
11	-0.478	-32.3	-57.038	-103.4	-31.053	16.5	-6.420	-1.2
12	-0.541	-52.0	-57.361	-151.0	-27.810	-28.3	-6.414	-27.2
13	-0.586	-71.8	-57.982	-153.5	-24.912	-74.2	-6.757	-50.6
14	-0.586	-91.9	-48.470	164.3	-23.949	-124.8	-6.750	-70.8
15	-0.686	-111.7	-46.081	100.5	-24.796	-157.2	-6.786	-92.7
16	-0.570	-131.7	-49.794	69.1	-25.168	-167.5	-7.009	-114.5
17	-0.606	-151.6	-48.000	44.9	-20.955	-171.3	-7.253	-135.1
18	-0.512	-171.3	-45.192	7.5	-14.771	169.4	-7.630	-155.3
19	-0.525	167.3	-47.795	-20.7	-8.003	135.4	-8.029	-174.0
20	-0.892	144.7	-51.928	9.2	-1.700	87.2	-8.433	167.5
21	-1.753	124.9	-50.258	19.5	2.793	27.9	-8.785	149.7
22	-2.279	108.6	-47.556	-27.1	5.175	-31.3	-9.023	132.7
23	-2.365	91.7	-46.223	-20.1	6.755	-83.2	-9.210	116.4
24	-2.329	72.6	-44.742	-27.8	8.258	-132.6	-9.337	99.2
25	-2.411	51.7	-43.842	-36.8	9.676	178.6	-9.250	83.6
26	-2.721	30.6	-42.789	-50.5	10.940	128.9	-8.816	66.4
27	-2.983	11.3	-42.009	-62.7	11.653	82.0	-8.542	46.3
28	-3.122	-9.9	-42.229	-58.7	12.463	35.5	-8.597	27.1
29	-3.381	-30.3	-40.342	-65.3	13.241	-10.4	-7.819	8.7
30	-3.855	-51.3	-36.748	-100.5	13.330	-53.8	-7.903	-12.1
31	-4.525	-68.9	-37.164	-106.5	13.772	-91.7	-7.187	-30.6
32	-4.125	-88.5	-35.238	-114.3	16.795	-130.6	-7.267	-59.0
33	-4.695	-123.1	-34.385	-154.1	17.037	171.1	-10.241	-79.9
34	-6.143	-152.4	-35.287	-169.6	17.722	131.3	-10.290	-88.5
35	-8.504	171.2	-35.005	172.4	19.395	83.5	-13.787	-110.4
36	-11.408	130.8	-35.560	164.4	19.913	29.7	-14.494	-114.9
37	-14.094	95.4	-34.322	142.5	20.233	-18.0	-15.874	-116.5
38	-17.804	59.6	-35.296	107.2	20.949	-66.4	-13.676	-139.9
39	-20.895	47.2	-37.664	83.2	21.949	-120.7	-13.183	169.1
40	-15.997	76.8	-39.666	54.1	22.786	179.7	-12.257	107.5
41	-13.126	67.6	-45.973	16.4	22.380	118.0	-13.371	58.9
42	-7.345	54.6	-48.829	-110.6	21.912	52.9	-13.244	53.3
43	-3.874	26.8	-41.305	178.7	20.032	-17.9	-8.712	44.4
44	-3.274	0.8	-40.410	130.8	16.601	-84.0	-5.856	23.3

Refer to the paragraph “Definition of the Sij reference planes”

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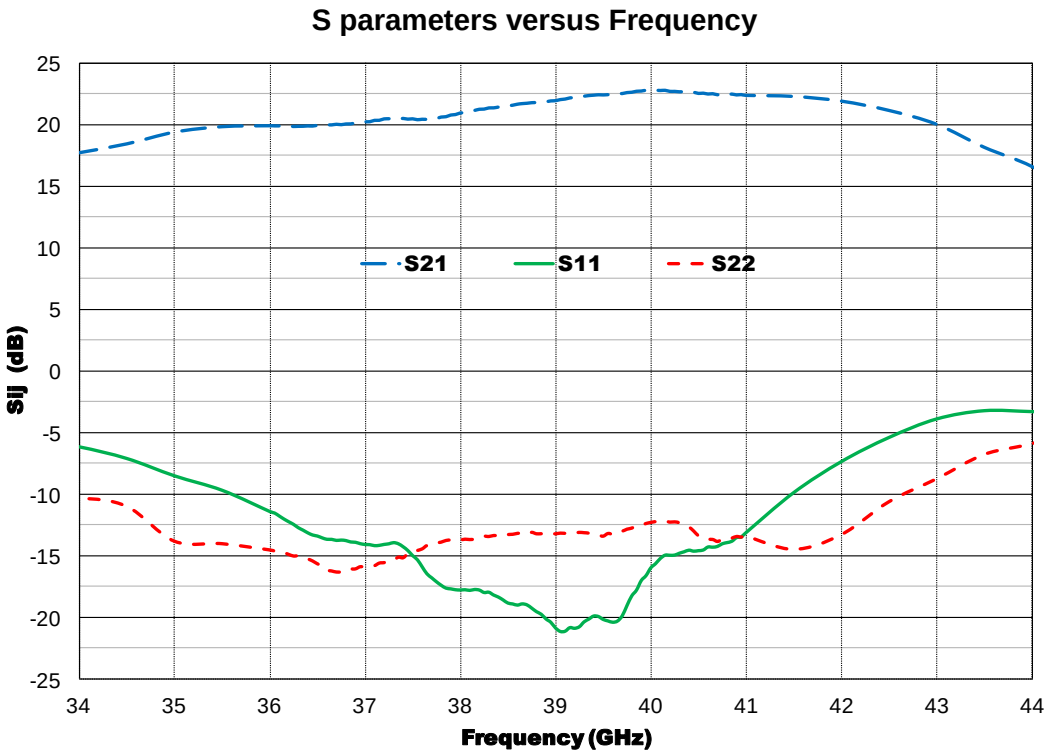
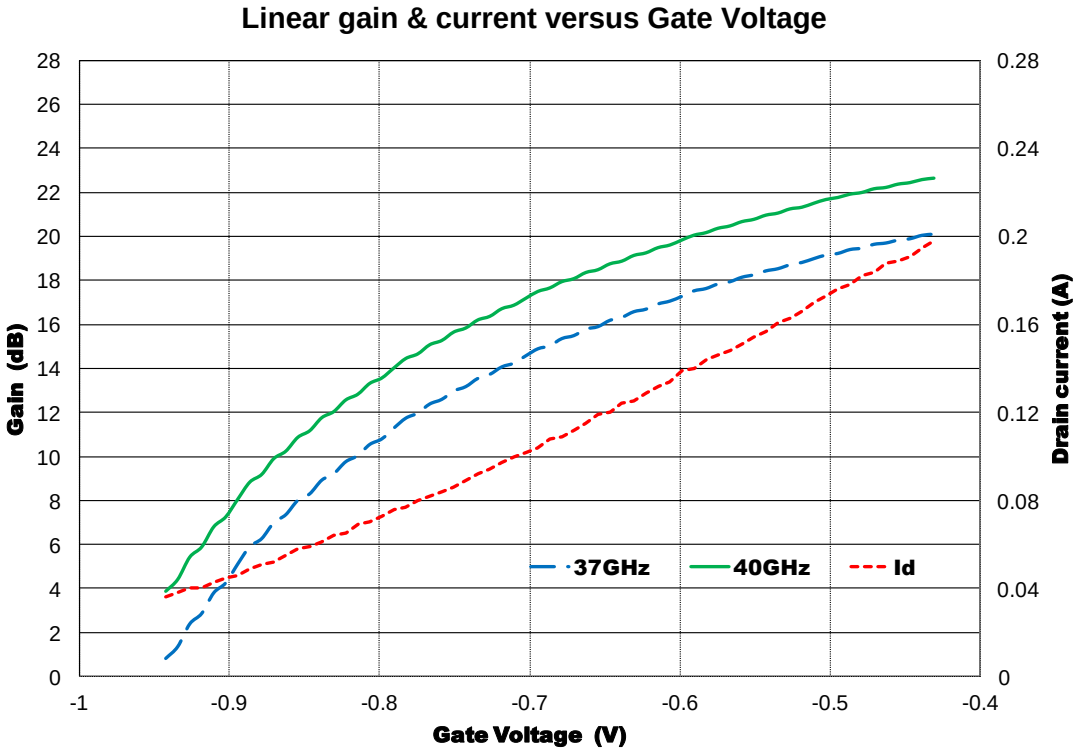
Typical Board Measurements

Tamb.= +25°C, Vd = +4.0V, Id = 200mA
These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".





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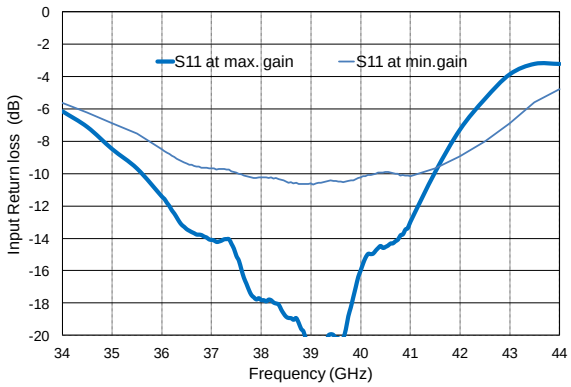
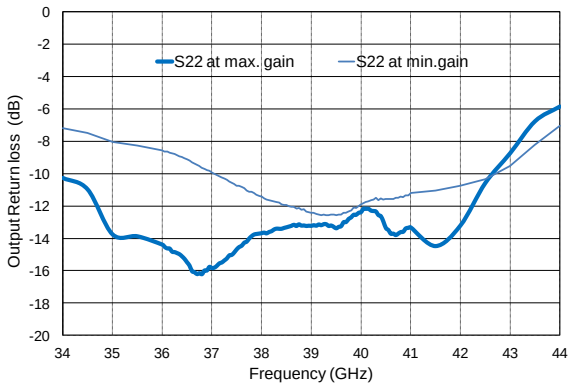
Typical Board Measurements

Tamb.= +25°C, Vd = +4.0V, Id = 200mA

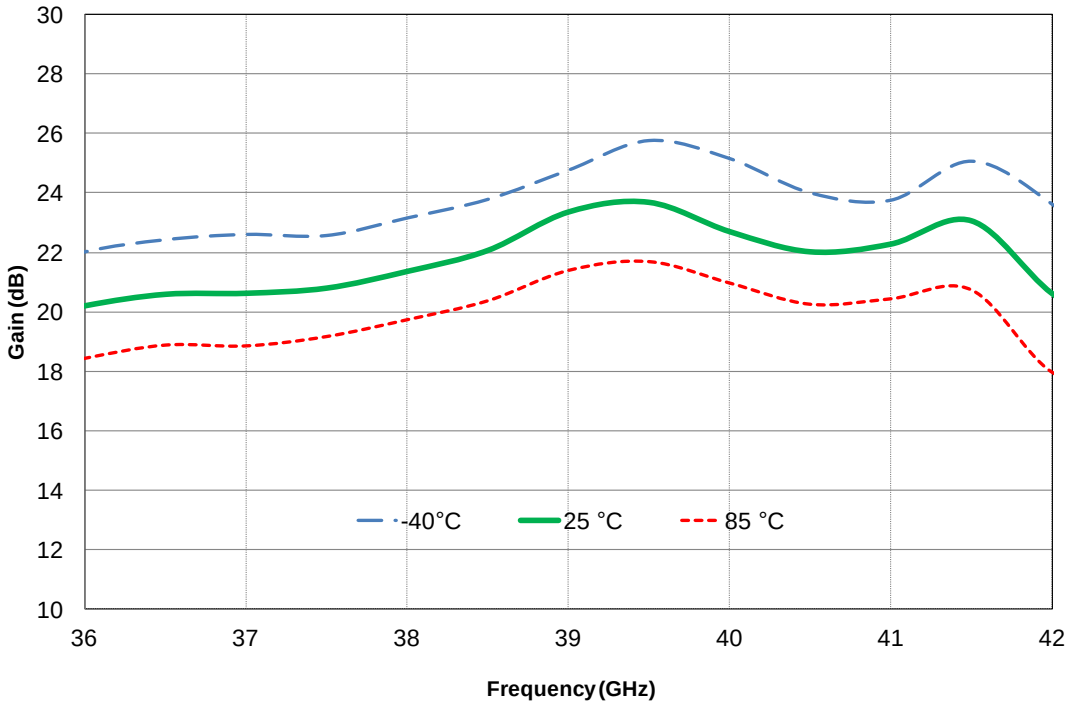
Input return loss versus gain ctrl



Output return loss versus gain ctrl



Linear gain versus Temperature



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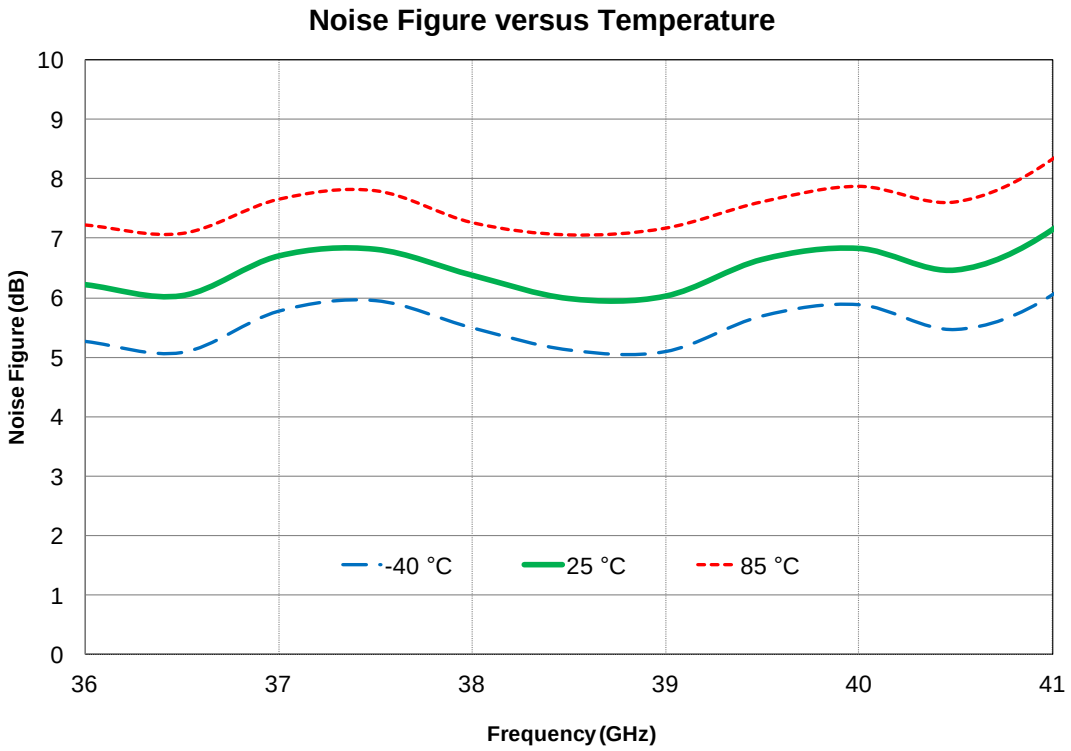
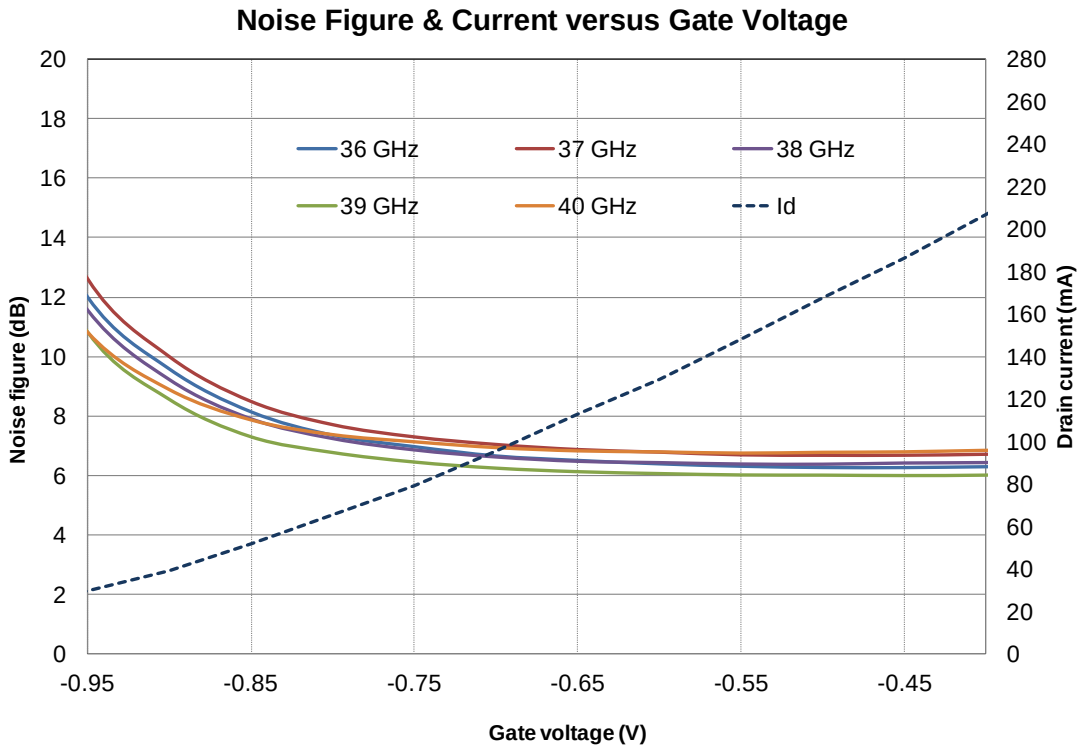
Typical Board Measurements

Tamb.= +25°C, Vd = +4.0V, Id = 200mA





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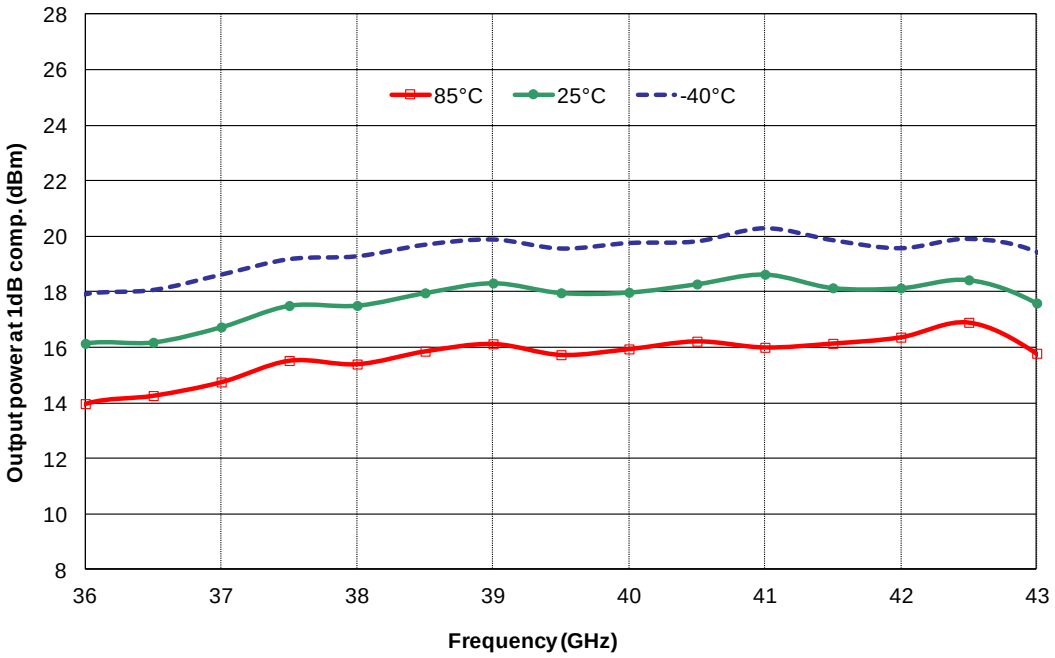
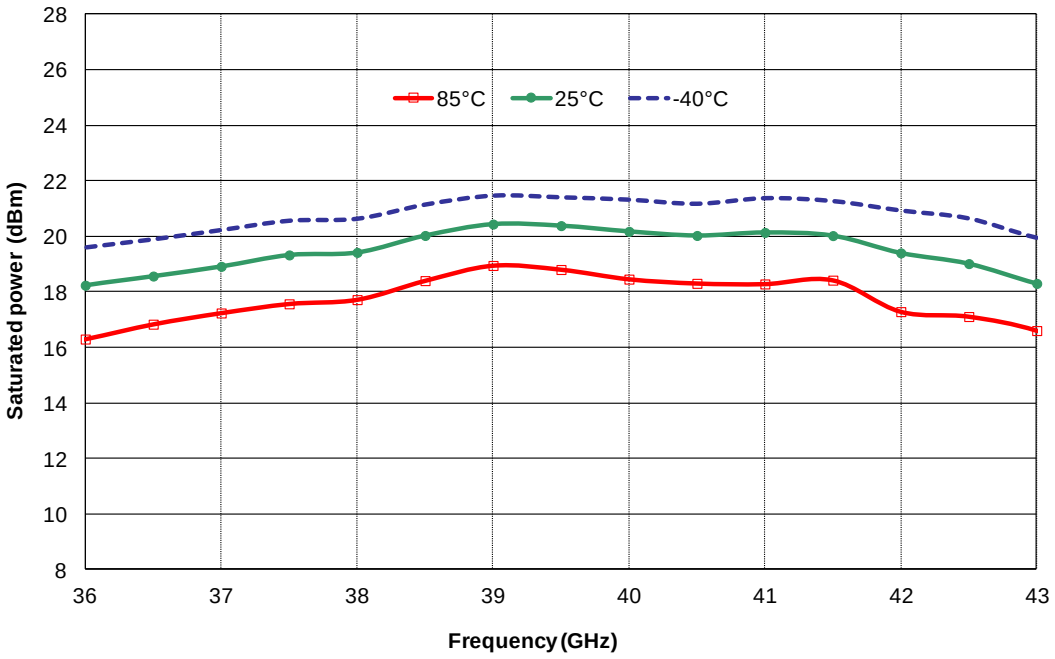
Typical Board Measurements

Tamb.= +25°C, Vd = +4.0V, Id = 200mA

Output Power at 1dB comp. versus Temperature



Saturated Power versus Temperature



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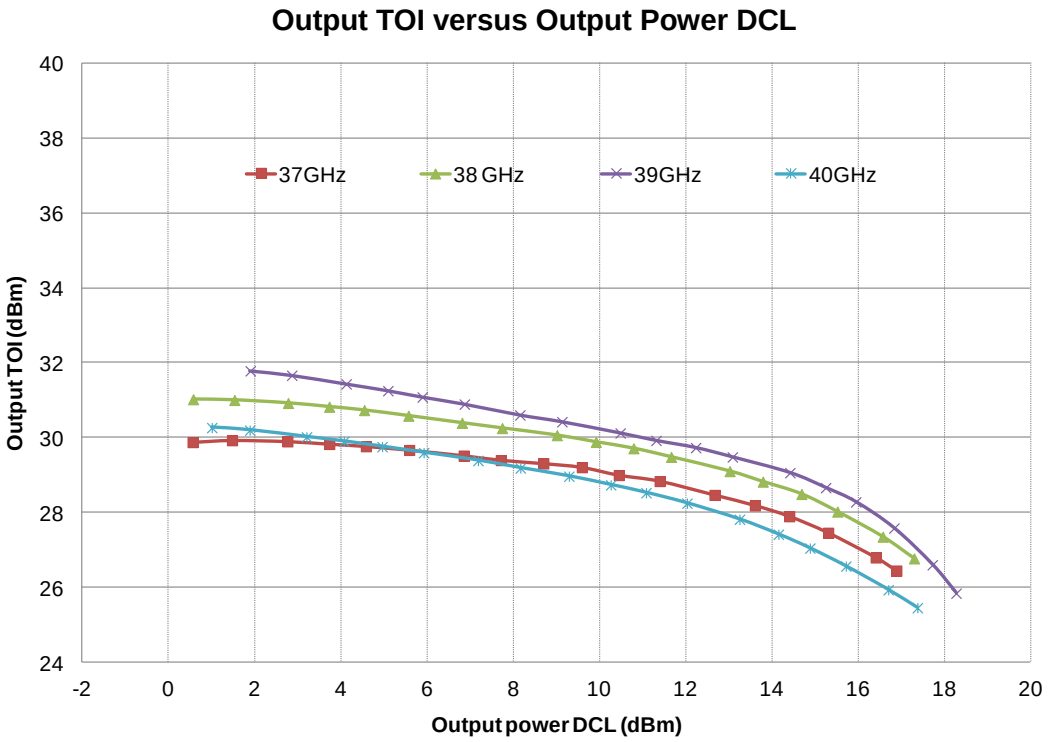

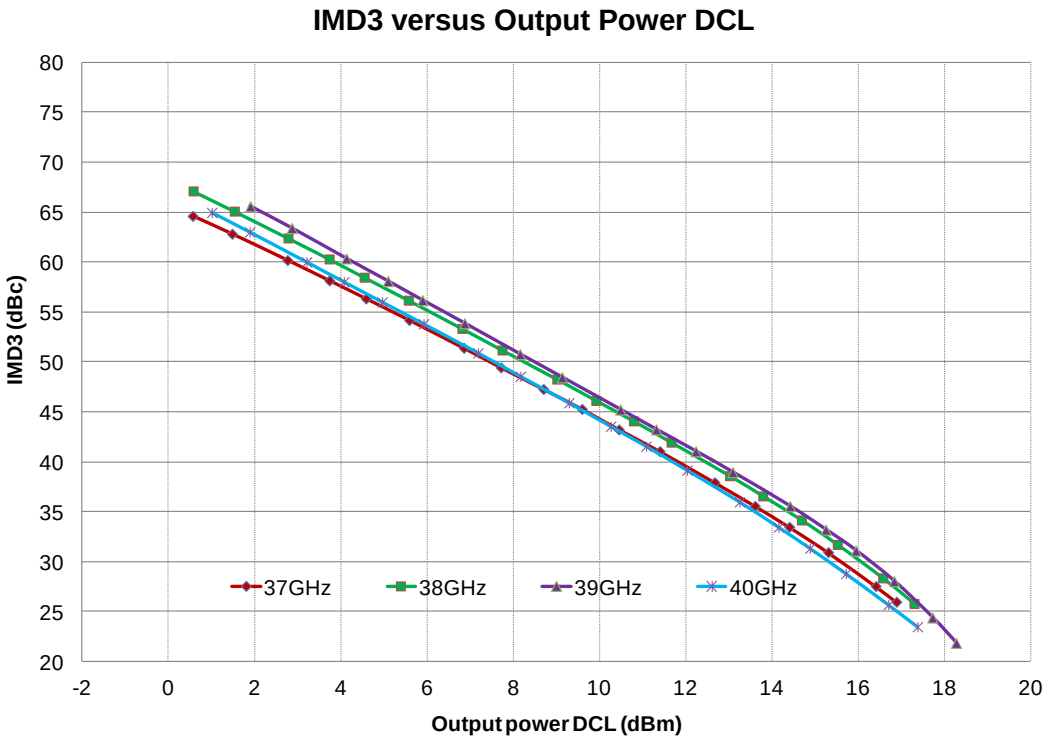

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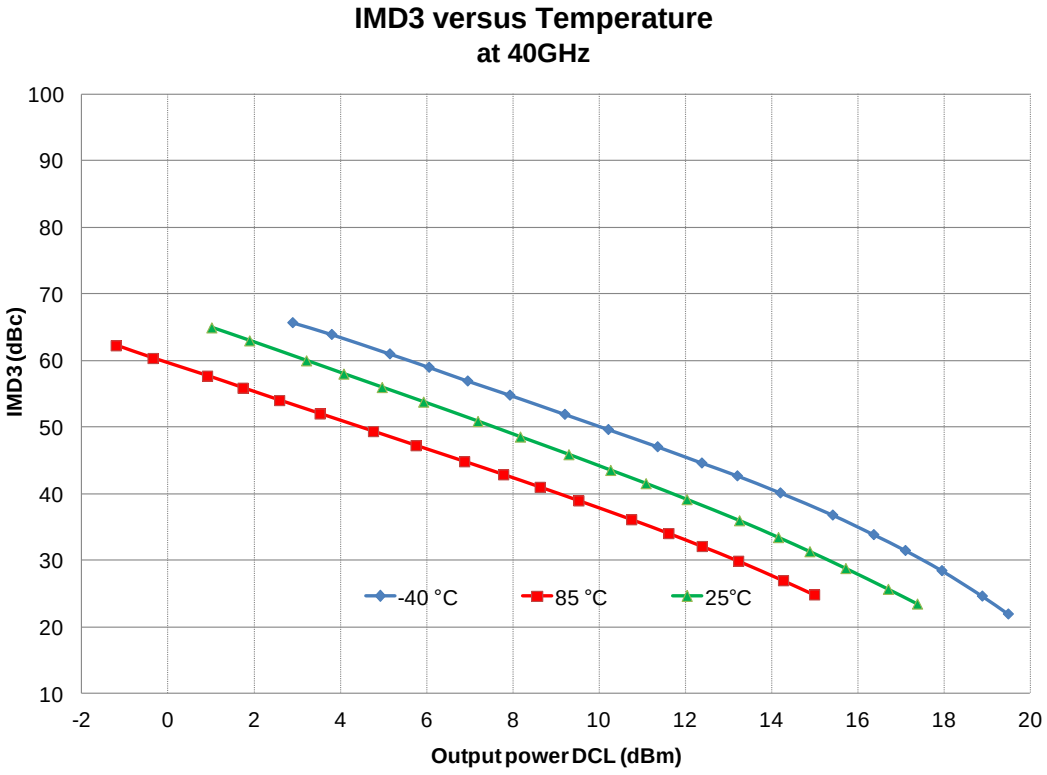

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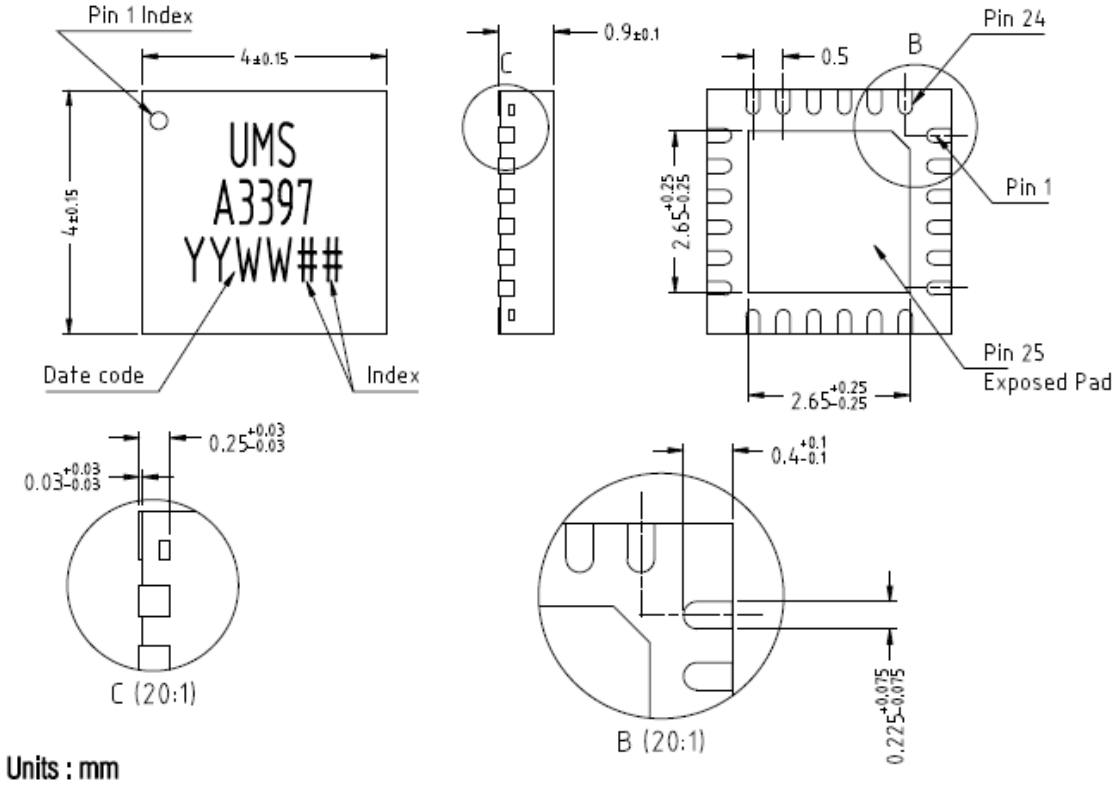
Package outline (1)



Matte tin, Lead Free (Green)		1- NC	9- Vg2	17- Gnd(2)
Units :	mm	2- Gnd(2)	10- Vg3	18- NC
From the standard :	JEDEC MO-220 (VGGD)	3- Gnd(2)	11- Vg4	19- Vd4
		4- RF IN	12- NC	20- Vd3
25- GND		5- Gnd(2)	13- Gnd(2)	21- Gnd
		6- Gnd(2)	14- Gnd(2)	22- Vd2
		7- NC	15- RF OUT	23- Vd1
		8- Vg1	16- Gnd(2)	24- NC

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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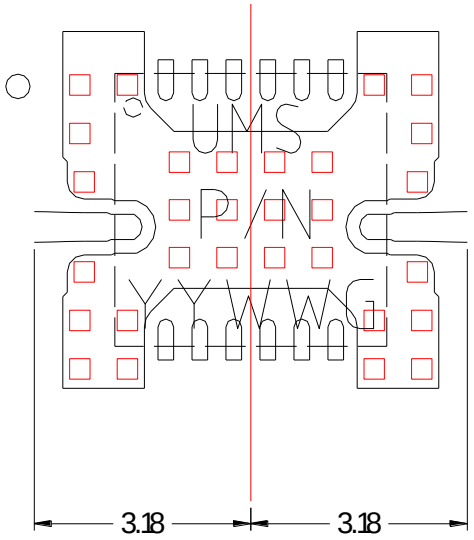
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".

Sij measurements are made in probes configuration with a dedicated board, without RF connectors.



ESD sensitivity

Standard	Value
MIL-STD-1686C	HBM Class 1
ESD STM5.1-1998	HBM Class 1B

Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte tin (Sn)
MSL Rating	MSL1

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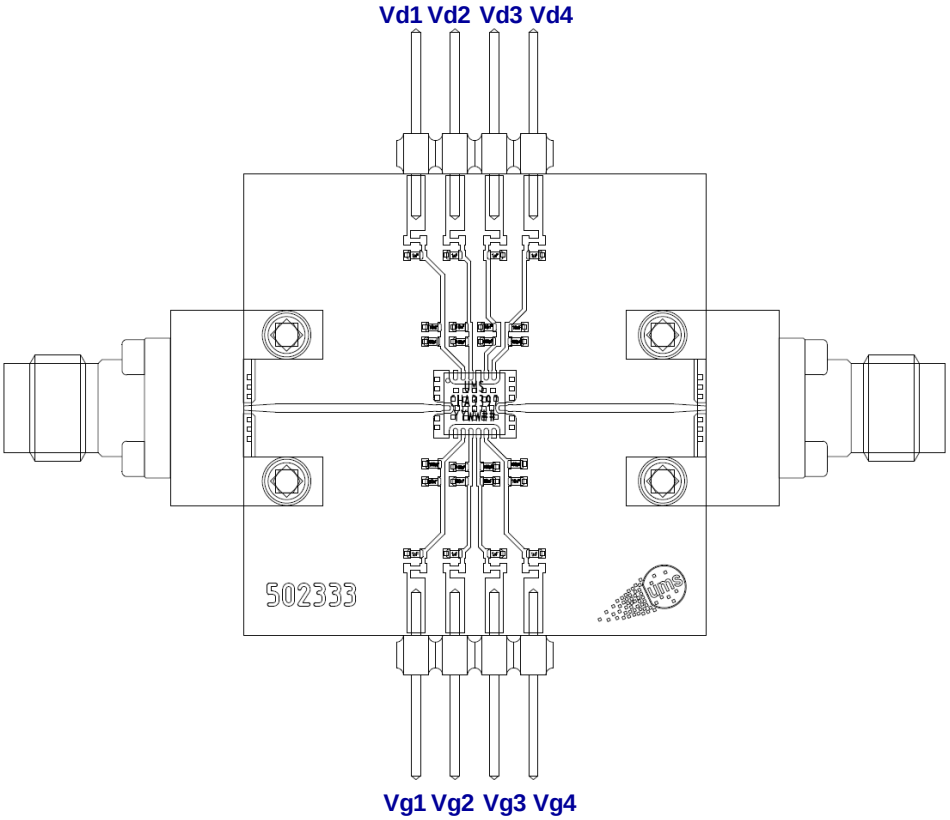
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4350 / 10mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF ±5% and 10nF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.



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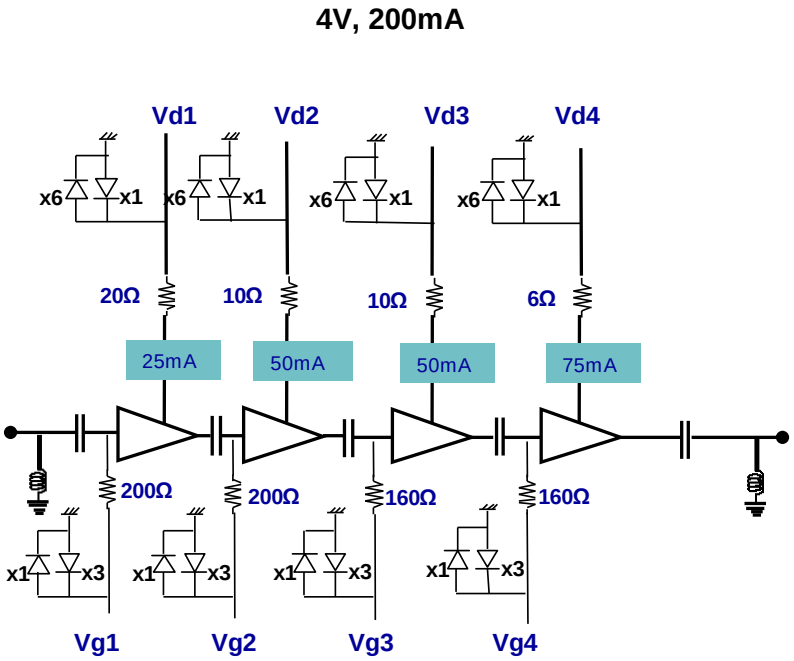
Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.

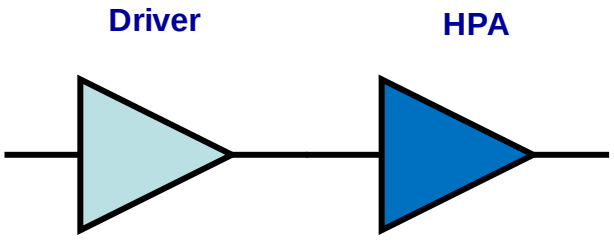
ESD protections are also implemented on all DC accesses.
The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package.

DC Schematic



Recommended UMS Power chain

The CHA6194-QXG could be associated with the CHA3397-QDG as driver.
Total Gain: 41dB
Gain control: 30dB with the two amplifiers.



CHA3397-QDG	CHA6194-QXG
36- 40.5GHz	37- 40GHz
4V, 200mA	6V, 800mA

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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 package:	CHA3397-QDG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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