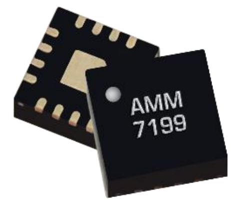
11-38 GHz GaAs Surface Mount LO Driver Amplifier AMM-7199SM

1. Device Overview

1.1 General Description

The AMM-7199SM is a surface-mount amplifier suitable for use as a single tone driver or general-purpose gain block. It can drive an L or H diode mixer from 11 to 38 GHz, or S diode mixer from 16 to 34 GHz. This amplifier also has exceptionally low input and output reflections, and excellent gain flatness in-band. The AMM-7199SM is packaged in a compact 3mm QFN for surface mount integration onto printed circuit boards.



Surface Mount QFN

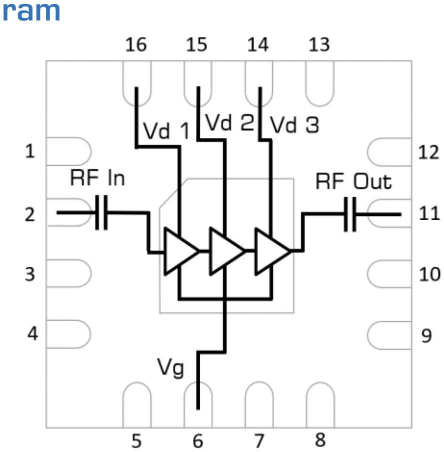
1.2 Features

- +21 dB Small Signal Gain
- +21 dBm saturated output power
- Excellent return losses
- Compact 3mm QFN package
- .s2p S-Parameters: EVAL-AMM-7199SM.s2p

1.3 Applications

- Mobile test and measurement equipment
- Radar and satellite communications
- 5G transceivers
- LO driver for Marki L-, H-, and S-diode mixers

1.4 Functional Block Diagram



1.5 Part Ordering Options[1]

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
AMM-7199SM	3x3 mm Surface Mount	QFN	**RoHS**	Active	3A001.b.2.d
EVAL-AMM-7199SM	Connectorized Evaluation Fixture	EVAL	**RoHS**	Active	EAR99

[1] Refer to our website for a list of definitions for terminology presented in this table.

Table of Contents

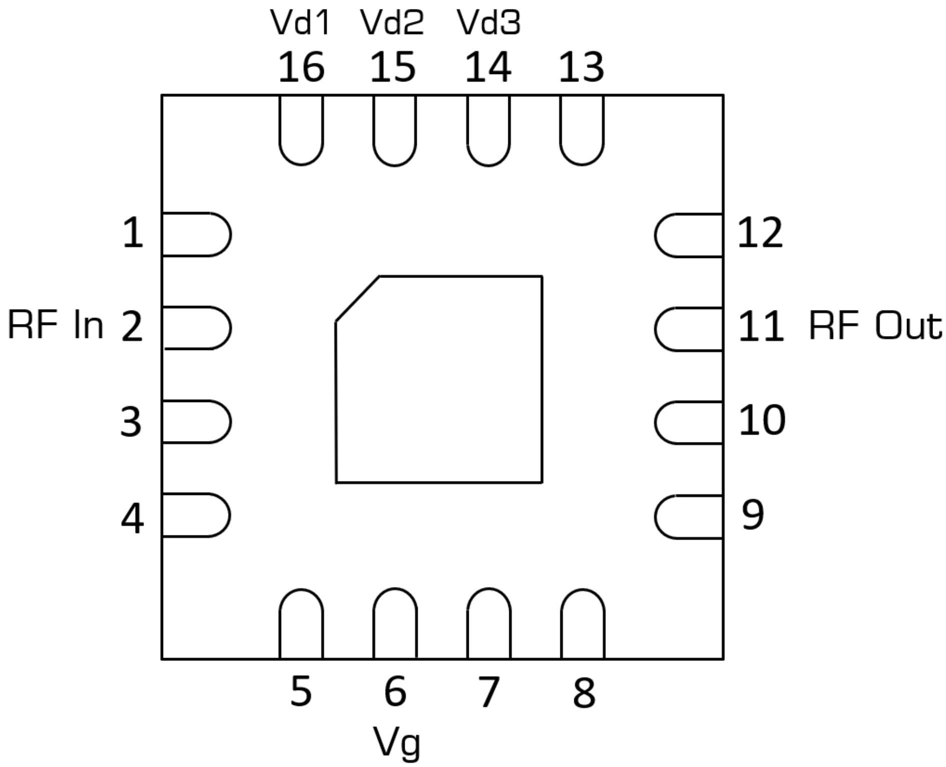
Revision History

Revision Code	Revision Date	Comment
-	May 2021	Datasheet Initial Release

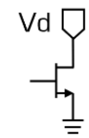
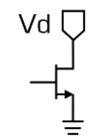
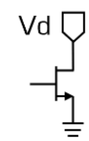
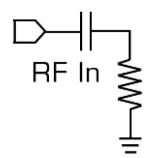
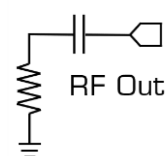
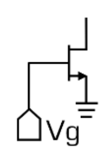
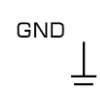
2. Port Configurations and Functions

2.1 Port Diagram

A port diagram of the AMM-7199SM's QFN package is shown below. The pin functions are detailed in section 2.2 of this datasheet.



2.2 Port Functions

Port	Function	Description	Equivalent Circuit for Package
Pin 14[2]	Positive DC Supply V_d	Pins 14 provides +2.5V to +4V DC voltage to the amplifier's third stage. Negative voltage must be supplied to Pin 6 before turning on the positive supply voltage.	
Pin 15[2]	Positive DC Supply V_d	Pins 15 provides +2.5V to +4V DC voltage to the amplifier's second stage. Negative voltage must be supplied to Pin 6 before turning on the positive supply voltage.	
Pin 16[2]	Positive DC Supply V_d	Pins 16 provides +2.5V to +4V DC voltage to the amplifier's first stage. Negative voltage must be supplied to Pin 6 before turning on the positive supply voltage.	
Pin 2	RF Input	Pin 2 is the RF input of the amplifier, and is matched to 50 ohms. It is internally DC blocked.	
Pin 11	RF Output	Pin 11 is the RF output of the amplifier, and is matched to 50 ohms. It is internally DC blocked.	
Pin 6[3]	Negative DC Supply V_g	Pin 6 provides -0.4V to -0.6V of DC voltage. This must be turned on before turning on the positive supply voltage to Pin 1.	
GND	Ground	Ground paddle and non-connected pins must be connected to a DC/RF ground potential with high thermal and electrical conductivity, and low inductance.	

[2] Pins 14, 15, and 16 may be biased together for ease of use, or individually to adjust overall performance

[3] Pin 6 may be biased with constant DC voltage, or actively biased to produce a fixed Id for consistent performance.

3. Specifications

3.1 Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may be inoperable or have a reduced lifetime. This amplifier is designed and characterized in a 50Ω system, and operation in a reflective environment can cause performance degradation.

Parameter	Maximum Rating	Units
Positive Drain Supply Voltage (Pin 14, 15, 16)	4.5	V
Negative Bias Voltage (Pin 6)	-2	V
RF Input Power	+20	dBm
Positive Drain Supply Current[4] (with RF Input)	450	mA
Operating Temperature	-40 to +85	°C
Storage Temperature	-65 to +150	°C
Thermal Resistance, θ_{JC}	94	°C/W
Continuous Power Dissipation (P_{DISS}) (at 85 °C case temp.)[5]	1	W
Max Junction Temperature for MTTF > 1E6 hours	175	°C

3.2 Package Information

Parameter	Details	Rating
Weight	EVAL Package	31.2g

[4] Positive Drain Supply DC current is specified as $Id_1 + Id_2 + Id_3$
[5] Derates by 11 mW/ °C above 85 °C case temperature.

3.3 Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications (3.5). Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the Electrical Specifications. For limits, above which damage may occur, see Absolute Maximum Ratings (3.1).

Parameter	Min	Nominal	Max	Units
T_A, Ambient Temperature	-40	+25	+85	°C
Power Supply DC Voltage	+2.5	+3	+4	V
Power Supply DC Current[6]	115	180	300	mA
Gate Bias DC Voltage	-0.6	-0.5	-0.4	V
Input Power for Saturation	+3	+6	+8	dBm

3.4 Sequencing Requirements

Turn-on Procedure:

1) Apply Vg (Pin 6)
2) Apply Vd (Pin 14, 15, 16)

Turn-off Procedure:

1) Turn off Vd (Pin 14, 15, 16)
2) Turn off Vg (Pin 6)

Note: RF input power can be injected at any moment in the bias sequencing procedure.

[6] Power Supply DC current is specified as $Id_1 + Id_2 + Id_3$

3.5 Electrical Specifications[7]

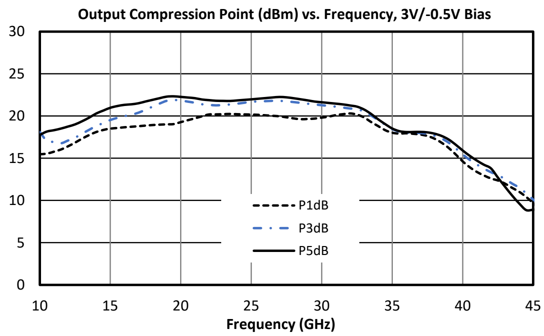
The electrical specifications apply at T_A=+25°C in a 50Ω system.

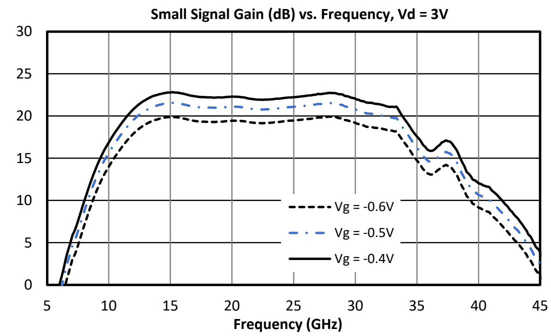
QFNs are 100% RF tested.

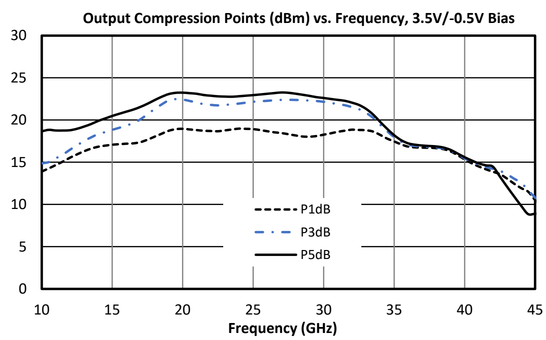
Parameter	Test Conditions	Frequency	Min	Typical	Units
Saturated Output Power[8]	3V/-0.5V bias	11 GHz – 15 GHz		+19	dBm
		15 GHz – 30 GHz	+17	+21	
		30 GHz – 38 GHz		+19	
Small Signal Gain	3V/-0.5V bias, -25 dBm Input Power	11 GHz – 15 GHz		20	dB
		15 GHz – 30 GHz	17	21	
		30 GHz – 38 GHz		17	
Input Return Loss		11 GHz – 38 GHz		16	
Output Return Loss		11 GHz – 38 GHz		13	
Reverse Isolation		11 GHz – 38 GHz		53	
Noise Figure	3V/-0.5V Bias	11 GHz – 38 GHz		5	
Drain Current[9], Id	3V/-0.4V	-		230	mA
	3V/-0.5V	-		180	
	3V/-0.6V	-		130	
Input IP3 (IIP3)	3V/-0.5V bias, -20 dBm Input Power	11 GHz – 38 GHz		+11	dBm
Output IP3 (OIP3)		11 GHz – 38 GHz		+29	
Output P_{1dB}	3V/-0.5V bias	11 GHz – 38 GHz		+19	
Input Power for Saturation	3V/-0.5V bias	11 GHz – 38 GHz		+6	dBm

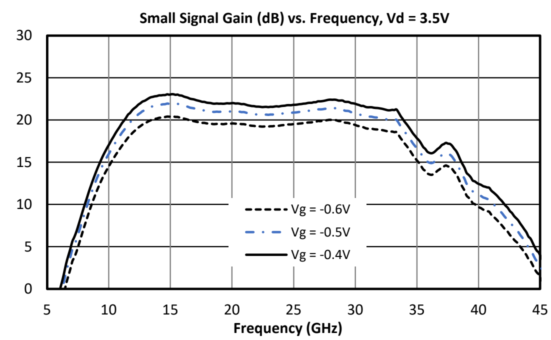
[7] Evaluation board losses are mathematically extracted from Saturated output power, Small signal gain, and Noise figure specifications.
[8] Saturated output power specification defined using the EVAL-APM-7199SM P_{5dB} compression curve shown in section 3.6, with board losses mathematically extracted.
[9] Bias conditions for Id tested with no RF input power. See section 3.6 for DC current vs. RF power. Bias conditions presented as Vd/Vg. Drain current is specified as $Id_1 + Id_2 + Id_3$

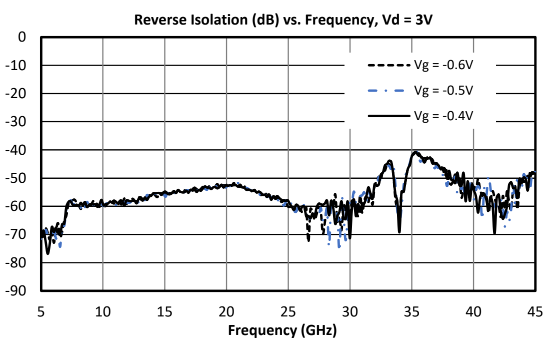
3.6 Typical Performance Plots[10] [11]

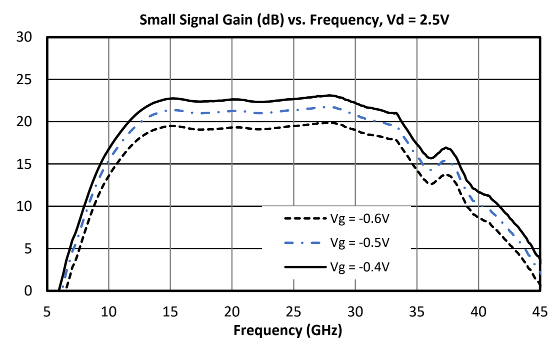


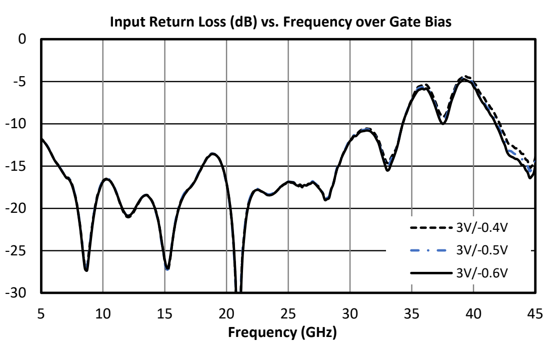


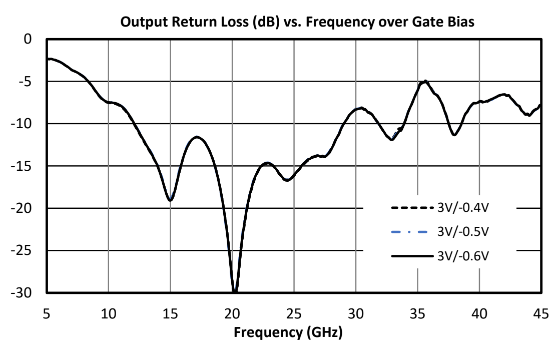












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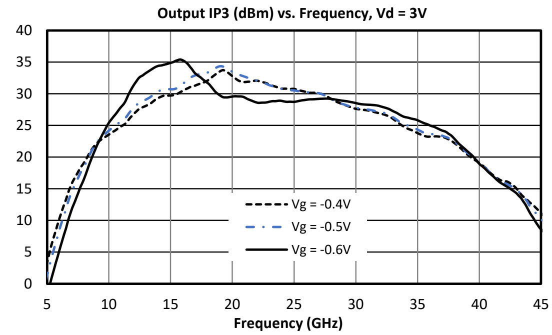
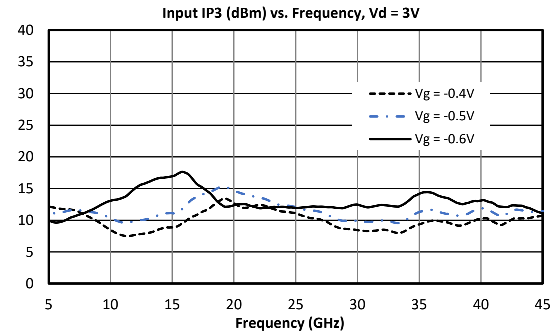
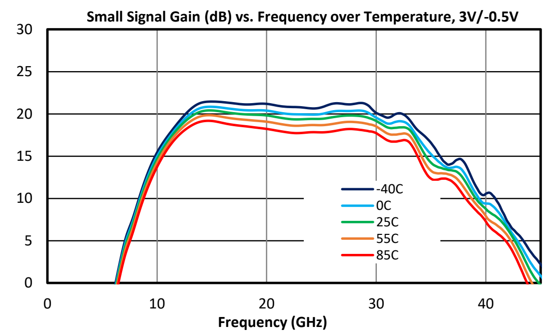
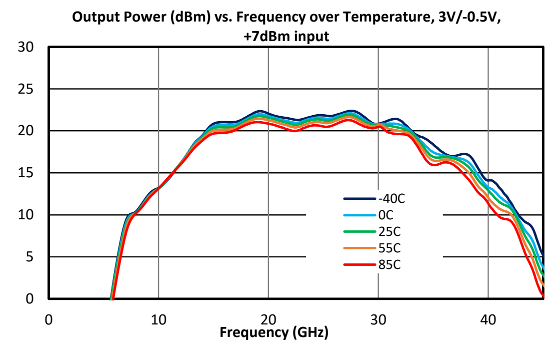
[10] Measurement data taken using the EVAL-AMM-7199SM module.

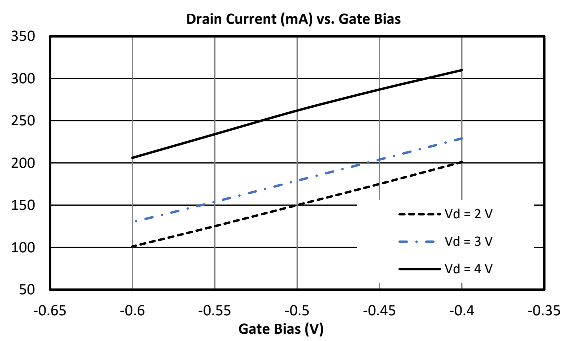
[11] Evaluation board losses are mathematically extracted out of Output Compression Curves, Small Signal Gain Plots, and Noise Figure plots. All other plots include evaluation board losses.

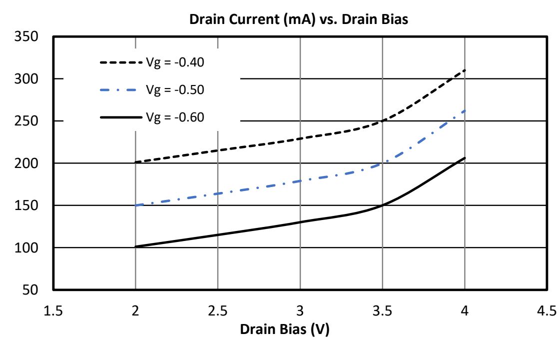


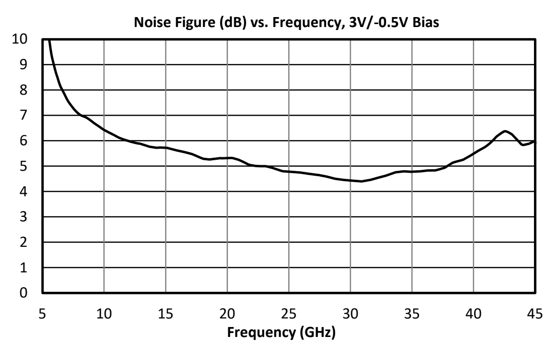


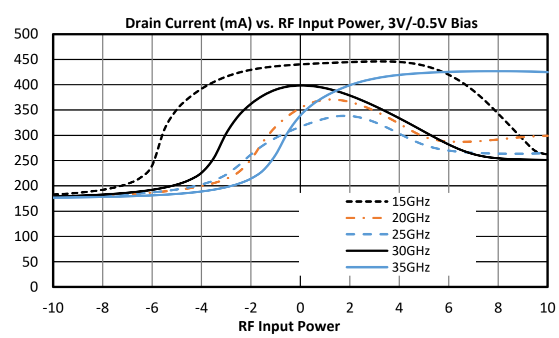












[13]

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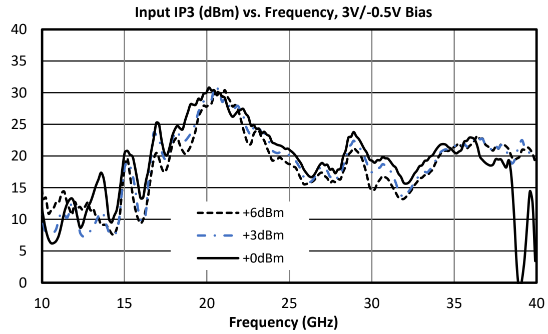
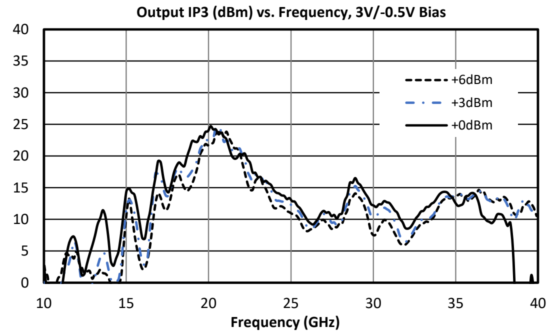
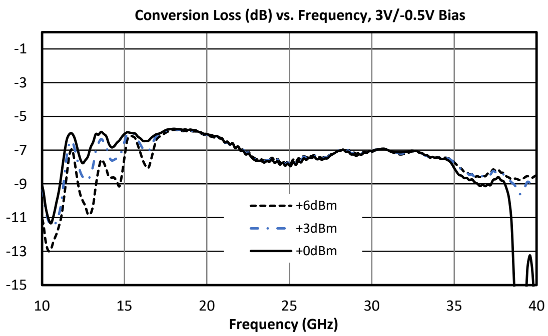
[13] Drain current is specified as $Id_1 + Id_2 + Id_3$

3.7 Typical Performance Plot of Marki MM1-1140H Using AMM-7199SM as LO Driver[14]







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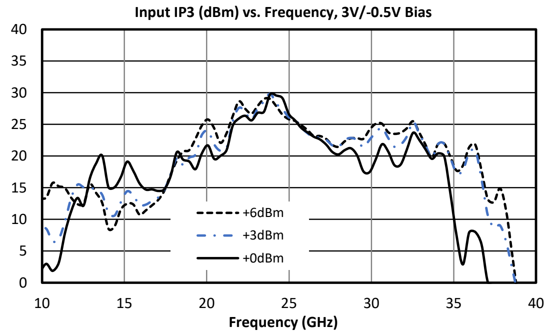
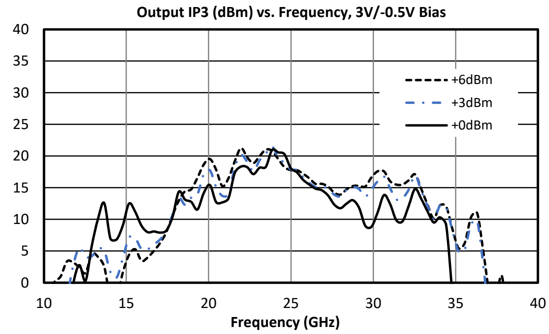
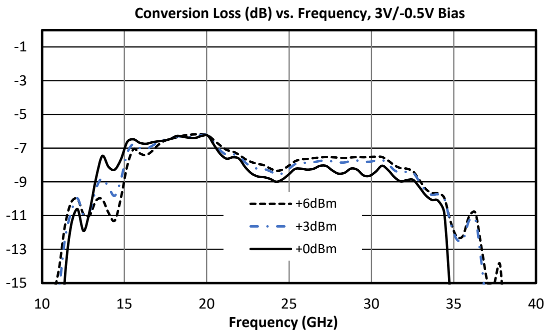
[14] Plots taken using EVAL-AMM-7199SM as LO driver for connectorized MM1-1140H module in configuration A with a 91MHz IF. Power specified is input power to EVAL-AMM-7199SM driver.

3.8 Typical Performance Plot of Marki MM1-1240S Using AMM-7199SM as LO Driver[15]







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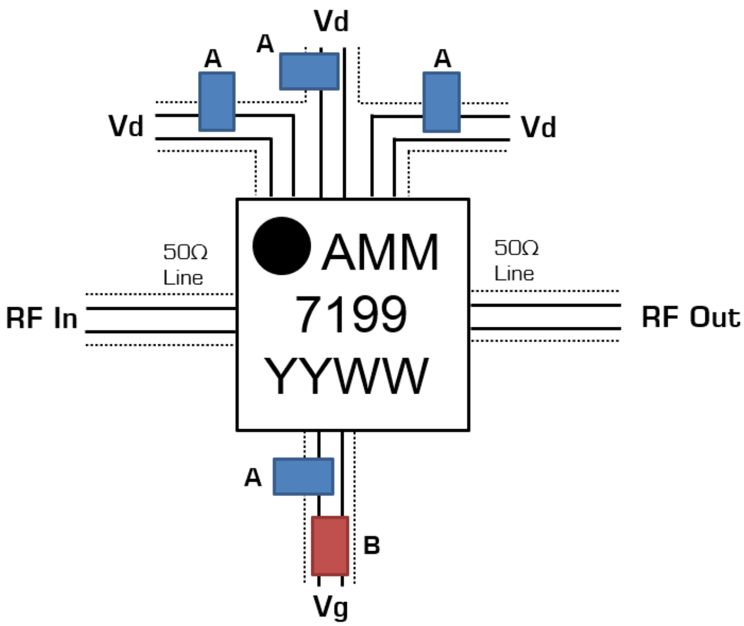
[15] Plots taken using EVAL-AMM-7199SM as LO driver for connectorized MM1-1240S module in configuration A with a 91MHz IF. Power specified is input power to EVAL-AMM-7199SM driver.

4. Application Information

4.1 Example Application Circuit

Below is the recommended application circuit for the AMM-7199SM. This is the configuration that is used to characterize this device. However, each PCB layout and environment are different which may require minor modifications of the biasing network. Please contact support@markimicrowave.com for more information.



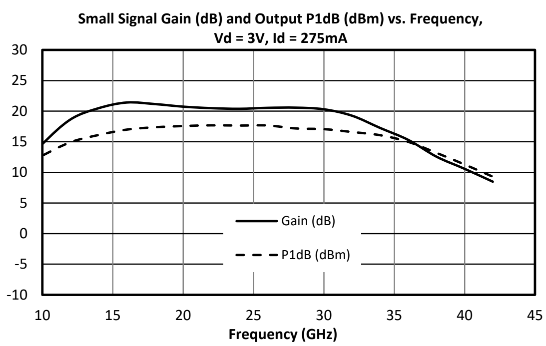
Designator	Description	Sample Part Number
A	0.1µF 16V 0402 Capacitor	AVX 0402YD104KAT2A
B	10Ω 0402 Resistor	TE CPF0402B10RE1

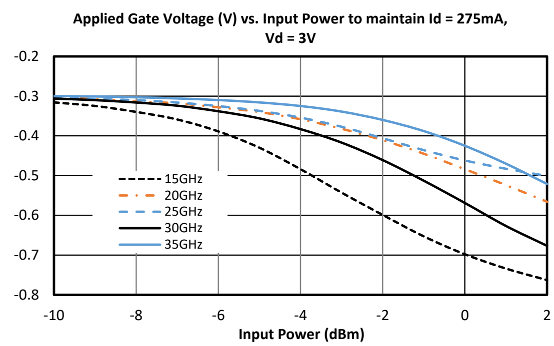
The three Vd lines are separated to minimize feedback between the transistor's stages. The passive devices should be 0402 or 0201 surface mount. Examples of suitable passive devices would be the AVX 0402YD104KAT2A capacitor and TE CPF0402B10RE1 resistor. In addition to the resistor and capacitor on the gate pin, the layout of the board should be designed to minimize stray coupling between the drain and gate biasing traces on the board. Additionally, the gate biasing pin AMM-7199SM can draw up to 0.5mA at certain combinations of frequency and input power.

4.2 Constant Current and Constant Voltage Operation

As with most amplifiers utilizing HEMT technology, the AMM-7199SM can be biased with a constant gate and drain voltage, or with a constant drain current by regulating the gate voltage. Using a constant gate and drain voltage for biasing reduces complexity, but has variable current consumption during operation. On the other hand, biasing the gate using a feedback network that samples the drain current minimizes unit-to-unit variation in gain and other parameters.

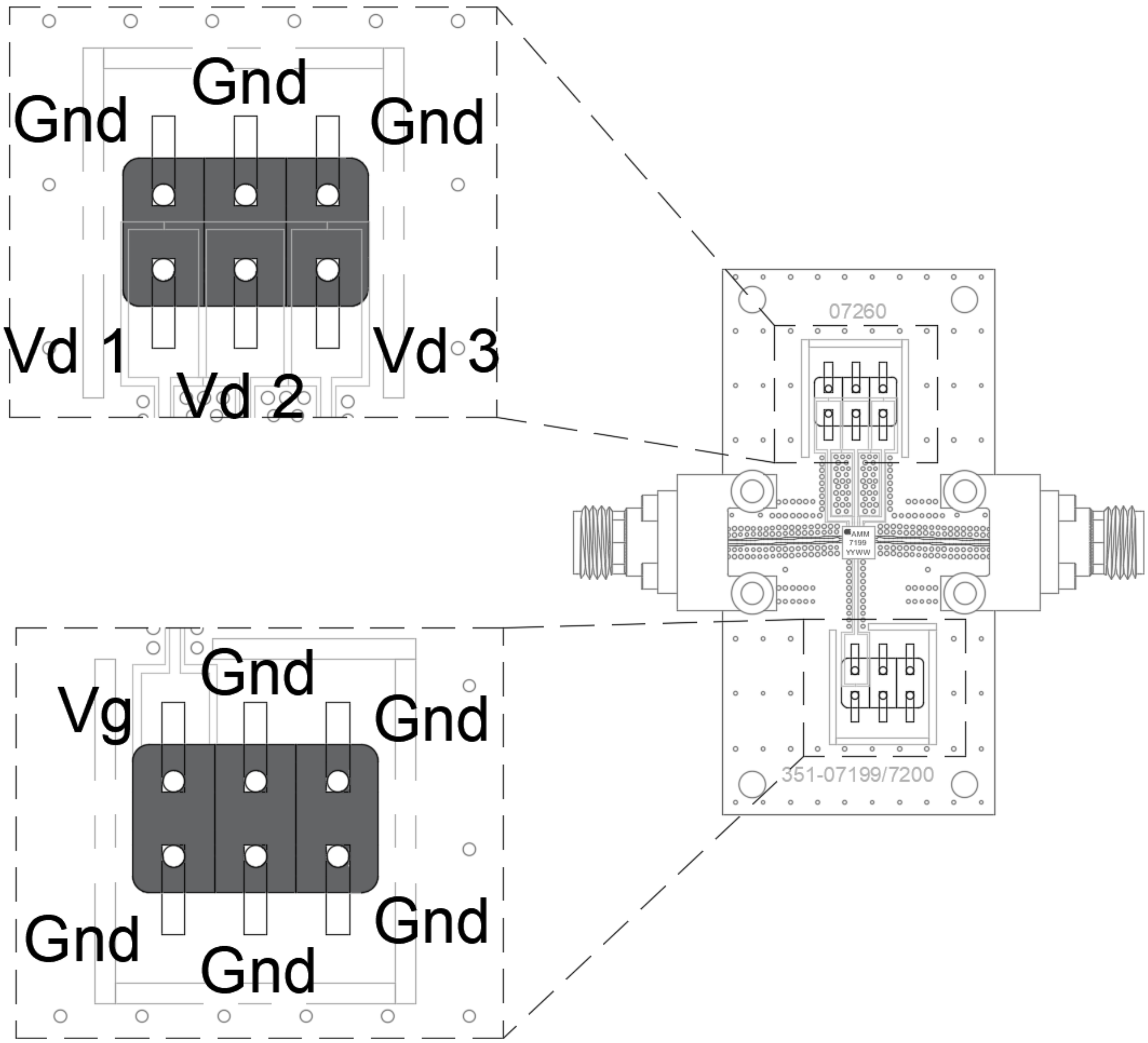
Under small signal excitation at a fixed temperature, these two approaches are equivalent. However, they will diverge in large signal conditions, where the drain current is affected by the frequency and power of the input signal. The output 1dB compression point versus frequency, and output power versus input power curves are shown under these conditions to give a sense for their behavior under these conditions. The gate voltage required to maintain constant current during these tests is also shown.





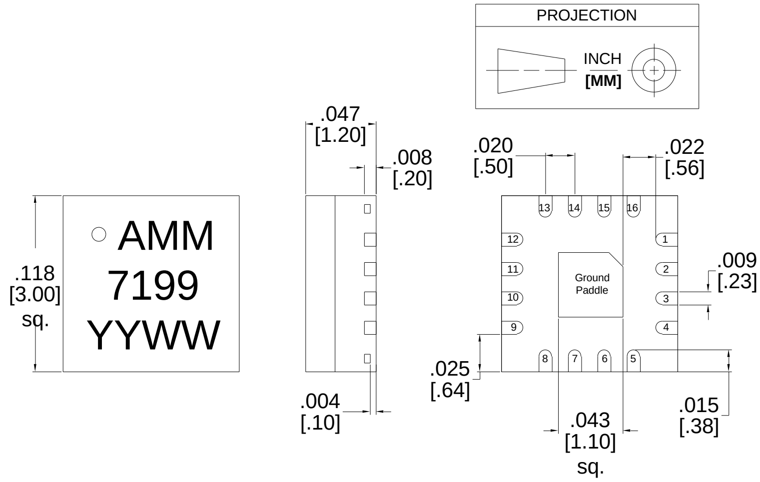
4.3 Header Pinouts

On the EVAL-AMM-7199SM, there are two headers for biasing the drains and gates of the transistors. The pinout of the headers is given with their location on the evaluation board below:



5. Mechanical Data

5.1 SMT Package Outline Drawing

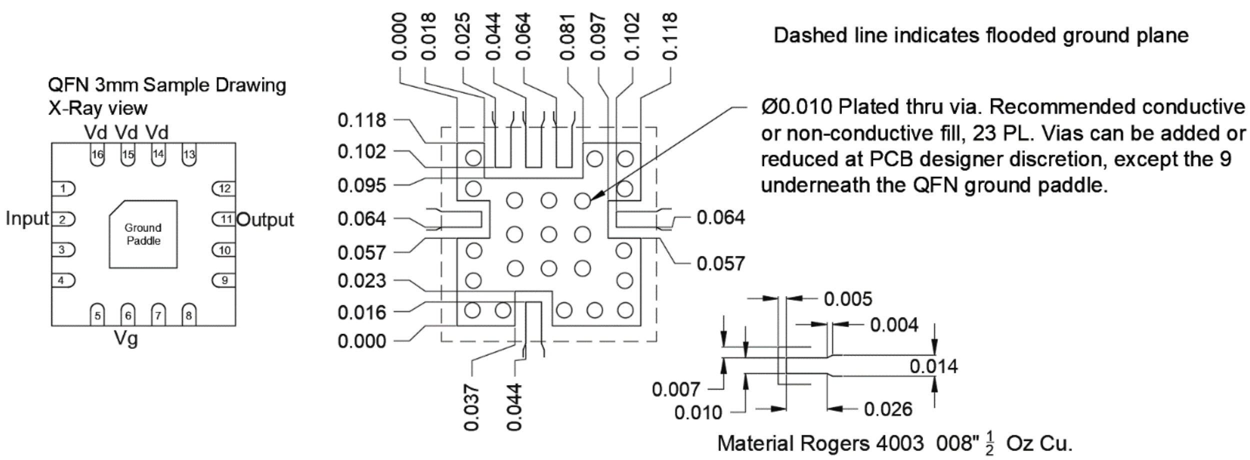


Pin #	Port
1	GND
2	RF In
3	GND
4	GND
5	N/C
6	Vg
7	N/C
8	N/C
9	GND
10	GND
11	RF Out
12	GND
13	N/C
14	Vd 3
15	Vd 2
16	Vd 1

Notes:

1) QFN material is plastic
2) I/O Leads and Die Paddle are 0.05 microns Au over 0.02 microns Pd over 0.5 microns Ni
3) All unconnected pins should be connected to PCB RF ground.

5.2 AMM-7199SM Recommended PCB Footprint



Landing pattern .dxf drawing: Landing Pattern AMM7199SM.dxf

5.3 EVAL Package Outline Drawing