LAUFTEK

LOW NOISE AMPLIFIER, 30K-40GHz

Model: LF-3040G-1215Q

PRODUCT OVERVIEW:

LF-3040G-1215Q is a wideband GaAs distributed low noise amplifier, which operates from 30K to 40GHz. The amplifier delivers 12 dB of gain with a corresponding noise figure of 7.0 dB and output 1dB compression point of 15 dBm at 40 GHz. The LF-3040G-1215Q is internally matched to 50 ohms which eliminates the need for RF port matching.

KEY FEATURES:

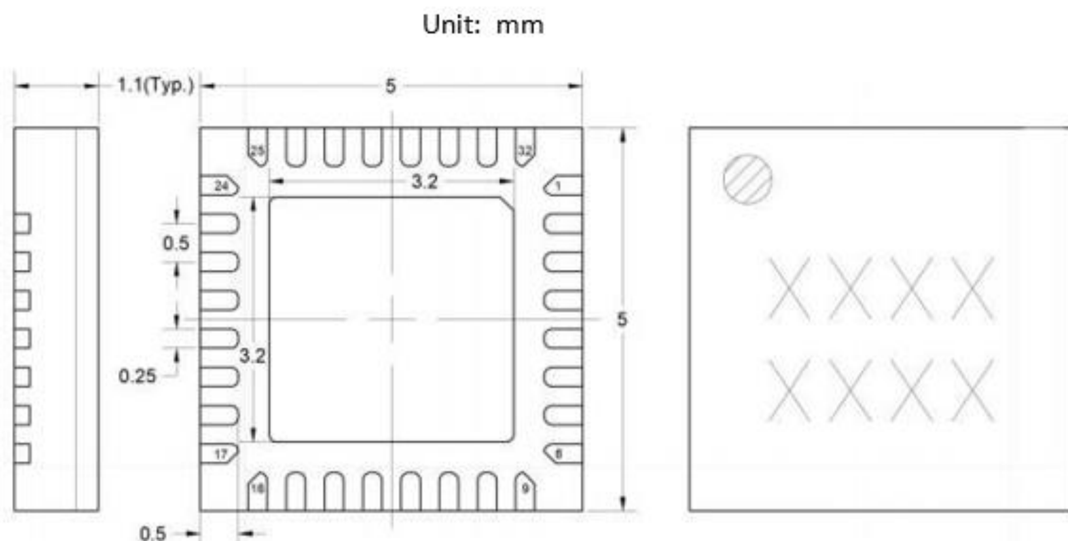
- Ultra Wide Band: 30K-40GHz
- Gain: 12dB Typ
- Output P1dB: 15dBm Typ
- Excellent return losses
- Compliant 5x5x1.1 mm QFN package

ELECTRICAL SPECIFICATIONS:

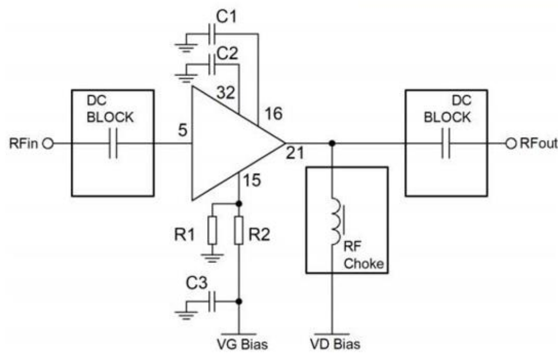
Parameter	Min	Typ	Max	Units
Frequency range	30KHz-40Ghz			
Gain		12		dB
Gain Flatness		±1.5	±2.5	dB
Output P1dB	10	15		dBm
Noise Figure		7		dB
Input VSWR		1.6	2.7	:1
Output VSWR		1.6	2.7	:1
DC Supply Current		120	150	mA

ABSOLUT MAXIMUM RATINGS:

Parameter	Valus
RF Input Power	17 dBm 30s CW
V_D	+8V
Channel temperature	150C
Operating Temperature	-55C ~ +85C
Non-operating Temperature	-55C ~ +150C

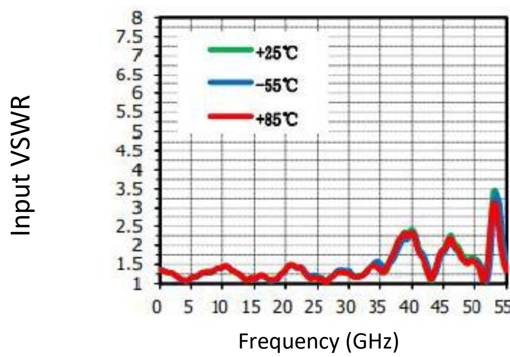


APPLICATION CIRCUIT DRAWING:

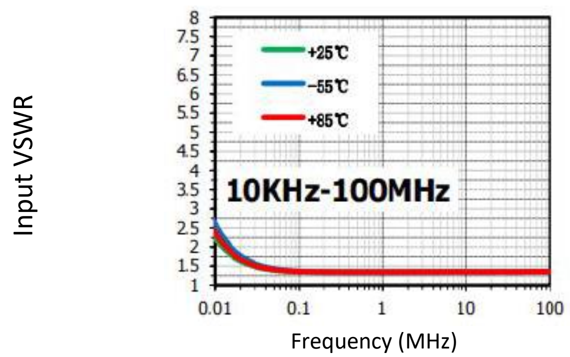


Test Curves: VD=+6V;IDQ=120mA

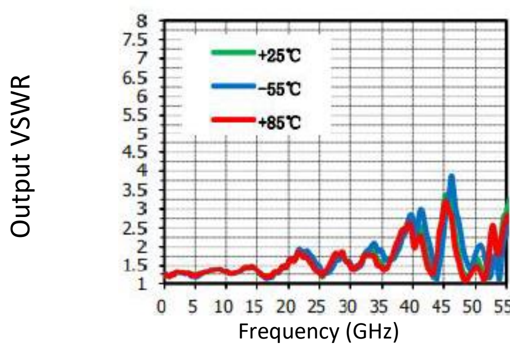
Input VSWR vs Temperature



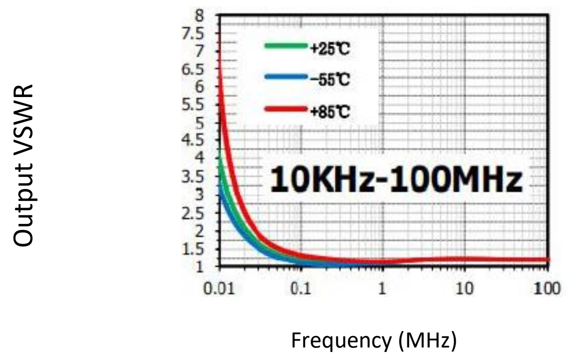
Input VSWR vs Temperature



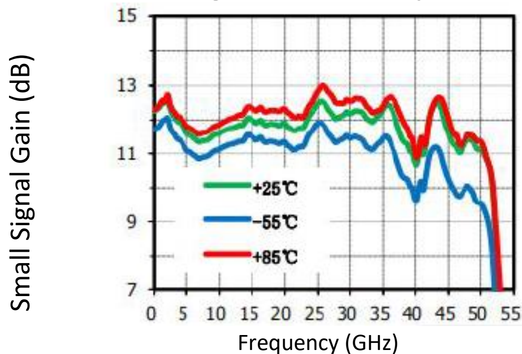
Output VSWR vs Temperature



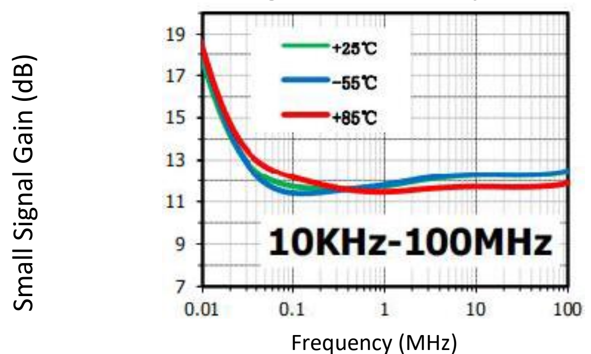
Output VSWR vs Temperature



Small Signal Gain vs Temperature



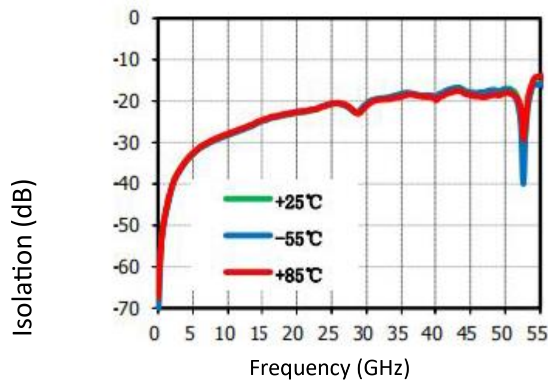
Small Signal Gain vs Temperature



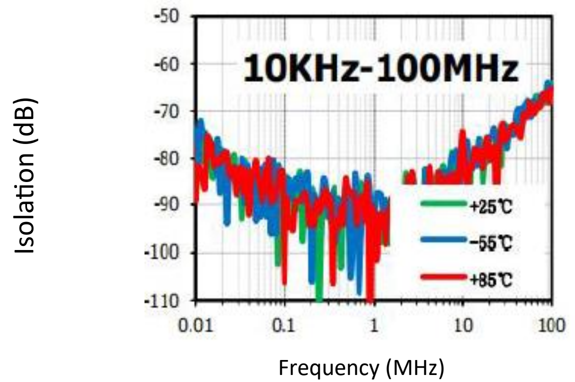
Note: Above data is for ref only, actual data may vary from unit to unit depending on operating environment and other factors like material lots etc.

Test Curves: VD=+6V;IDQ=120mA

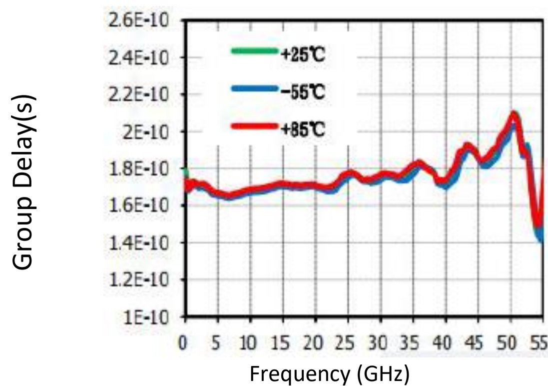
Isolation vs Temperature



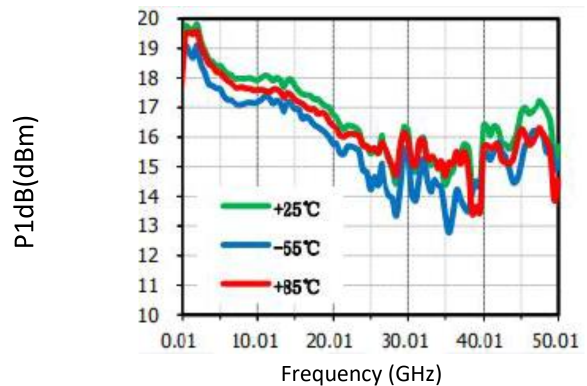
Isolation vs Temperature



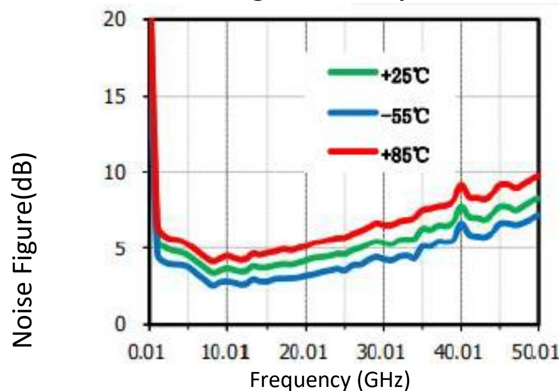
Groupe Delay vs Temperature



P1dB vs Temperature



Noise Figure vs Temperature



Note: Above data is for ref only, actual data may vary from unit to unit depending on operating environment and other factors like material lots etc.

ADDITIONAL INFORMATION:

1. Storage: The chip must be placed in a container with electrostatic protection function and stored in nitrogen environment.
2. Cleaning: The bare chip must be operated and used in a purified environment. It is forbidden to use liquid detergent to clean the chip.
3. Electrostatic protection: Please strictly comply with ESD protection requirements to avoid electrostatic damage.
4. Routine operation: Please use vacuum chuck or precision pointed tweezers to take the chip. Avoid touching the chip surface with tools or fingers during operation.
5. Power on sequence: when power on, apply gate voltage first and then Drain voltage; When the energizing, remove the Drain voltage first and then the gate voltage.

6. Mounting operation: The chip can be installed by AuSn solder eutectic sintering or conductive adhesive bonding process. The installation surface must be clean and flat, and the gap between the chip and the input / output RF connecting line substrate shall be as small as possible.
7. Sintering process: 80 / 20 AuSn shall be used for sintering. The sintering temperature shall not exceed 300C, the sintering time shall be as short as possible, not more that 20 seconds, and the friction time shall not exceed 3 seconds.
8. Bonding process: The dispensing amount of conductive adhesive shall be minimized during bonding, and the curing conditions shall refer to the data provided by the conductive adhesive manufacturer.
9. Bonding operation: Unless otherwise specified, two bonding wires (diameter 25 um gold wire) are used for Rf input and output, and the bonding wire shall be as short as possible. The thermal ultrasonic bonding temperature is 150C and the ultrasonic energy is as small as possible. The pressure of spherical bonding cleaver is 40~50gf and the pressure of wedge bonding cleaver is 18 ~ 22gf.
10. If you have any questions, please contact the supplier.