

21-26.5GHz Integrated Down converter

GaAs Monolithic Microwave IC

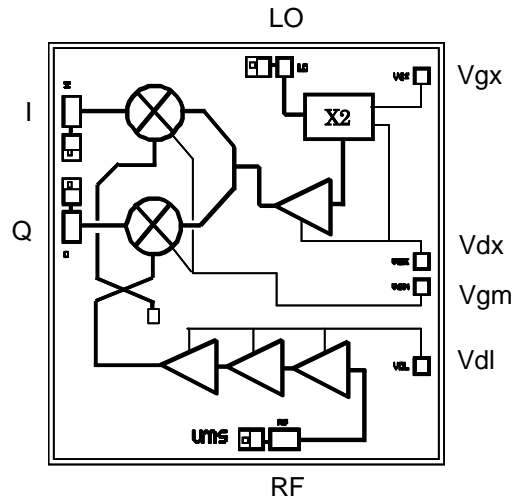
Description

The CHR3693-99F is a multifunction chip, which integrates a balanced cold FET mixer, a time two multiplier, and a RF self biased LNA.

It is designed for a wide range of applications, typically commercial communication systems.

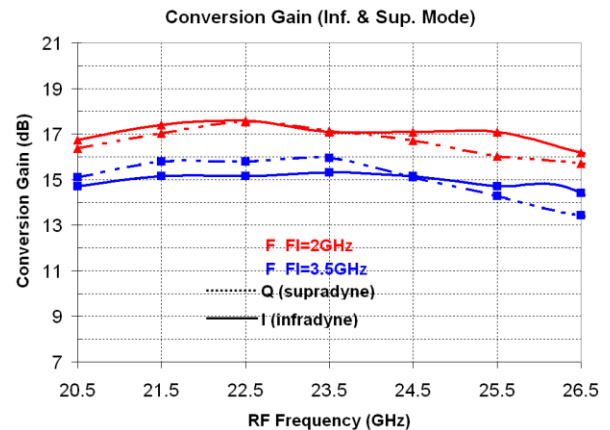
The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.



Main Features

- Broadband performance 21-26.5GHz
- 18dB gain
- -7dBm input IP3
- 18dBc image rejection
- DC bias: Vd=4.0Volt@Id=160mA
- Chip size: 2,45 x 2,45 x 0,1mm



Main Electrical Characteristics

Tamb.= +25°C, Vdx=Vdl = +4.0V, Vgx=-0.9V, Vgm=-0.7V

Symbol	Parameter	Min	Typ	Max	Unit
F_RF	RF frequency range	21		26.5	GHz
F_LO	LO frequency range	9		14	GHz
F_IF	IF frequency range	DC		3.5	GHz
Gc	Conversion gain	11	15		dB

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

Electrical Characteristics

Tamb.= +25°C, Vdx=Vdl = +4.0V, Vgx=-0.9V, Vgm=-0.7V

Symbol	Parameter	Min	Typ	Max	Unit
F_RF	RF frequency range	21		26.5	GHz
F_LO	LO frequency range	9		14	GHz
F_IF	IF frequency range	DC		3.5	GHz
Gc	Conversion gain	11	15	19	dB
NF	Noise Figure for IF>0.1GHz		3.2	3.7	dB
P_LO	LO Input power		2	5	dBm
Img Sup	Image Suppression ⁽²⁾	15	18		dBc
IIP3	Input IP3		-7		dBm
LO_RL	LO return loss		-9.5	-7	dB
RF_RL	RF return loss (21 to 24GHz)		-9.5	-7	dB
	RF return loss (24 to 26.5GHz)		-8	-6	dB
Id	Bias current ⁽¹⁾ (Idl + Idx)	120	160	200	mA

⁽¹⁾ Typically, Idl= 90mA, Idx=70mA

⁽²⁾ With external I/Q 90° hybrid coupler

These values are representative of on-wafer measurements that are made without bonding wires at the RF ports. A bonding wire of typically 0.1 to 0.15nH will improve the matching at the accesses.

Absolute Maximum Ratings ⁽¹⁾

Tamb.= +25°C

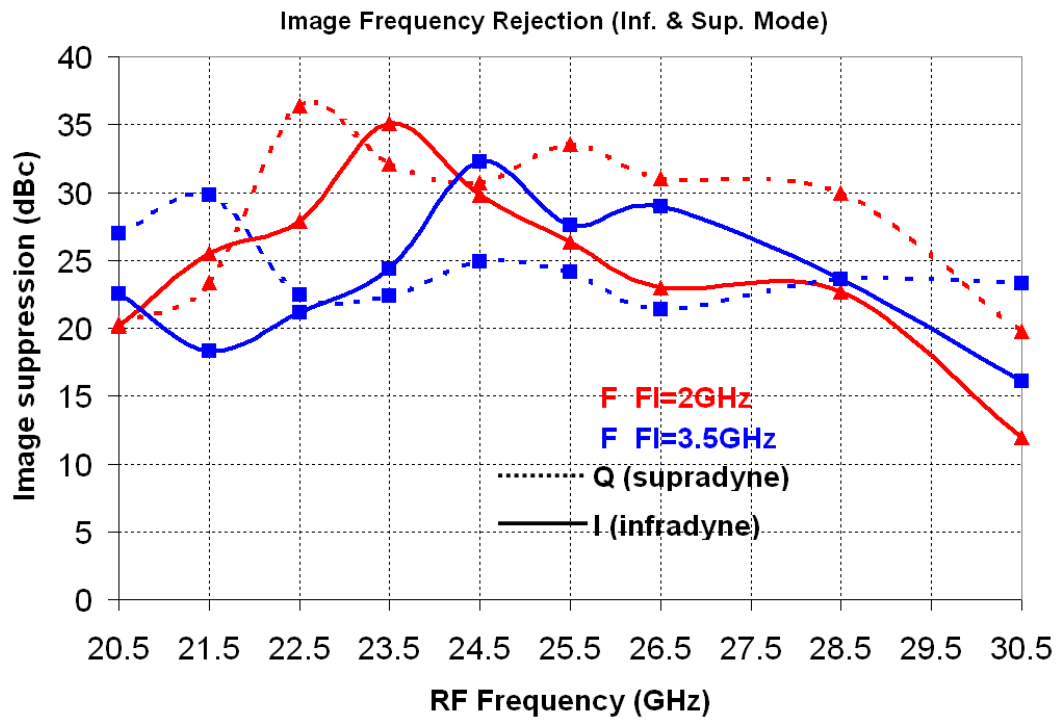
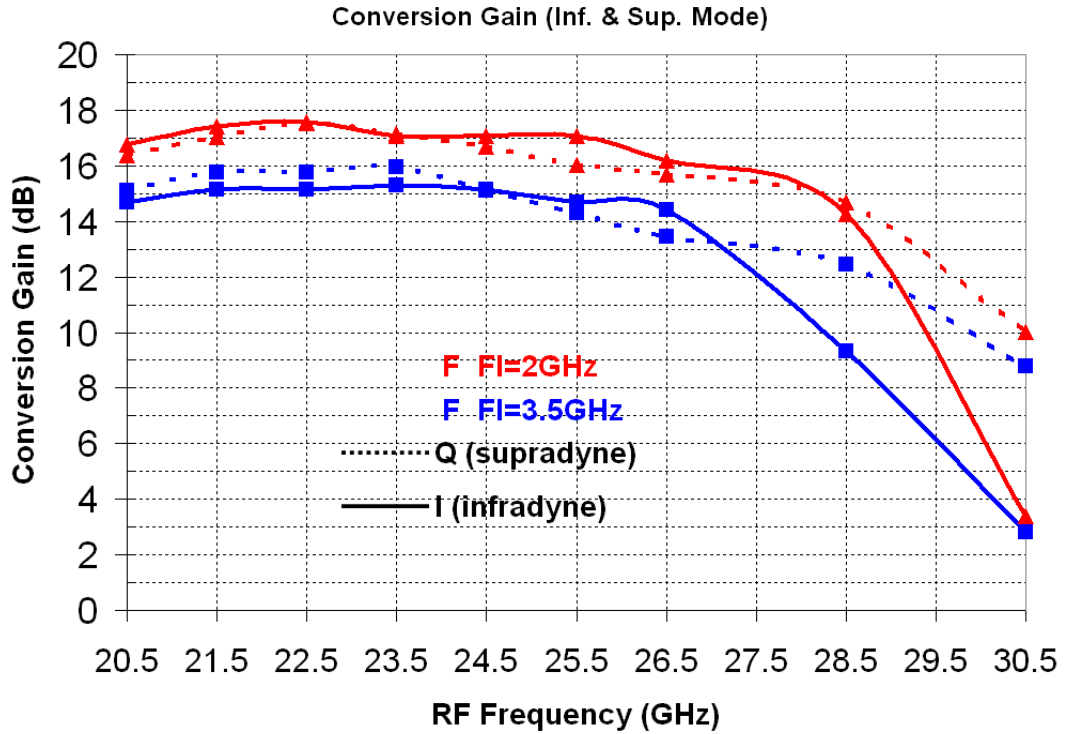
Symbol	Parameter	Values	Unit
Vd	Maximum drain bias voltage	4.5	V
Id	Maximum drain bias current	230	mA
Vg	Gate bias voltage	-2.0 to +0.4	V
P_RF	Maximum RF input power ⁽²⁾	10	dBm
P_LO	Maximum LO input power ⁽²⁾	10	dBm
Tch	Maximum channel temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

⁽¹⁾ Operation of this device above any one of these parameters may cause permanent damage.

⁽²⁾ Duration < 1s.

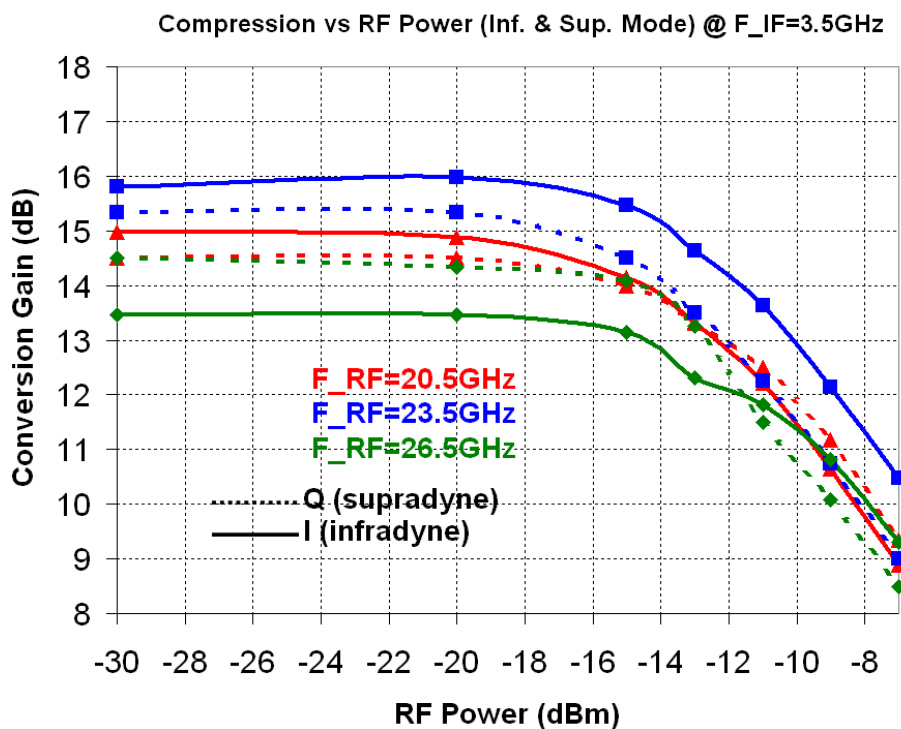
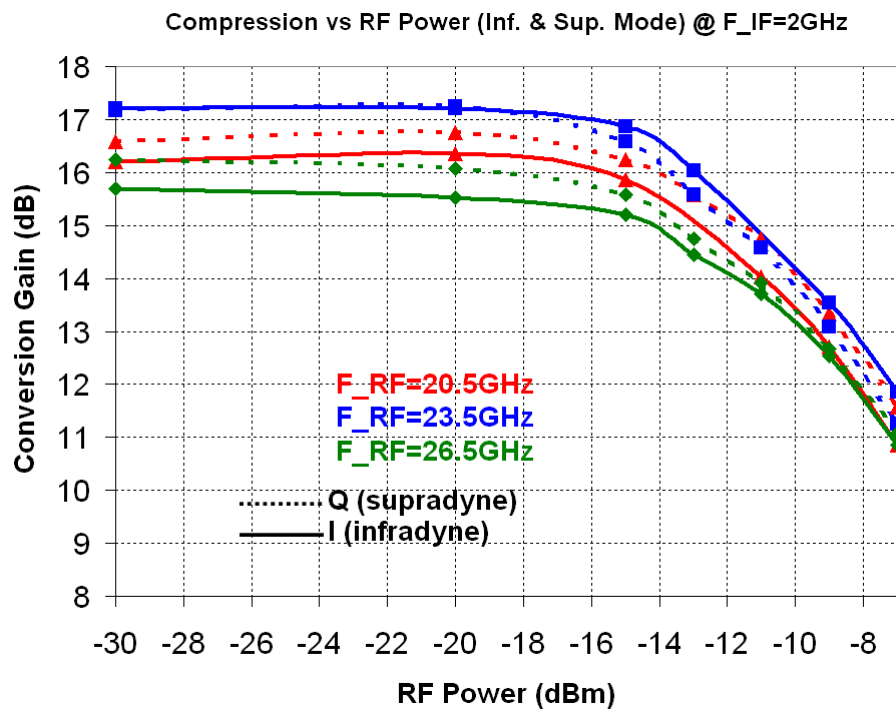
Typical on wafer Measurements

Tamb=25°C, Vdx=Vdl=4V, Typical Vgx=-0.9V & Vgm=-0.7V



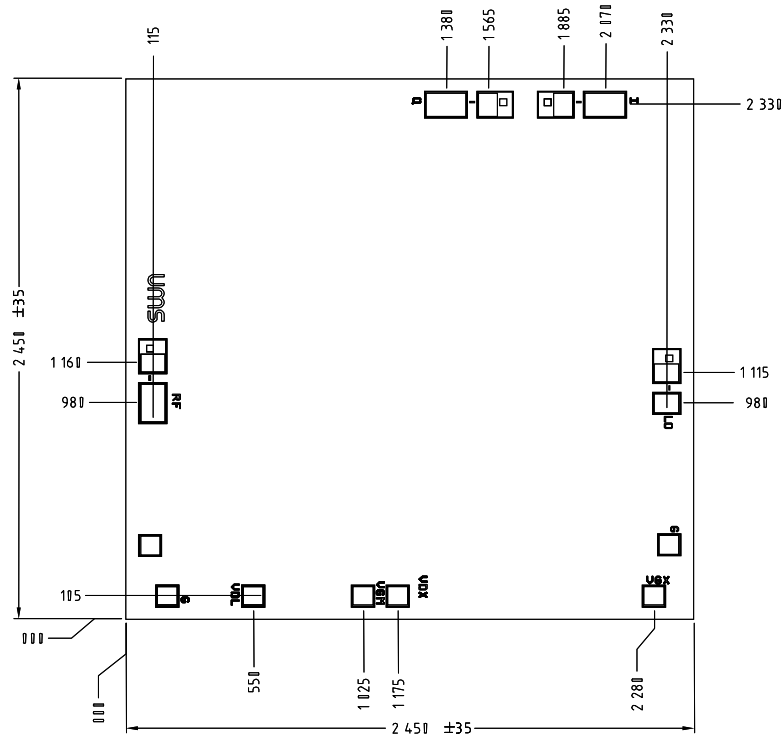
Typical on wafer Measurements

Tamb=25°C, Vdx=Vdl=4V, Typical Vgx=-0.9V & Vgm=-0.7V



Mechanical data

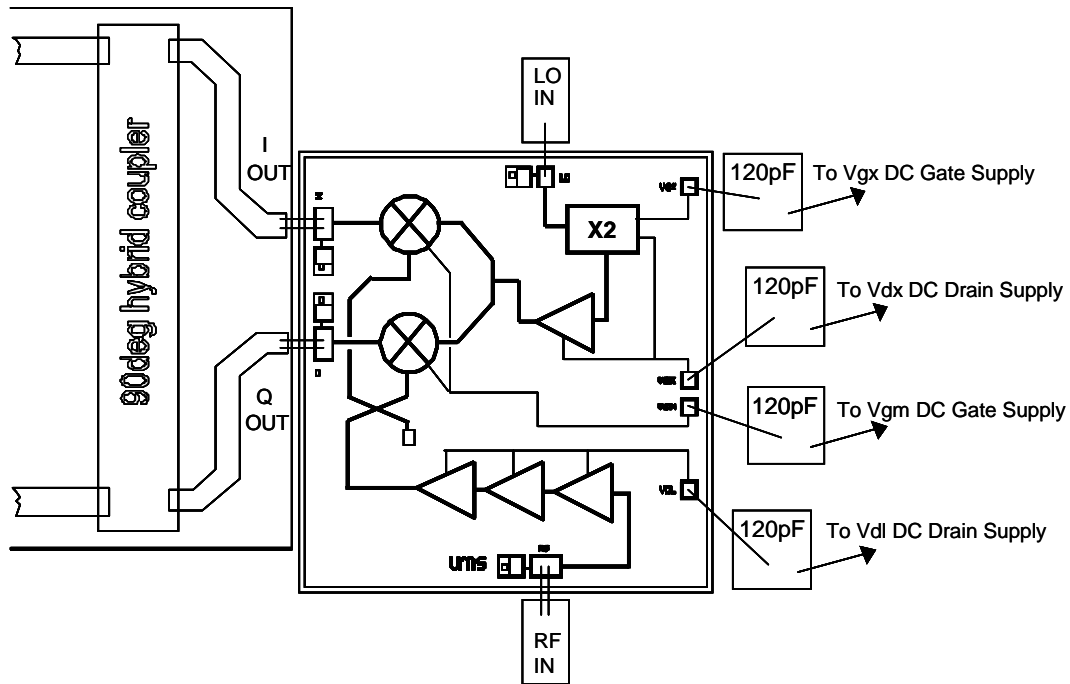
Bonding pad positions



Chip thickness: 100µm.
Chip size: 2450x2450 ±35µm
All dimensions are in micrometers

Supply feed should be capacitively bypassed.
25µm diameter gold wire is recommended.

Recommended assembly plan



25µm wedge bonding is preferred

Recommended circuit bonding table

Label	Type	Decoupling	Comment
Vgx	Vg	120pF	Multiplier gate control
Vdx	Vd	120pF	Multiplier chain Drain Supply
Vgm	Vg	120pF	Mixer gate control
Vdl	Vd	120pF	LNA Drain Supply

Notes

Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS products.

Ordering Information

Chip form:

CHR3693-99F/00

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