

(SP2T) SWITCH, 0.1 GHz to 44 GHz

Model: LF-SP2T-44-LGA

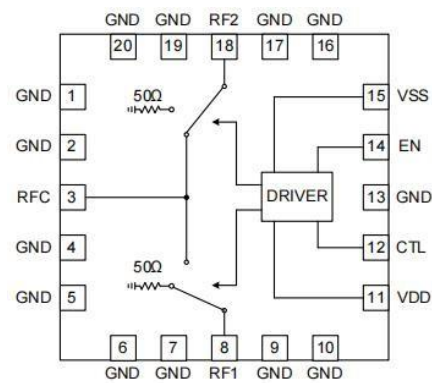
PRODUCT OVERVIEW:

The **LF-SP2T-44-LGA** is a wideband, high isolation, low insertion loss, absorptive, double-throw (SP2T) switch. It operates from 0.1 GHz to 44 GHz (10kHz is available) with an insertion loss of lower than 1.8 dB and isolation of around 50 dB. The **LF-SP2T-44-LGA** comes in a 20-terminal, 3 mm x 3 mm, RoHS-compliant, land grid array (LGA) package.

KEY FEATURES:

- Ultrawide Band: 0.1-44GHz (10kHz is available)
- Insertion Loss:
 - 1.2dB@100MHz-18GHz
 - 1.4dB@18GHz-26GHz
 - 1.8dB@26GHz-44GHz
- Isolation:
 - 60dB@100MHz-18GHz
 - 55dB@18GHz-26GHz
 - 50dB@26GHz-44GHz
- Compliant 20-terminal, 3x3 mm LGA package

FUNCTIONAL BLOCK DIAGRAM:



ELECTRICAL SPECIFICATIONS: (TA=+25°C, Vdd=3.3V, Vss=-3.3V, v1=v2=0/3.3v):

Parameter		Min	Typ	Max	Units
Frequency range		0.1-44			GHz
Insertion Loss	100MHz-18GHz		1.2		dB
	18GHz-26GHz		1.4		
	26GHz-44GHz		1.8		
Isolation	100MHz-18GHz		60		dBm
	18GHz-26GHz		55		
	26GHz-44GHz		50		
Input Return Loss			-18		dB
Output Return Loss	Isolation state		-17		dB
	Insertion loss state		-16		
Input P1dB@9KHz-22GHz			27		dBm
Input IP3@1-40GHz			41		dBm
VDD		3		5	V
IDD			0.4		mA
VSS		-3.6		-3	V

ELECTRICAL SPECIFICATIONS: (TA=+25°C, Vdd=3.3V, Vss=-3.3V, v1=v2=0/3.3v):

Parameter		Min	Typ	Max	Units
V1、 V2	Low	0		0.3	V
	High	3		3.6	
	Lin		15		μA
Rise/Fall Time	10% to 90% RF output		17		ns
Switch Time	50% VCTRL to 10%/90% RF output		3		ns
Input Power	Insertion loss state			24	dBm
	Isolation state			24	
Phase Consistency			2		°
Amplitude Consistency			0.1		dB

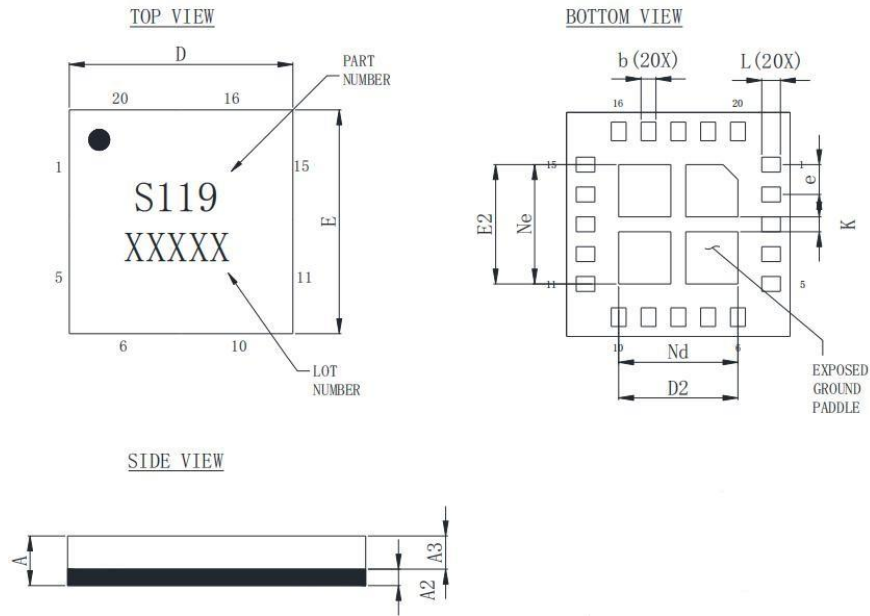
Note:

1. The minimum frequency of the test instrument is 10KHz, so only the test data above 10KHz is displayed.
2. There is no integrated DC/DC conversion module inside the chip, so the positive/negative power supply (VDD/VSS) of the chip must be turned on, and the range of VSS is -3.6~-3.0 (V).

ABSOLUTE MAXIMUM RATINGS:

Parameter	Value
Input Power (Insertion loss state)	28 dBm
Input Power (Isolation state)	26 dBm
VDD	-0.3-5.6V
V1、 V2	-0.5-3.6V
T jmax	135°C
R jc	110°C/W
Operating Temperature	-40°C~+85°C
Non-operating Temperature	-65°C~+150°C
ESD(HBM)	Class 1C V
ESD(CDM)	Class C3 V

OUTLINE AND PORT SIZE: Unit mm

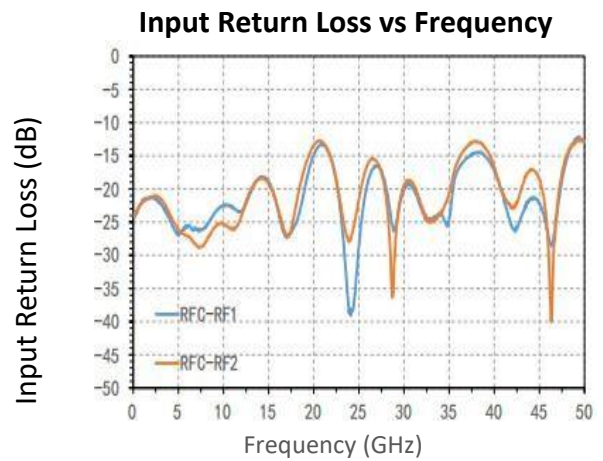
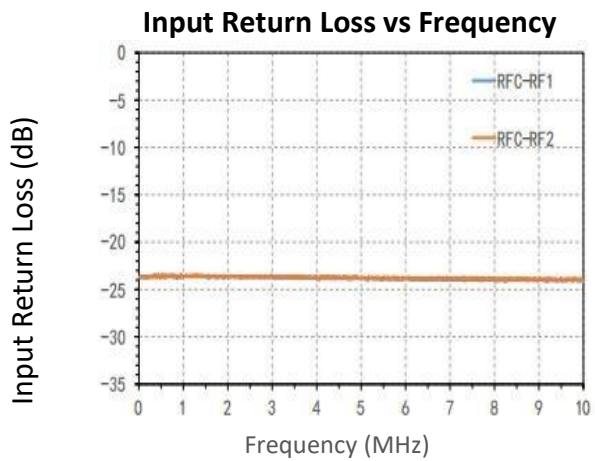
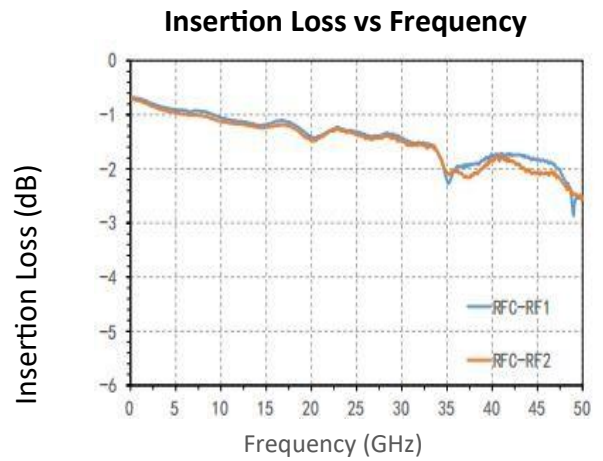
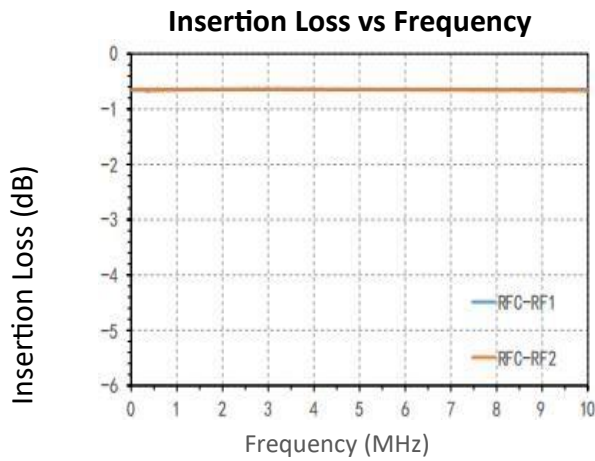


Symbol	Min	Nom	Max
A	0.565	0.665	0.765
A2	0.19	0.22	0.25
A3	0.445		
b	0.15	0.2	0.25
D	2.9	3	3.1
D2	1.5	1.6	1.7
e	0.40BSC		
Ne	1.60BSC		
Nd	1.60BSC		
E	2.9	3	3.1
E2	1.5	1.6	1.7
K	0.5	0.6	0.7
L	0.2	0.25	0.3

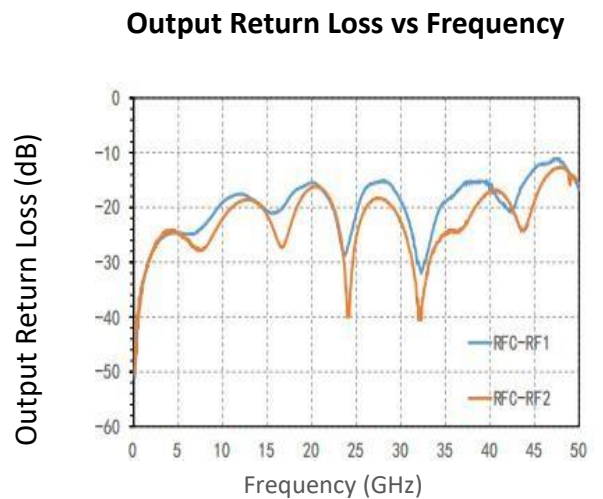
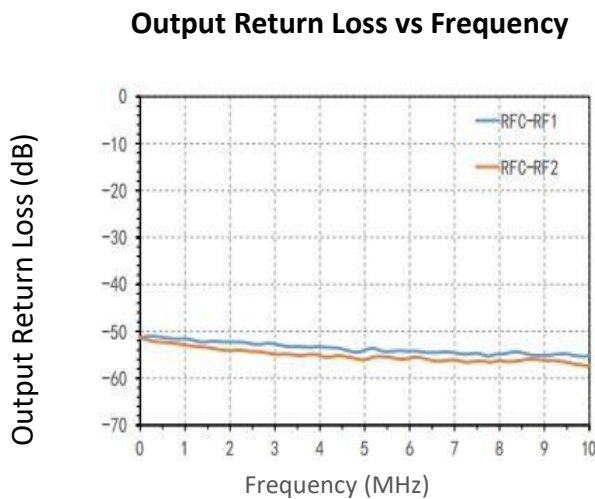
EN	CTL	Signal Path State	
		RFC-RF1	RFC-RF2
Low	Low	OFF	ON
Low	High	ON	OFF
High	Low	OFF	OFF
High	High	OFF	OFF

TYPICAL PERFORMANCE DATA:

Test Curves: (TA=+25°C, Vdd=+3.3V, Vgg=-3.3V, v1=v2=0/3.3v)



Isolation state



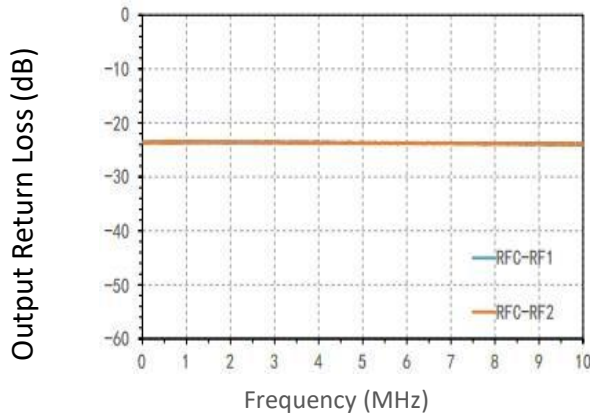
Note: Above data is for ref only, actual data may vary from unit to unit depending on operating environment and other factors like material lots etc.

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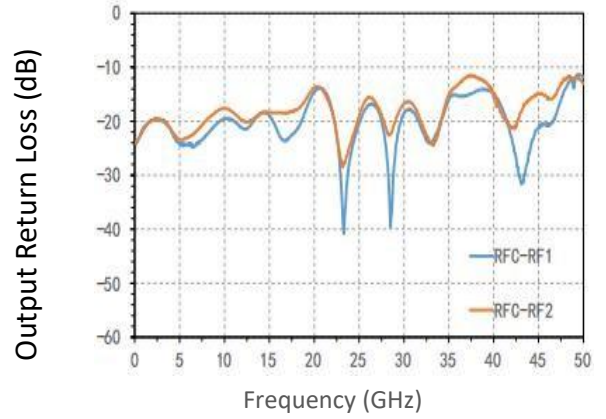
Test Curves: (TA=+25°C, Vdd=3.3V, Vgg=-3.3V, v1=v2=0/3.3v)

Insertion loss state

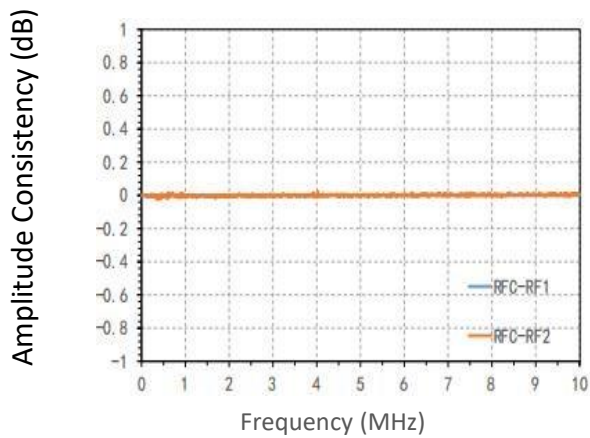
Output Return Loss vs Frequency



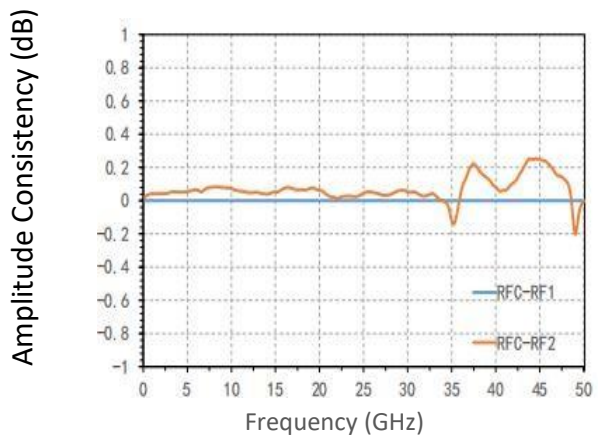
Output Return Loss vs Frequency



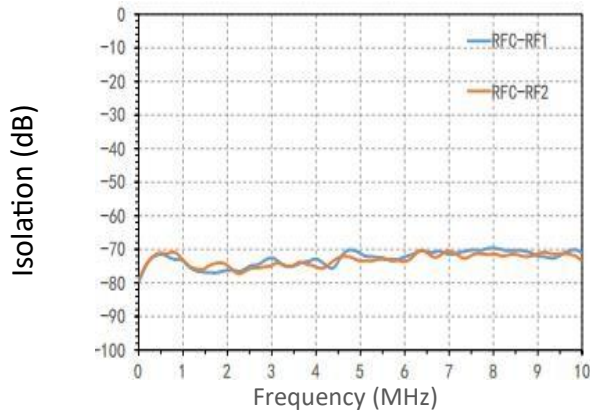
Amplitude Consistency vs Frequency



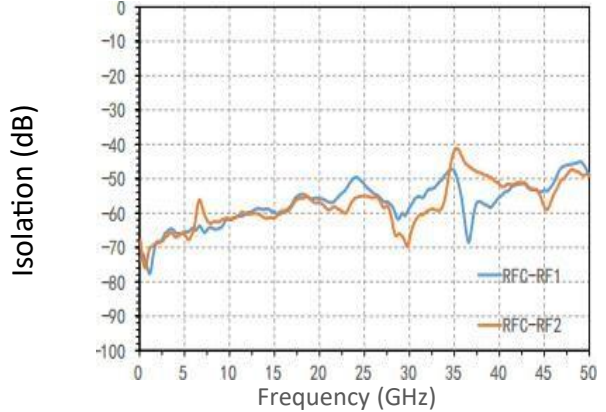
Amplitude Consistency vs Frequency



Isolation vs Frequency



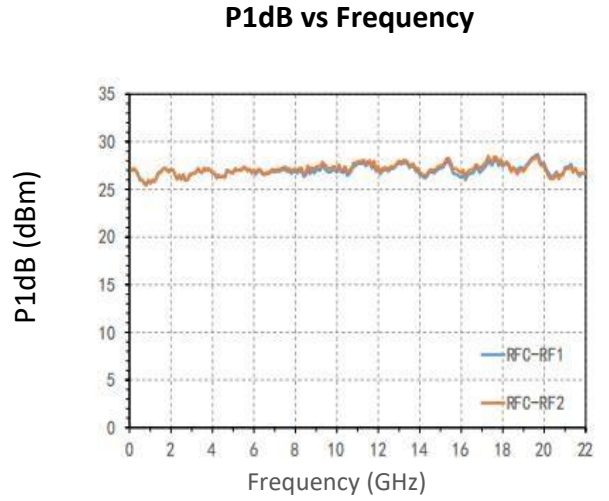
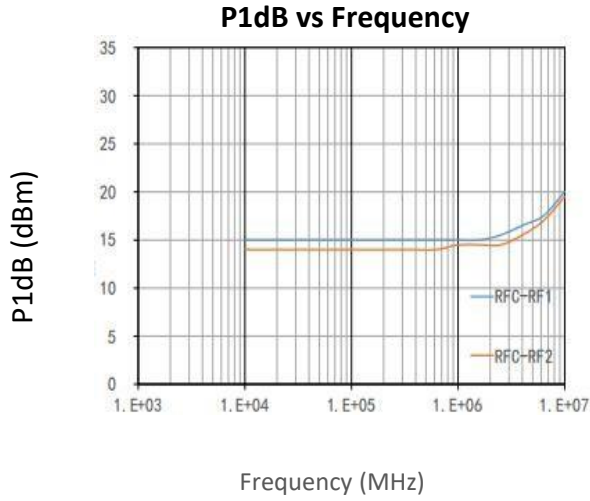
Isolation vs Frequency



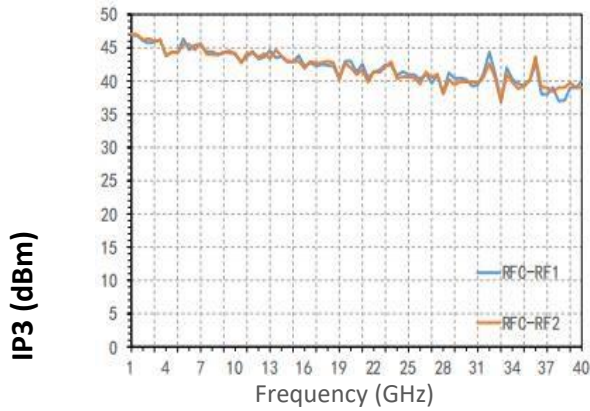
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TYPICAL PERFORMANCE DATA:

Test Curves: (TA=+25°C, Vdd=3.3V, Vgg=-3.3V, v1=v2=0/3.3v)



IP3 vs Frequency



Note: Above data is for ref only, actual data may vary from unit to unit depending on operating environment and other factors like material lots etc.

APPLICATION INFORMATION:

1. Storage: The chip must be placed in a container with electrostatic protection function and stored in nitrogen environment.
2. Cleaning: The bare chip must be operated and used in a purified environment. It is forbidden to use liquid detergent to clean the chip.
3. Electrostatic protection: Please strictly comply with ESD protection requirements to avoid electrostatic damage.
4. Routine operation: Please use vacuum chuck or precision pointed tweezers to take the chip. Avoid touching the chip surface with tools or fingers during operation.
5. Power on sequence: when power on, apply gate voltage first and then Drain voltage; When de-energizing, remove the Drain voltage first and then the gate voltage.
6. Mounting operation: The chip can be installed by AuSn solder eutectic sintering or conductive adhesive bonding process. The installation surface must be clean and flat, and the gap between the chip and the input / output RF connecting line substrate shall be as small as possible.
7. Sintering process: 80 / 20 AuSn shall be used for sintering. The sintering temperature shall not exceed 300 °C, the sintering time shall be as short as possible, not more than 20 seconds, and the friction time shall not exceed 3 seconds.
8. Bonding process: The dispensing amount of conductive adhesive shall be minimized during bonding, and the curing conditions shall refer to the data provided by the conductive adhesive manufacturer.
9. Bonding operation: Unless otherwise specified, two bonding wires (diameter 25µm gold wire) are used for RF input and output, and the bonding wire shall be as short as possible. The thermal ultrasonic bonding temperature is 150 °C, and the ultrasonic energy is as small as possible. The pressure of spherical bonding cleaver is 40 ~ 50gf, and the pressure of wedge bonding cleaver is 18 ~ 22gf.
10. If you have any questions, please contact the supplier.