35-45GHz Self biased Single Side Band Mixer

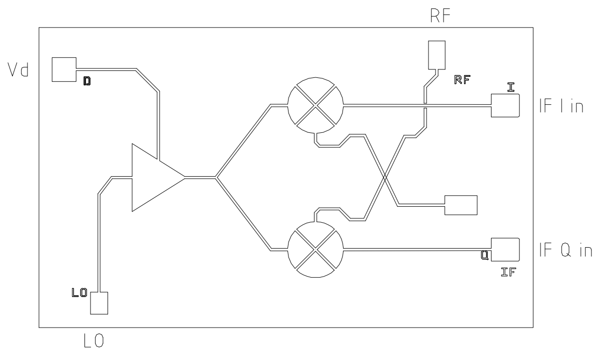
GaAs Monolithic Microwave IC

Description

The CHM1294 is a multifunction chip (MFC) which integrates a self biased LO buffer amplifier and a sub-harmonically balanced diode mixer for 2LO suppression and image rejection. It is usable both for up-conversion and down-conversion.

It is designed for a wide range of applications, typically commercial communication systems for broadband local access. The backside of the chip is both RF and DC grounded. This helps to simplify the assembly process.

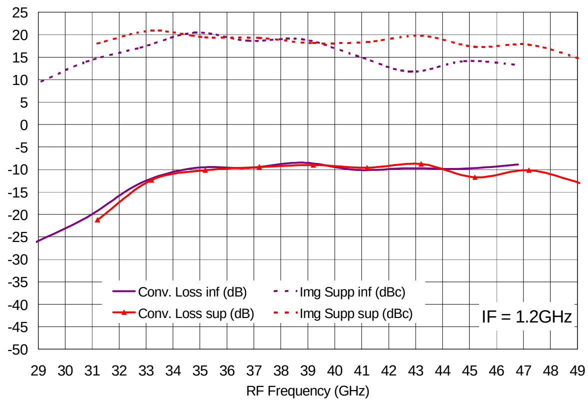
The circuit is manufactured with a pHEMT process, 0.25µm gate length.
It is available in chip form.



Main Features

- ■ Broadband performances: 35-45GHz
- ■ 11dB conversion Loss
- ■ 15dBc image rejection
- ■ +10dBm LO input power
- ■ +0dBm input power (1dB gain comp.)
- ■ Power consumption 60mA@4V
- ■ Chip size: 2.06x1.25x0.10mm

Up converter, Infradyne & supradyne



Main Characteristics

Tamb. = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	35		45	GHz
F_{LO}	LO frequency range	16		24	GHz
F_{IF}	IF frequency range	DC		3	GHz
L_c	Conversion Loss		11		dB

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

United Monolithic Semiconductors S.A.S.
Route Départementale 128 - B.P.46 - 91401 Orsay Cedex France
Tel. : +33 (0)1 69 33 03 08 - Fax : +33 (0)1 69 33 03 09

Electrical Characteristics for Broadband Operation

Tamb=+25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_{LO}	LO frequency range	16		24	GHz
F_{IF}	IF frequency range	DC		3	GHz
L_c	Conversion Loss		11		dB
P_{LO}	LO Input power		+10		dBm
2xLO Leak	2xLO Leakage (for P_{LO} = +10dBm)		-35		dBm
Img Rej	Image Rejection (1)		15		dBc
P1dB	Input power at 1dB compression		+0		dBm
LO Match	LO VSWR*		2.0:1		
RF Match	RF VSWR*		2.0:1		
IF Match	IF VSWR*		2.0:1		
Vd	Drain bias supply		4		V
Id	Bias current		60		mA

(1) With external quadrature hybrid coupler (reference on request). The minimal value depends on the quality of the external quadrature combiner.
* A bonding wire of typically 0.1 to 0.15nH will improve the accesses matching.

Absolute Maximum Ratings

Tamb.=+25°C (1)

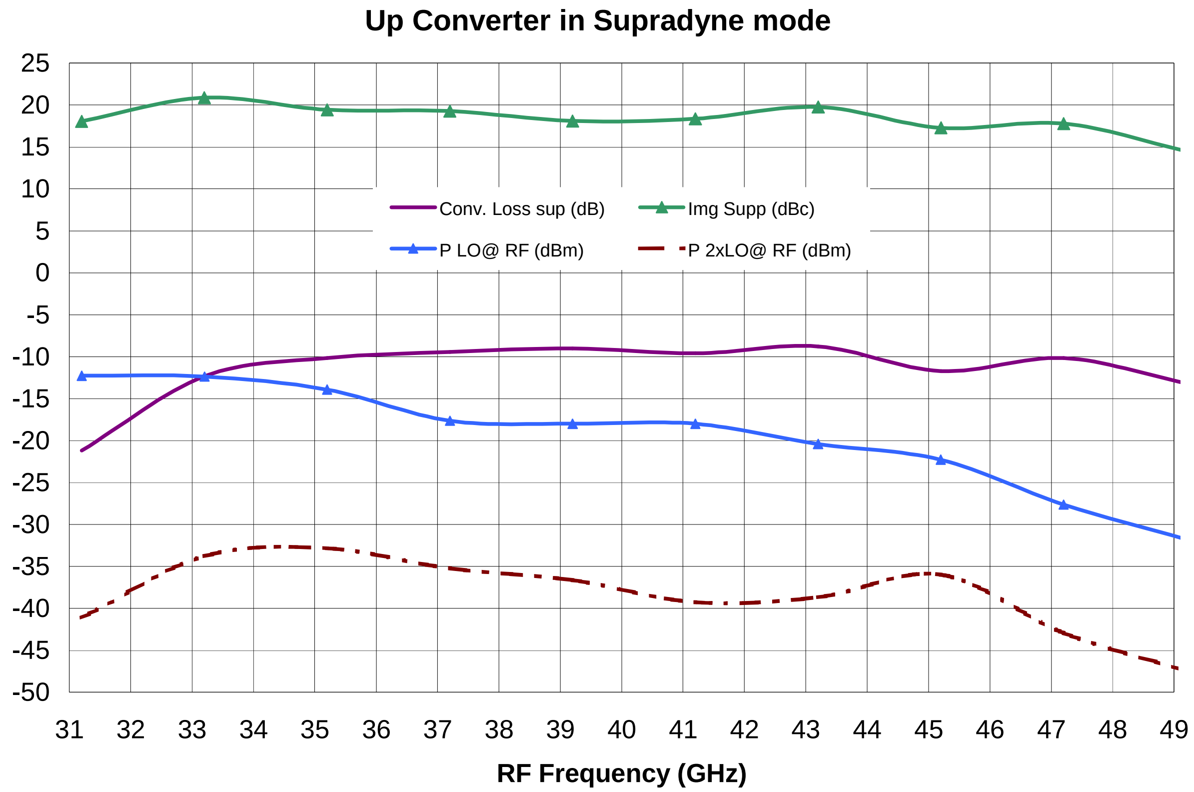
Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.5	V
Id	Drain bias current	90	mA
P_{LO}	Maximum LO input power	15	dBm
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +125	°C

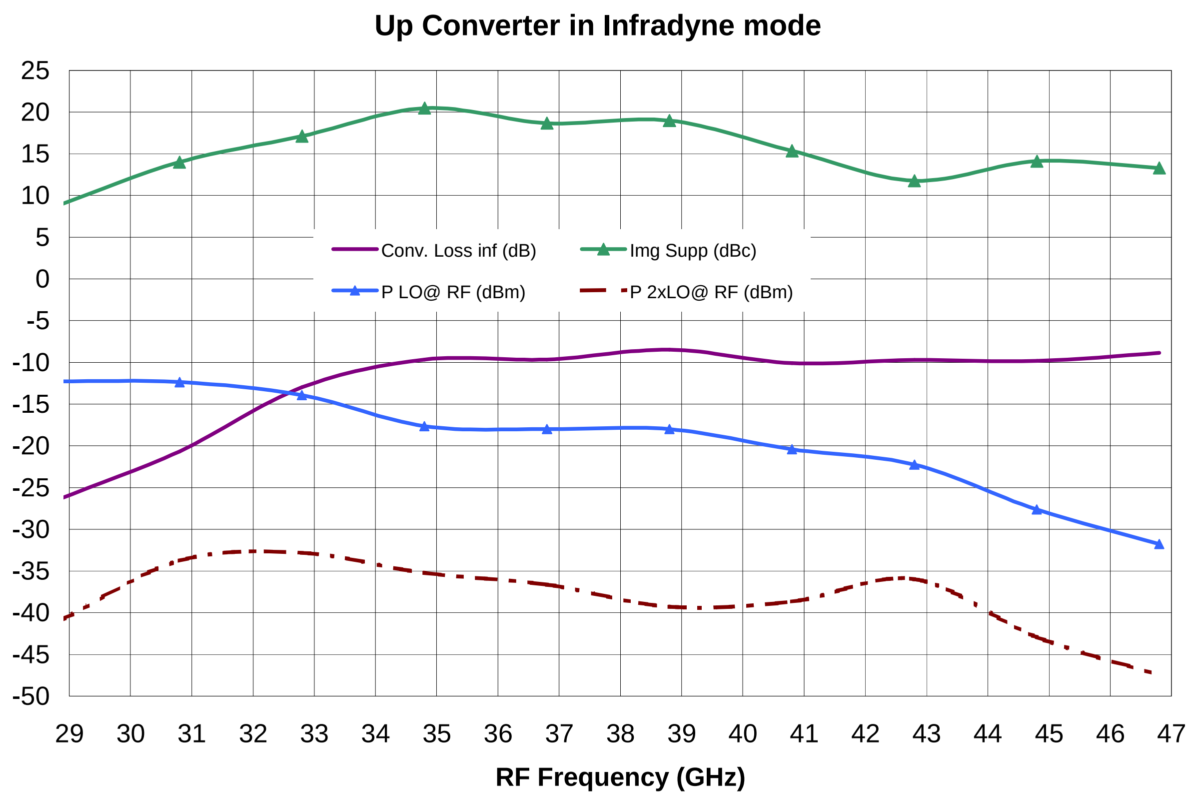
(1) Operation of this device above anyone of these parameters may cause permanent damage.

Route Départementale 128, B.P.46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0)1 69 33 03 08 - Fax : +33 (0)1 69 33 03 09
united monolithic semiconductors

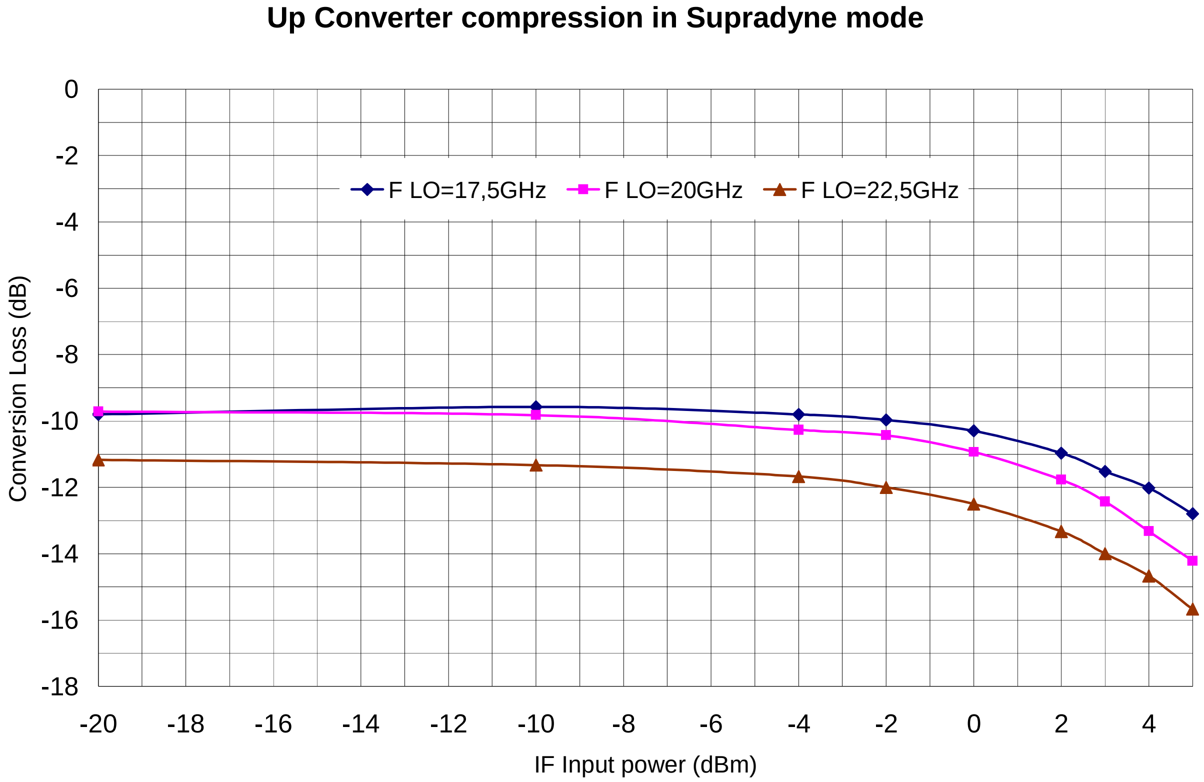
Typical on wafer measurement

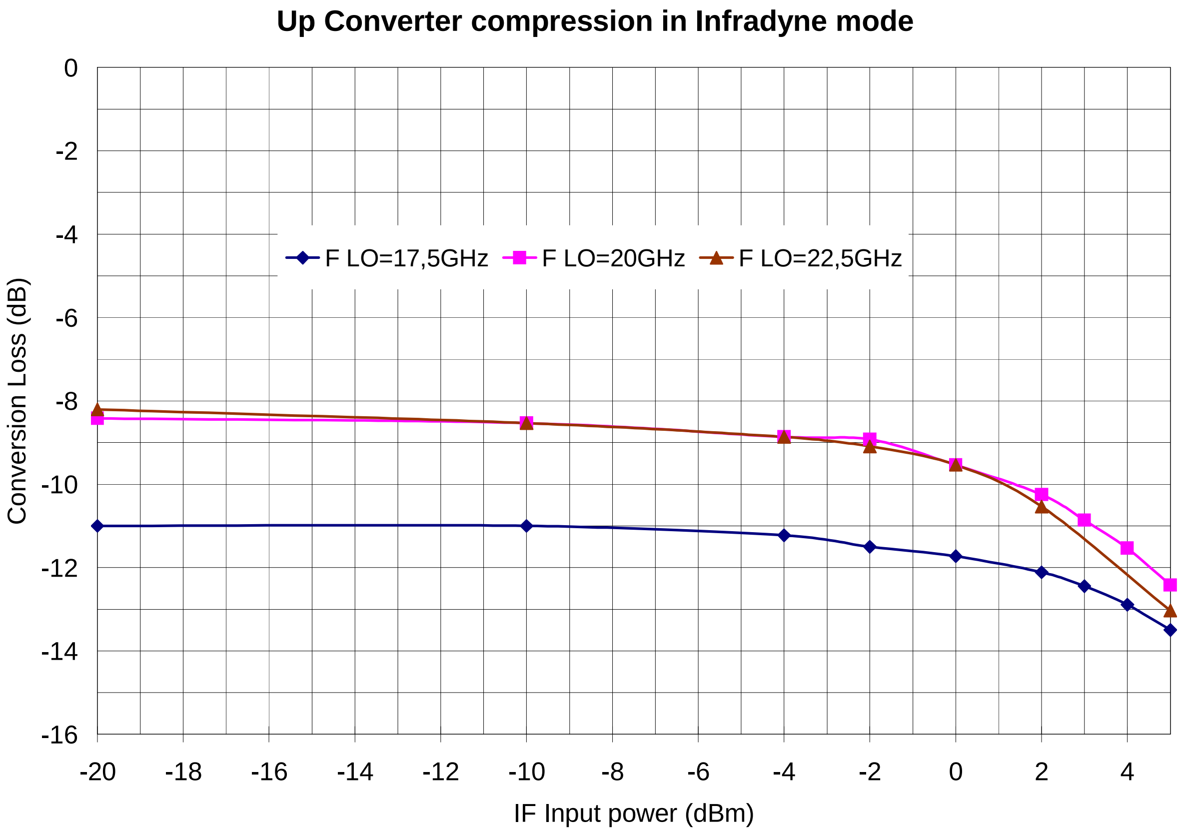
Tamb=+25℃, Vd=4V, Id=60mA, Freq IF=1.2GHz, P_LO=10 dBm





Route Départementale 128, B.P.46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0)1 69 33 03 08 - Fax : +33 (0)1 69 33 03 09

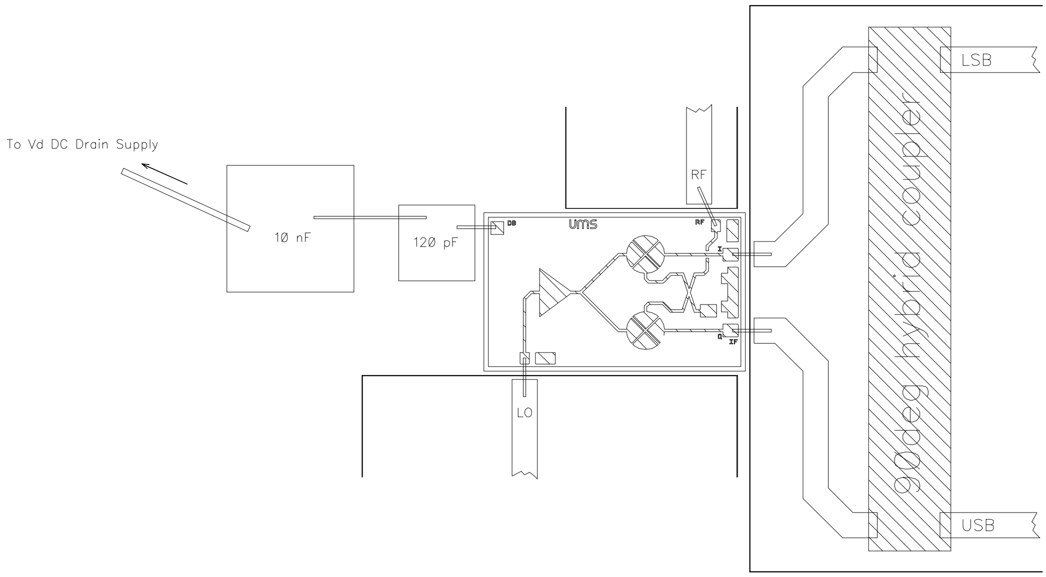




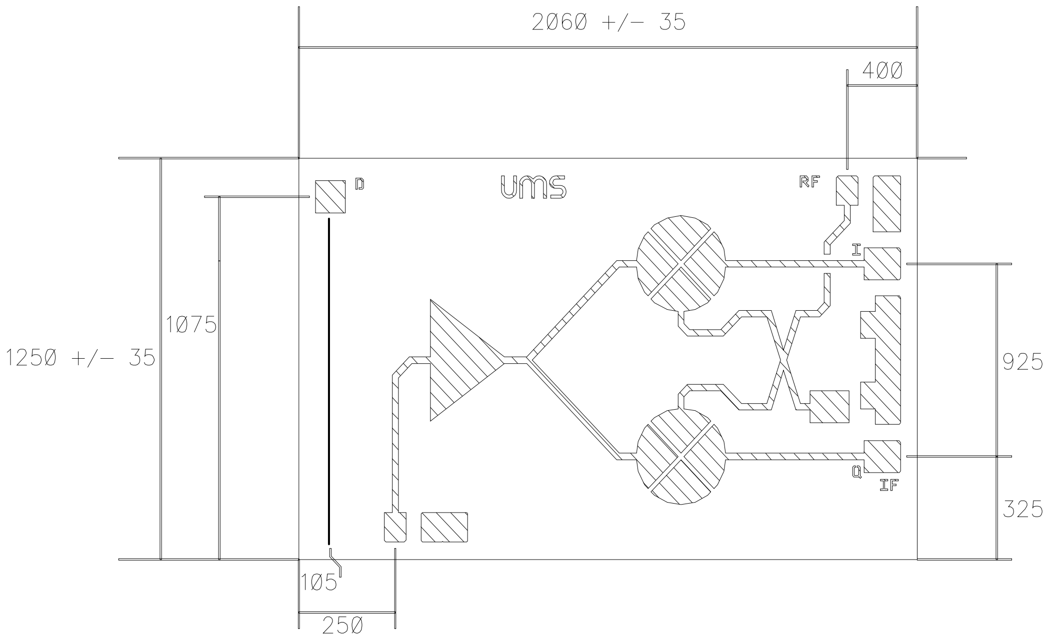
Route Départementale 128, B.P.46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0)1 69 33 03 08 - Fax : +33 (0)1 69 33 03 09

united monolithic semiconductors

Chip Assembly and Mechanical Data



Note: Supply feed should be bypassed. 25µm diameter gold wire is recommended



Chip Mechanical Data and Pin references

(Chip thickness: 100µm. All dimensions are in micrometers)

Route Départementale 128, B.P.46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0)1 69 33 03 08 - Fax : +33 (0)1 69 33 03 09

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS products.

Ordering Information

Chip form: CHM1294-99F/00

Route Départementale 128, B.P.46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0)1 69 33 03 08 - Fax : +33 (0)1 69 33 03 09