Microwave Wideband Synthesizer with Integrated VCO

FEATURES

- Output frequency range: 800 MHz to 12.8 GHz
- Jitter = 18 fs_{RMS} (integration bandwidth: 100 Hz to 100 MHz)
- Jitter = 27 fs_{RMS} (ADC SNR method)
- Wideband noise floor: −160 dBc/Hz at 12 GHz
- PLL specifications
  - −239 dBc/Hz: normalized in-band phase noise floor
  - −147 dBc/Hz: normalized in-band 1/f noise
  - Phase detector frequency up to 500 MHz
  - Reference input frequency up to 1000 MHz
  - Typical spurious f_{PFD}: −95 dBc at f_{OUT} = 12 GHz
- Reference input to output delay specifications
  - Device-to-device standard deviation: 3 ps
  - Temperature coefficient: 0.03 ps/°C
  - Adjustment step size: < ±0.1 ps
- Multichip output phase alignment
- 3.3 V and 5 V power supplies
- 7 mm × 7 mm 48-lead LGA

APPLICATIONS

- High performance data converter and MxFE clocking
- Wireless infrastructure (MC-GSM, 5G)
- Test and measurement

GENERAL DESCRIPTION

The ADF4377 is a high performance, ultralow jitter, dual output integer-N phased locked loop (PLL) with an integrated voltage controlled oscillator (VCO) ideally suited for data converter and mixed signal front end (MxFE) clock applications. The high performance PLL has a figure of merit of −239 dBc/Hz, ultralow 1/f noise, and a high phase frequency detector (PFD) frequency that can achieve ultralow in-band noise and integrated jitter. The fundamental VCO and output divider of the ADF4377 generate frequencies from 800 MHz to 12.8 GHz. The ADF4377 integrates all necessary power supply bypass capacitors, saving board space on compact boards.

For multiple data converter and MxFE clock applications, the ADF4377 simplifies clock alignment and calibration routines required with other clock solutions by implementing the automatic reference to output synchronization feature, the matched reference to output delays across process, voltage, and temperature feature, and the less than ±0.1 ps, jitter free reference to output delay adjustment capability feature.

These features allow for predictable and precise multichip clock and system reference (SYSREF) alignment. JESD204B and JESD204C Subclass 1 solutions are supported by pairing the ADF4377 with an integrated circuit (IC) that distributes pairs of reference and SYSREF signals.

FUNCTIONAL BLOCK DIAGRAM

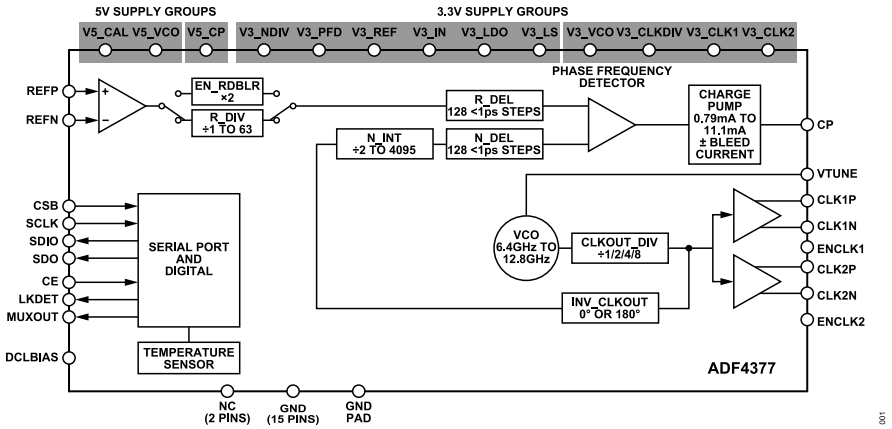

Figure 1.

Rev. 0

DOCUMENT FEEDBACK
TECHNICAL SUPPORT

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REVISION HISTORY

10/2022—Revision 0: Initial Version

SPECIFICATIONS

3.3 V Supply Group 1 pins voltage ($V_{3.3V\_1}$) = 3.3 V Supply Group 2 pins voltage ($V_{3.3V\_2}$) = 3.15 V to 3.45 V, V_{V5_VCO} = V_{V5_CP} = V_{V5_CAL} = 4.75 V to 5.25 V, all voltages are with respect to GND, T_A = −40°C to +105°C, operating temperature range, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE INPUTS (REFP, REFN)						
Input Frequency	f_{REF}	10		1000	MHz	
Input Signal Level	V_{REF}	0.5		2.6	V p-p	Refer to Figure 61
Minimum Input Slew Rate			100		V/µs	
Input Duty Cycle			50		%	
Self-Bias Voltage			1.85		V	
Input Resistance			3		kΩ	Differential
Input Capacitance			1		pF	Differential
Input Current			−2		µA	
Reference Peak Detector						
Input Frequency		10		1000	MHz	
Minimum Input Signal Detected (REF_OK Bit = 1)			200		mV p-p	f_{REF} = 100 MHz, single-ended sine wave
Maximum Input Signal Not Detected (REF_OK Bit = 0)			160		mV p-p	f_{REF} = 100 MHz, single-ended sine wave
REFERENCE DIVIDER		1		63		All integers included
REFERENCE DOUBLER						
Input Frequency		10		250	MHz	EN_RDBLR = 1
PHASE/FREQUENCY DETECTOR (PFD)						
Input Frequency	f_{PFD}	3		500	MHz	
CHARGE PUMP (CP)						
Output Current Range	I_{CP}		0.79 to 11.1		mA	Set by CP_I bit fields
Output Current Source/Sink Accuracy			±2		%	All CP_I bit field settings, V_{CP} = V_{V5_CP}/2
Output Current Source/Sink Matching			±2		%	All CP_I bit field settings, V_{CP} = V_{V5_CP}/2
Output Current vs. Output Volt Sensitivity			0.2		%/V	V_{CP}[1]
Output Current vs. Temperature			280		ppm/°C	V_{CP} = V_{V5_CP}/2
Output High-Z Leakage Current			−0.01		µA	Minimum I_{CP}, V_{CP}[1]
			−0.3		µA	Maximum I_{CP}, V_{CP}[1]
VCO						
Frequency Range	f_{VCO}	6.4		12.8	GHz	
Tuning Sensitivity	K_{VCO}		0.75 to 1.25		%Hz/V	K_{VCO}[2, 3]
VCO Calibration Frequency	f_{DIV_RCLK}			125	MHz	Must set DCLK_MODE = 1, when f_{DIV_RCLK} > 80 MHz
FEEDBACK DIVIDER (N) AND CLOCK OUTPUT DIVIDER (O)						
N		2		4095		All integers included
O		1		8		1, 2, 4, 8
CLOCK OUTPUTS (CLK1P and CLK1N, CLK2P and CLK2N)						Differential termination = 100 Ω for all clock output specifications unless noted
Output Frequency	f_{OUT}	0.8		12.8	GHz	
Output Differential Voltage	V_{OD}		320		mV	V_{OH} − V_{OL} measurement across a differential pair with output driver not toggling and CLKOUT1_OP = CLKOUT2_OP = 0
			420		mV	V_{OH} − V_{OL} measurement across a differential pair with output driver not toggling and CLKOUT1_OP = CLKOUT2_OP = 1

SPECIFICATIONS

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
			530		mV	V_{OH} − V_{OL} measurement across a differential pair with output driver not toggling and CLKOUT1_OP = CLKOUT2_OP = 2
			640		mV	V_{OH} − V_{OL} measurement across a differential pair with output driver not toggling and CLKOUT1_OP = CLKOUT2_OP = 3
Output Resistance			100		Ω	Differential
Output Common Mode			V_{CLK} − 1.2 × V_{OD}		V	
Output Rise Time	t_R		15		ps	20% to 80%, CLKOUT1_OP = CLKOUT2_OP = 1
Output Fall Time	t_F		15		ps	80% to 20%, CLKOUT1_OP = CLKOUT2_OP = 1
Output Duty Cycle			50		%	
Skew, CLK1P to CLK2P			±0.5		ps	
REFERENCE INPUT TO OUTPUT DELAY						Device setup[4] for all delay specifications unless noted, measure rising reference edge at REFP input to rising edge at CLK1P output
Propagation Delay Temperature Coefficient	t_{PD-TC}		0.03		ps/°C	REF_SEL = 0
Propagation Delay	t_{PD}		104		ps	f_{OUT} = 12 GHz, f_{REF} = 200 MHz, f_{PFD} = 200 MHz, R_DIV = 1, REF_SEL = 0
			112		ps	f_{OUT} = 6 GHz, f_{REF} = 200 MHz, f_{PFD} = 200 MHz, R_DIV = 1, REF_SEL = 0
			110		ps	f_{OUT} = 3 GHz, f_{REF} = 200 MHz, f_{PFD} = 200 MHz, R_DIV = 1, REF_SEL = 0
			110		ps	f_{OUT} = 1.6 GHz, f_{REF} = 200 MHz, f_{PFD} = 200 MHz, R_DIV = 1, REF_SEL = 0
			122		ps	f_{OUT} = 3 GHz, f_{REF} = 100 MHz, f_{PFD} = 200 MHz, EN_RDBLR = 1, REF_SEL = 0
N_DEL, R_DEL Step Size			1		ps	
N_DEL Range			110		ps	N_DEL = 127, R_DEL = 0
R_DEL Range			127		ps	N_DEL = 0, R_DEL = 127
LOGIC INPUTS (CSB, SCLK, SDIO, ENCLK1, and ENCLK2)						
Input High Voltage	V_{INH}	1.2			V	
Input Low Voltage	V_{INL}			0.6	V	
Input Current	I_{IH}/I_{IL}			±1	µA	
Input Capacitance (CSB, SCLK, ENCLK1, ENCLK2)	C_{IN}		1		pF	
SDIO	$C_{IN-SDIO}$		2		pF	
LOGIC INPUT (CE Pin)						
Input High Voltage	V_{INH-CE}	1.8			V	
Input Low Voltage	V_{INL-CE}			0.8	V	
Input Current	I_{IH-CE}/I_{IL-CE}			±1	µA	
Input Capacitance	C_{IN-CE}		1		pF	
LOGIC OUTPUTS (SDIO, SDO, LKDET, MUXOUT)						
Output High Voltage (1.8 V Mode)	V_{OH}	1.5	1.8		V	I_{OH} = 500 µA, 1.8 V output selected (default setting)
Output High Voltage (3.3 V Mode)	V_{OH-3V}	$V_{3.3V}$ − 0.4				I_{OH} = 500 µA, 3.3 V output selected, set by voltage on V3_LDO pin
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 500 µA
SDO High-Z Leakage	I_{ZH}/I_{ZL}			±1	µA	

SPECIFICATIONS

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLIES						Device setup[5] for all supply current specifications, unless noted
V5_VCO Supply Range	V_{V5_VCO}	4.75	5	5.25	V	
V5_CAL Supply Range	V_{V5_CAL}	4.75	5	5.25	V	
V5_CP Supply Range	V_{V5_CP}	4.75	5	5.25	V	
$V_{3.3V\_1}$ Supply Range	$V_{3.3V\_1}$	3.15	3.3	3.45	V	3.3 V Power Supply Group 1 (V3_LS, V3_LDO, V3_REF, V3_PFD, V3_NDIV, V3_IN)
$V_{3.3V\_2}$ Supply Range	$V_{3.3V\_2}$	3.15	3.3	3.45	V	3.3 V Power Supply Group 2 (V3_CLK1, V3_CLK2, V3_VCO, V3_CLKDIV)
V5_VCO Supply Current	I_{V5_VCO}		90	135	mA	f_{OUT} = 12.8 GHz
			170	220	mA	f_{OUT} = 6.4 GHz, CLKOUT_DIV = 0
V5_CAL Supply Current	I_{V5_CAL}		50	160	µA	
			8		mA	During VCO calibration
V5_CP Supply Current	I_{V5_CP}		55	65	mA	CP current (I_{CP}) = 11.1 mA, CP_I = 15
			26		mA	I_{CP} = 0.79 mA, CP_I = 0
			55.2		mA	CP_I = 15, EN_BLEED = 1, BLEED_I[1:0] = 512
$V_{3.3V\_1}$ Supply Current	$I_{3.3V\_1}$		173	200	mA	
			173		mA	R_DEL = 127
			176		mA	REF_SEL = BST_REF = FILT_REF = 1
			173		mA	PD_RDET = 1
			189		mA	During VCO calibration, EN_DRCLK = EN_DNCLK = EN_ADC_CLK = 1
$V_{3.3V\_2}$ Supply Current	$I_{3.3V\_2}$		195		mA	CLKOUT1_OP = CLKOUT2_OP = 0, CLKOUT_DIV = 3
			169		mA	CLKOUT1_OP = CLKOUT2_OP = 0
			179		mA	CLKOUT1_OP = CLKOUT2_OP = 1
			188		mA	CLKOUT1_OP = CLKOUT2_OP = 2
			197		mA	CLKOUT1_OP = CLKOUT2_OP = 3,
			139	160	mA	ENCLK2 = low
Typical Power Dissipation	P_{DIS}		1.75 to 1.9		W	ENCLK2 = low, $V_{3.3V\_1}$ = $V_{3.3V\_2}$ = 3.3 V, V_{V5_VCO} = 5 V, VCO Core 2 and Core 3
			1.95 to 2.15		W	ENCLK2 = low, $V_{3.3V\_1}$ = $V_{3.3V\_2}$ = 3.3 V, V_{V5_VCO} = 5 V, VCO Core 0 and Core 1
Typical Power Down Current						
3.3 V Supplies			11	15	mA	PD_ALL = 1, $I_{3.3V\_1}$ + $I_{3.3V\_2}$
5 V Supplies			350	750	µA	PD_ALL = 1, I_{V5_VCO} + I_{V5_CAL} + I_{V5_CP}
Typical Disable Current						
3.3 V Supplies			0.1	1.5	mA	CE = low, $I_{3.3V\_1}$ + $I_{3.3V\_2}$
5 V Supplies			350	750	µA	CE = low, I_{V5_VCO} + I_{V5_CAL} + I_{V5_CP}
CLOCK OUTPUT NOISE CHARACTERISTICS						
12 GHz Output Frequency						Device setup[6], f_{OUT} = 12 GHz
Phase Noise Floor			−160		dBc/Hz	
RMS Jitter						
12 kHz to 20 MHz Integration			17.6		fs_{rms}	
100 Hz to 100 MHz Integration			18		fs_{rms}	
Equivalent ADC SNR Method[7]			27		fs_{rms}	
10 GHz Output Frequency						Device setup[6], f_{OUT} = 10 GHz
Phase Noise Floor			−159.5		dBc/Hz	
RMS Jitter						

SPECIFICATIONS

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
12 kHz to 20 MHz Integration			18.5		fs_{rms}	
100 Hz to 100 MHz Integration			18.7		fs_{rms}	
Equivalent ADC SNR Method[7]			30		fs_{rms}	
8 GHz Output Frequency						Device setup[6], f_{OUT} = 8 GHz
Phase Noise Floor			−160.5		dBc/Hz	
RMS Jitter						
12 kHz to 20 MHz Integration			18		fs_{rms}	
100 Hz to 100 MHz Integration			18.3		fs_{rms}	
Equivalent ADC SNR Method[7]			30		fs_{rms}	
6 GHz Output Frequency						Device setup[6], f_{OUT} = 6 GHz
Phase Noise Floor			−163		dBc/Hz	
RMS Jitter						
12 kHz to 20 MHz Integration			17.7		fs_{rms}	
100 Hz to 100 MHz Integration			18.3		fs_{rms}	
Equivalent ADC SNR Method[7]			27		fs_{rms}	
3 GHz Output Frequency						Device setup[6], f_{OUT} = 3 GHz
Phase Noise Floor			−165.7		dBc/Hz	
RMS Jitter						
12 kHz to 20 MHz Integration			17.7		fs_{rms}	
100 Hz to 100 MHz Integration			18.3		fs_{rms}	
Equivalent ADC SNR Method[7]			28		fs_{rms}	
1.5 GHz Output Frequency						Device setup[6], f_{OUT} = 1.5 GHz
Phase Noise Floor			−169.5		dBc/Hz	
RMS Jitter						
12 kHz to 20 MHz Integration			19.5		fs_{rms}	
100 Hz to 100 MHz Integration			20.5		fs_{rms}	
Equivalent ADC SNR Method[7]			29		fs_{rms}	
Normalized In-Band Phase Noise Floor[8]	L_{NORM}		−239		dBc/Hz	
Normalized 1/f Phase Noise Floor[8]	$L_{1/f}$		−287		dBc/Hz	Normalized to 1 Hz
	L_{1/f_1G_10k}		−147		dBc/Hz	Normalized to 1 GHz at 10 kHz offset
Spurious						
f_{REF}			−105		dBc	LOCKED bit = 1, f_{REF} = 100 MHz, f_{PFD} = 200 MHz, f_{OUT} = 12 GHz
f_{PFD}			−95		dBc	LOCKED bit = 1, f_{REF} = 100 MHz, f_{PFD} = 200 MHz, f_{OUT} = 12 GHz

SPECIFICATIONS

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE SENSOR (ADC)						
ADC Clock Frequency	f_{ADC_CLK}			400	kHz	ADC clock divider output
ADC Clock Divider Frequency	f_{ADC_CLKDIV}			125	MHz	ADC clock divider input
Resolution				8	Bits	

[1] $1.2\ V < V_{CP} < 3.4\ V$.

[2] Valid for $1.60\ V \le V_{VTUNE} \le 2.85\ V$ with device calibrated after a power cycle or software power-on reset.

[3] Based on characterization.

[4] Device setup: f_{REF} = 200 MHz, f_{PFD} = 200 MHz, f_{OUT} = 3000 MHz, ENCLK1 = ENCLK2 = CE = HIGH. Bit fields: R_DEL= 0, N_DEL = 0, CP_I = 15, CLKOUT1_OP = 1, CLKOUT2_OP = 1, REF_SEL = 0, EN_BLEED = 0, PD_RDET = 0, PD_ADC = 0, PD_LD = 0, LOCKED = 1.

[5] Device Setup: f_{REF} = 100 MHz, f_{PFD} = 200 MHz, f_{OUT} = 12.8 GHz, ENCLK1 = ENCLK2 = CE = HIGH. Bit fields: R_DEL= 0, N_DEL = 0, CP_I = 15, CLKOUT1_OP = 1, CLKOUT2_OP = 1, REF_SEL = 0, EN_BLEED = 0, PD_RDET = 0, PD_ADC = 0, PD_LD = 0, LOCKED = 1, EN_DNCLK = EN_DRCLK = EN_ADC_CLK = 0.

[6] Device Setup: f_{REF} = 1000 MHz, f_{PFD} = 500 MHz, ENCLK1 = ENCLK2 = CE = HIGH. Bit fields: R_DEL = 0, N_DEL_0, CP_I = 15, CLKOUT1_OP = 1, CLKOUT2_OP = 1, REF_SEL = 0, EN_BLEED = 0, PD_RDET = 0, PD_ADC = 0, PD_LD = 0, LOCKED = 1, the reference oscillator is the 0-CEGM-058AWEL-R-1GHz from NEL Frequency Control.

[7] Phase integration range 1 kHz to f_{OUT} produces the same result as when clocking an ADC.

[8] Refer to Equation 18 through Equation 22. These values are modeled in ADIsimPLL™.

SERIAL INTERFACE TIMING CHARACTERISTICS

$V_{3.3V\_1}$ = $V_{3.3V\_2}$ = 3.15 V to 3.45 V, V_{V5_VCO} = V_{V5_CP} = V_{V5_CAL} = 4.75 V to 5.25 V, all voltages are with respect to GND, T_A = −40°C to +105°C, operating temperature range, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SERIAL INTERFACE (CSB, SCLK, SDIO, SDO)						See Figure 2, Figure 3, and Figure 4
SCLK Frequency	f_{SCLK}			65	MHz	$f_{SCLK} = 1/t_{SCLK}$
SCLK Pulse Width High	t_{HIGH}	7.6			ns	
SCLK Pulse Width Low	t_{LOW}	7.6			ns	
SDIO Setup Time	t_{DS}	3			ns	
SDIO Hold Time	t_{DH}	3			ns	
SCLK Fall Edge to SDIO Valid Prop Delay	t_{ACCESS_SDIO}	7.6			ns	
SCLK Fall Edge to SDO Valid Prop Delay	t_{ACCESS_SDO}	7.6			ns	
CSB Rising Edge to SDIO High-Z	t_Z	7.6			ns	
CSB Falling Edge to SCLK Rise Setup Time	t_S	3			ns	
SCLK Rising Edge to CSB Rise Hold Time	t_H	3			ns	

Timing Diagrams

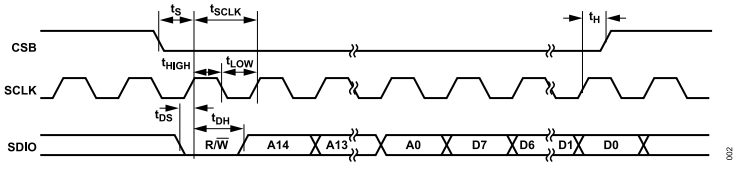

Figure 2. Write Timing Diagram

SPECIFICATIONS

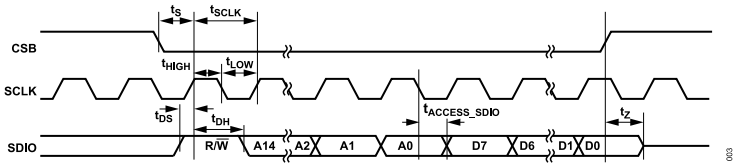

Figure 3. 3-Wire Read Timing Diagram (SDO_ACTIVE = 0)

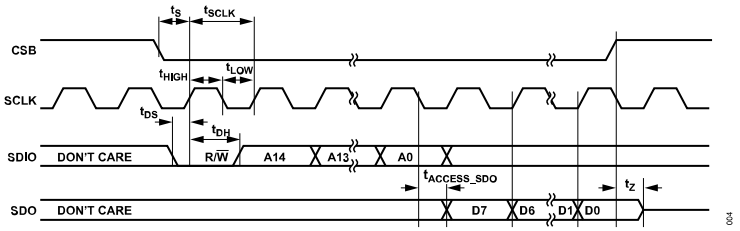

Figure 4. 4-Wire Read Timing Diagram (SDO_ACTIVE = 1)

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3. Absolute Maximum Ratings

Parameter	Rating
$V_{3.3V\_1}$ (V3_LS, V3_LDO, V3_REF, V3_PFD, V3_NDIV) to GND	−0.3 V to +3.6 V
$V_{3.3V\_2}$ (V3_VCO, V3_CLKDIV, V3_CLK1, V3_CLK2) to GND	−0.3 V to +3.6 V
V_{5V} (V5_CAL, V5_VCO, V5_CP) to GND	−0.3 V to +5.5 V
Voltage on CP Pin	−0.3 V to V_{V5_CP} + 0.3 V
Digital Outputs (MUXOUT, LKDET, SDO, SDIO)	5 mA
CLK1P, CLK1N, CLK2P, CLK2N	Maximum (GND − 0.3 V, $V_{3.3V\_2}$ − 1.2 V) to $V_{3.3V\_2}$ + 0.3 V
REFP, REFN	−0.65 V to $V_{3.3V\_1}$ + 0.65 V
Voltage on All Other Pins	−0.3 V to $V_{3.3V\_1}$ + 0.3 V
REFP to REFN, when $V_{3.3V\_1}$ > 3 V	±1.35 V
Operating Junction Temperature Range[1]	−40°C to +125°C
Storage Temperature Range	−40°C to +125°C
Maximum Junction Temperature	125°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	30 s

[1] Device is guaranteed to meet the specified performance limits over the full operating junction temperature range.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

TRANSISTOR COUNT

The transistor count for the ADF4377 is 114258 (CMOS) and 2941 (bipolar).

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required. θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	$\theta_{JC\text{-}TOP}$	$\theta_{JC\text{-}BOTTOM}$	θ_{JB}	Ψ_{JT}	Ψ_{JB}	Unit
CC-48-6[1]	28.7	25.8	6.3	13.1	2.6	13.7	°C/W

[1] Test Condition 1: thermal impedance simulated values are based on use of a 4-layer PCB with the thermal impedance paddle soldered to a ground plane.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDDEC JS-001.
Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADF4377

Table 5. ADF4377, 48-Lead LGA

ESD Model	Withstand Threshold (V)	Class
HBM	3500	2
CDM	1250	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

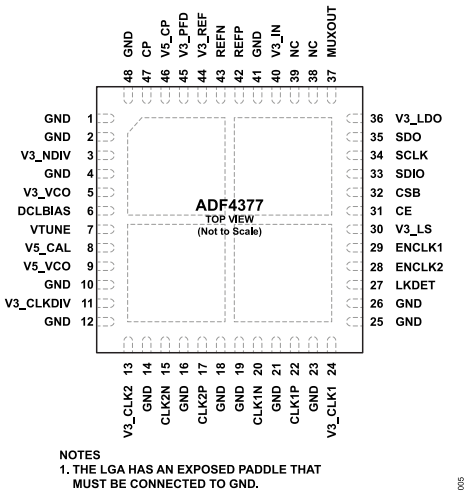

Figure 5. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4, 10, 12, 14, 16, 18, 19, 21, 23, 25, 26, 41, 48	GND	Negative Power Supply (Ground). These pins must be tied directly to the ground pad.
3	V3_NDIV	3.15 V to 3.45 V Positive Power Supply Pin for the PLL Feedback Divider Circuitry. Short this pin to the other pins in 3.3 V Power Supply Group 1.
5	V3_VCO	3.15 V to 3.45 V Positive Power Supply Pin for the 3.3 V Portion of the VCO Circuitry. Short this pin to the other pins in 3.3 V Power Supply Group 2.
6	DCLBIAS	Do not connect to this pin.
7	VTUNE	VCO Tuning Input. This frequency control pin is normally connected to the external loop filter.
8	V5_CAL	4.75 V to 5.25 V Positive Power Supply Pin for VCO Calibration Circuitry. This pin can be shorted to the V5_VCO supply plane.
9	V5_VCO	4.75 V to 5.25 V Positive Power Supply Pin for the 5 V Portion of the VCO Circuitry.
11	V3_CLKDIV	3.15 V to 3.45 V Positive Power Supply Pin for the Output Divider Circuitry. Short this pin to the other pins in 3.3 V Power Supply Group 2.
13	V3_CLK2	3.15 V to 3.45 V Positive Power Supply Pin for the Clock 2 Buffer Circuitry. Short this pin to the other pins in 3.3 V Power Supply Group 2.
15, 17	CLK2N, CLK2P	Clock 2 Output Signal. The VCO output divider is buffered and presented differentially on these pins. The outputs have 50 Ω (typical) output resistance per side (100 Ω differential). The far end of the transmission line is typically terminated with 100 Ω connected across the outputs. The output amplitude is programmable via the serial port.
20, 22	CLK1N, CLK1P	Clock 1 Output Signal. The VCO output divider is buffered and presented differentially on these pins. The outputs have 50 Ω (typical) output resistance per side (100 Ω differential). The far end of the transmission line is typically terminated with 100 Ω connected across the outputs. The output amplitude is programmable via the serial port.
24	V3_CLK1	3.15 V to 3.45 V Positive Power Supply Pin for the Clock 1 Buffer Circuitry. Short this pin to the other pins in 3.3 V Power Supply Group 2.
27	LKDET	PLL Lock Detect. This output presents the lock status of the PLL. PLL is locked when the LKDET pin is a logic high.
28	ENCLK2	Enable Clock 2 Output Buffer. 1.8 V and 3.3 V compatible CMOS input. When ENCLK1 = high, the CLK2P and CLK2N output buffer is active. When ENCLK2 = low, the CLK2P and CLK2N output buffer is powered down.
29	ENCLK1	Enable Clock 1 Output Buffer. 1.8 V and 3.3 V compatible CMOS input. When ENCLK1 = high, the CLK1P and CLK1N output buffer is active. When ENCLK1 = low, the CLK1P and CLK1N output buffer is powered down.
30	V3_LS	3.15 V to 3.45 V Positive Power Supply Pin for the Internal Level Shift Circuitry. Short this pin to the other pins in 3.3 V Power Supply Group 1.
31	CE	Chip Enable. 3.3 V CMOS input. Does not support 1.8 V CMOS levels. This CMOS input enables the device when driven high. A logic low disables the device, putting the device in a full power-down state, causing the registers to reset. Conversely, the PD_ALL bit powers down the device, but does not reset the registers.
32	CSB	Serial Port Chip Select. 1.8 V and 3.3 V compatible CMOS input. This CMOS input initiates a serial port communication burst when driven low, ending the burst when driven back high.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
33	SDIO	Serial Data Input/Output. 1.8 V and 3.3 V programmable CMOS input/output. When configured as an input, the serial port uses this CMOS input for data. In 3-wire readback mode (default mode), this pin outputs data from the serial port during a read communication burst.
34	SCLK	Serial Port Clock. 1.8 V and 3.3 V compatible. This CMOS input clocks serial port input data on its rising edge.
35	SDO	Optional Serial Data Output. 1.8 V and 3.3 V programmable CMOS output. In 3-wire mode (default mode), this three state CMOS pin remains in a high impedance state. In 4-wire readback mode, this pin presents data from the serial port during a read communication burst. When the $\overline{CS}$ is deasserted, SDO returns to a high impedance. Optionally, attach a resistor of > 200 kΩ to prevent a floating output.
36	V3_LDO	3.15 V to 3.45 V Positive Power Supply Pin for the Internal LDO Circuitry. Short this pin to the other pins in 3.3 V Power Supply Group 1.
37	MUXOUT	Internal Device Mux Output. This output pin can be connected to multiple internal nodes for factory test and debug purposes.
38, 39	NC	No Connect or GND. These pins are connected internally to ESD diodes.
40	V3_IN	3.15 V to 3.45 V Positive Power Supply. Short this pin to the other pins in 3.3 V Power Supply Group 1.
42, 43	REFP, REFN	Reference Input Signal. This differential input is buffered with a delay matched amplifier (DMA) for well controlled reference to output propagation delays (default mode, REF_SEL = 0). For low slew rate reference input signals, an alternate low noise amplifier (LNA) can be selected via the serial port (REF_SEL = 1). Reference inputs are self-biased and must be ac-coupled with 1 µF capacitors. Reference inputs accept differential or single-ended inputs.
44	V3_REF	3.15 V to 3.45 V Positive Power Supply Pin for the PLL Reference Circuitry. Short this pin to the other pins in 3.3 V Power Supply Group 1.
45	V3_PFD	3.15 V to 3.45 V Positive Power Supply Pin for PFD Circuitry. Short this pin to the other pins in 3.3 V Power Supply Group 1.
46	V5_CP	4.75 V to 5.25 V Positive Power Supply Pin for Charge Pump Circuitry. This pin must be isolated from the V5_VCO supply plane.
47	CP	Charge Pump Output. This bidirectional current output is normally connected to the external loop filter.
Exposed Pad	EP	Exposed Pad. Negative power supply (ground). The exposed pad must be soldered directly to the PCB land. The PCB land pattern must have multiple thermal vias to the ground plane for both low ground inductance and low thermal resistance.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{3.3V\_1}$ = $V_{3.3V\_2}$ = 3.3 V, V_{5V} = 5 V, all voltages are with respect to GND, T_A = 25°C, unless otherwise noted.

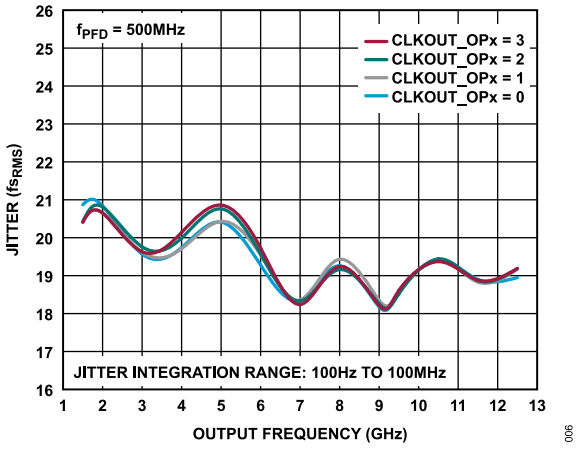

Figure 6. Jitter vs. Output Frequency at Various Output Amplitudes

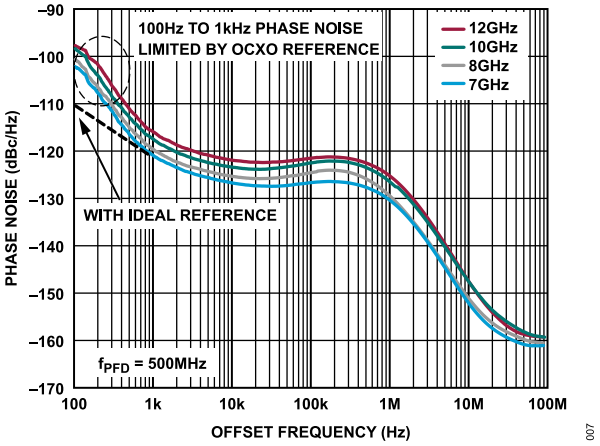

Figure 7. Closed Loop Phase Noise at Various Output Frequencies

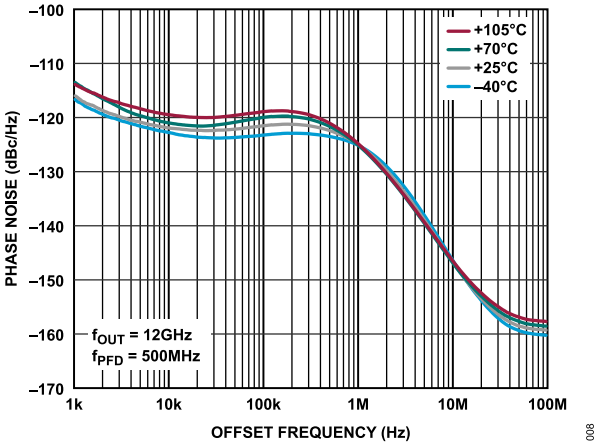

Figure 8. Closed Loop Phase Noise at Various Temperatures

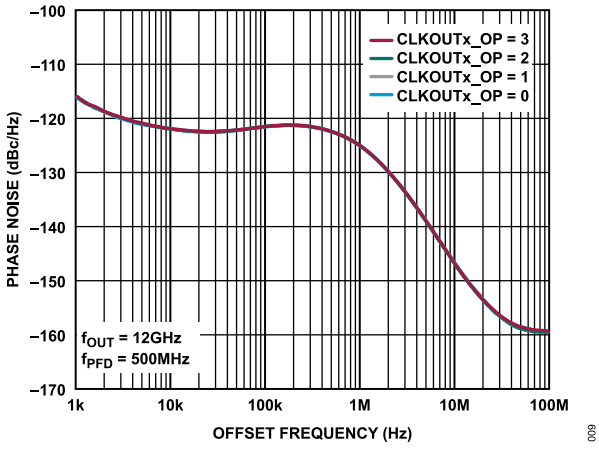

Figure 9. Closed Loop Phase Noise at Various Output Amplitudes

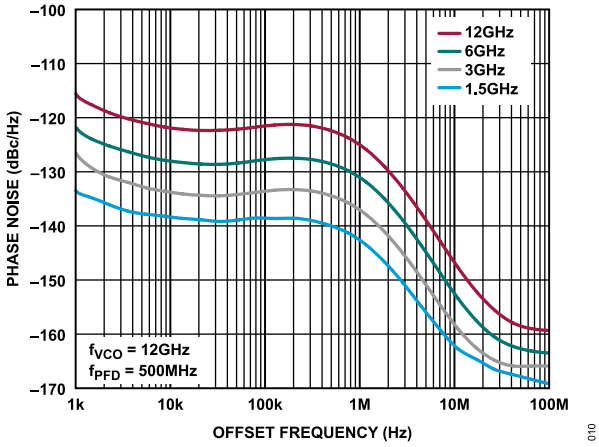

Figure 10. Closed Loop Phase Noise at Various CLKOUT_DIV Settings

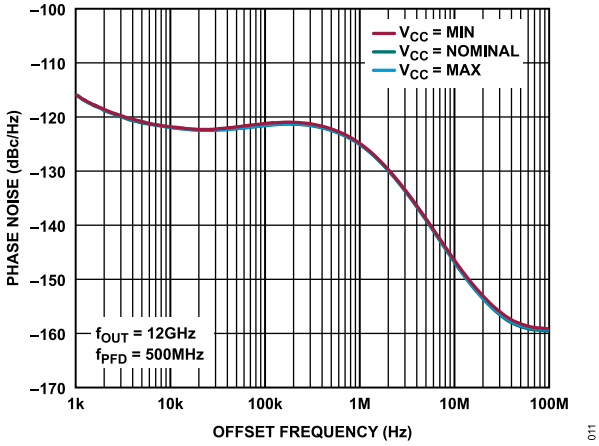

Figure 11. Closed Loop Phase Noise at Various Power Supply Voltages

TYPICAL PERFORMANCE CHARACTERISTICS

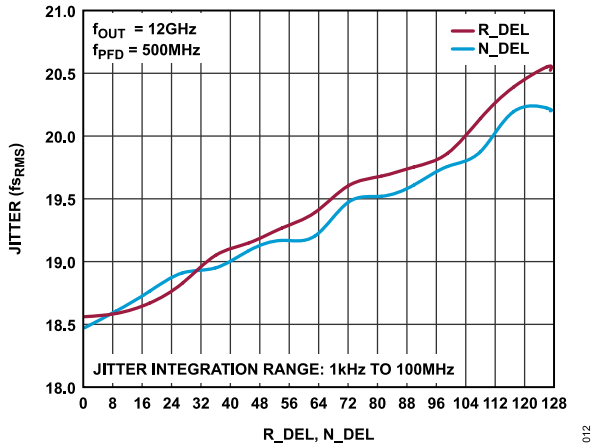

Figure 12. Jitter vs. R_DEL, N_DEL

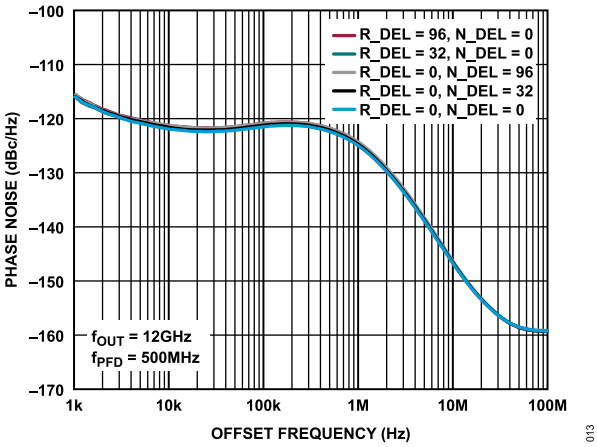

Figure 13. Closed Loop Phase Noise at Various R_DEL and N_DEL Settings

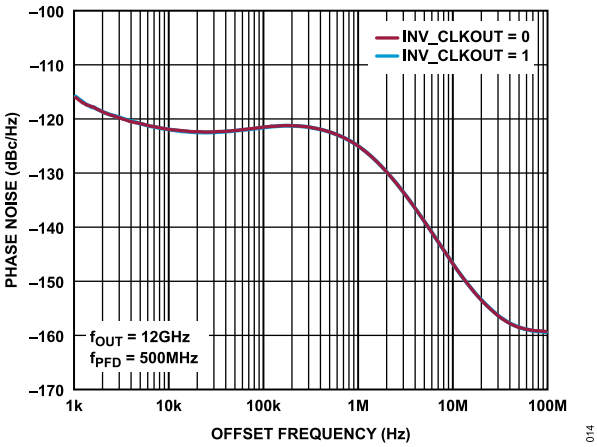

Figure 14. Closed Loop Phase Noise at Various Clock Invert Settings

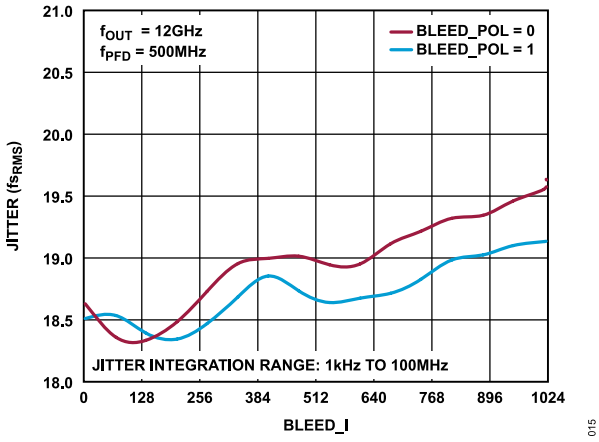

Figure 15. Jitter vs. BLEED_I

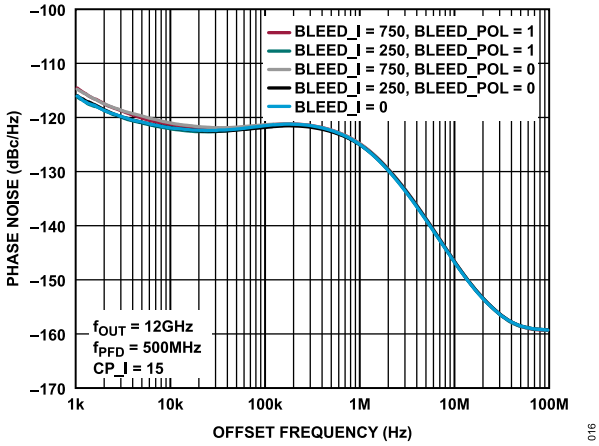

Figure 16. Closed Loop Phase Noise at Various Charge Pump Bleed Delays

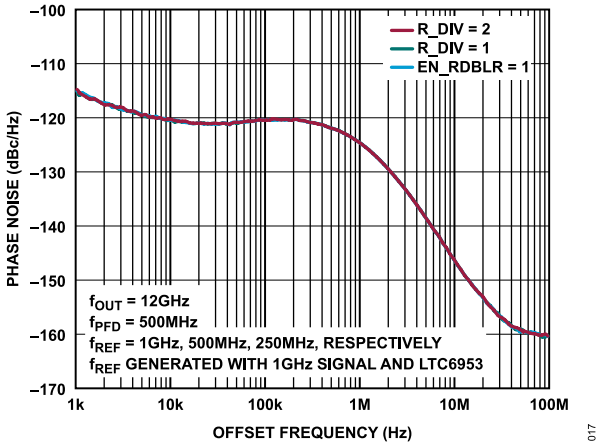

Figure 17. Closed Loop Phase Noise at Various Reference Doubler and Reference Divider Settings

TYPICAL PERFORMANCE CHARACTERISTICS

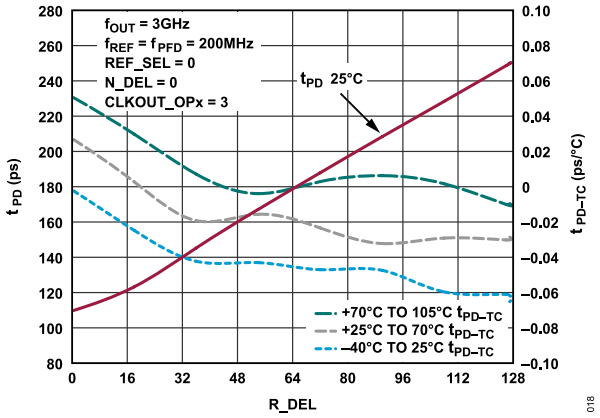

Figure 18. Propagation Delay (t_{PD}) and Propagation Delay Temperature Coefficient (t_{PD-TC}) vs. R_DEL

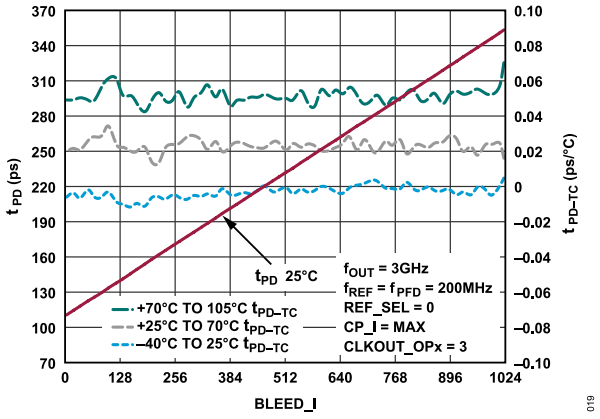

Figure 19. t_{PD} and t_{PD-TC} vs. BLEED_I , BLEED_POL = 0

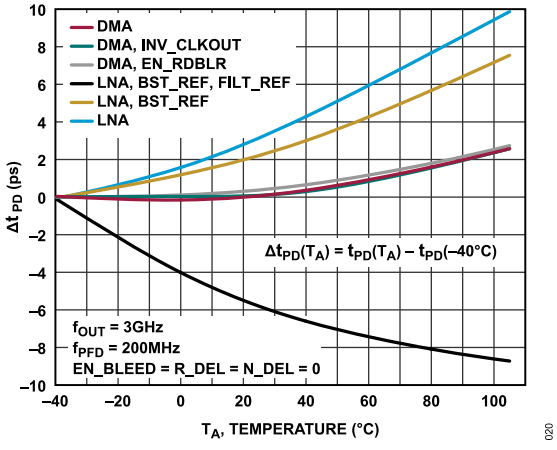

Figure 20. Delta Propagation Delay (Δt_{PD}) vs. T_A, Temperature, Device Configuration

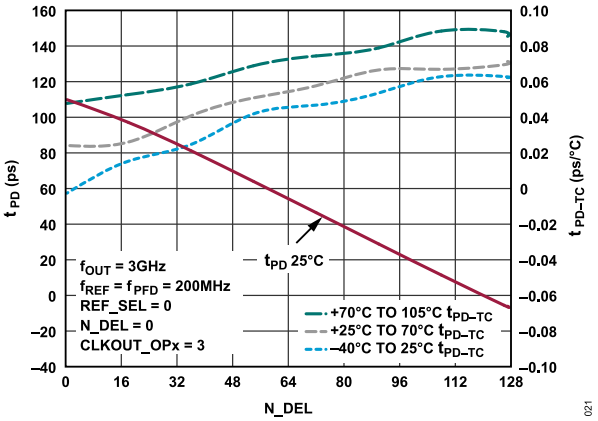

Figure 21. t_{PD} and t_{PD-TC} vs. N_DEL

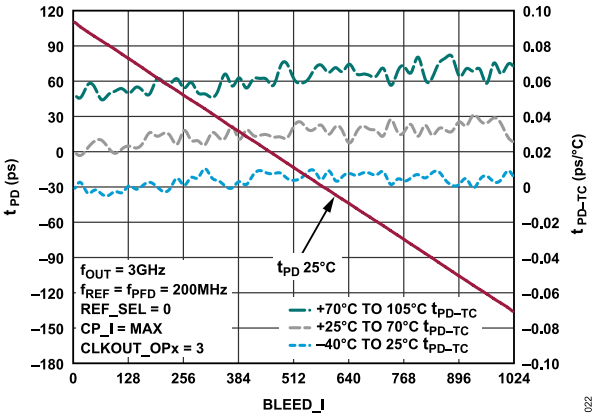

Figure 22. t_{PD} and t_{PD-TC} vs. BLEED_I, BLEED_POL = 1

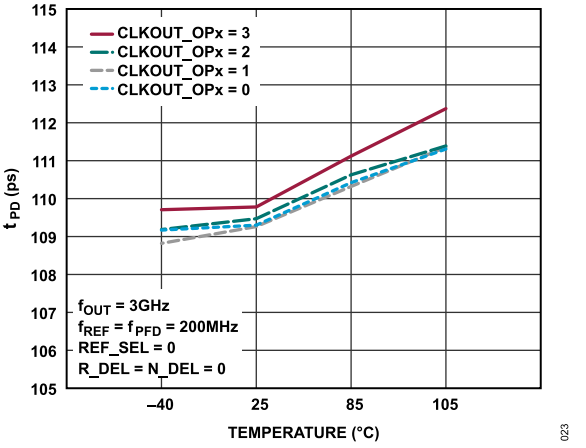

Figure 23. t_{PD} vs. Temperature, CLKOUT_OP Setting

TYPICAL PERFORMANCE CHARACTERISTICS

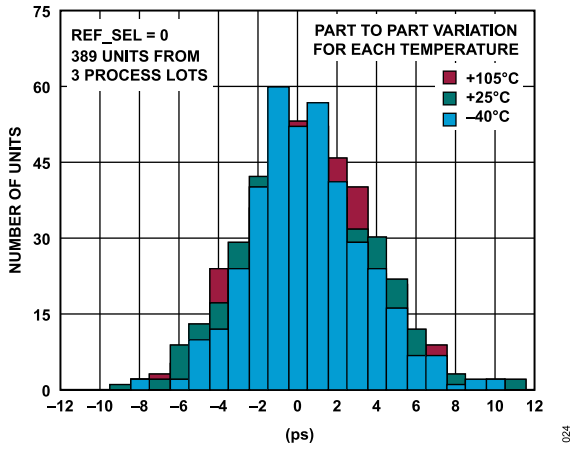

Figure 24. Normalized Propagation Delay (t_{PD}) Histogram

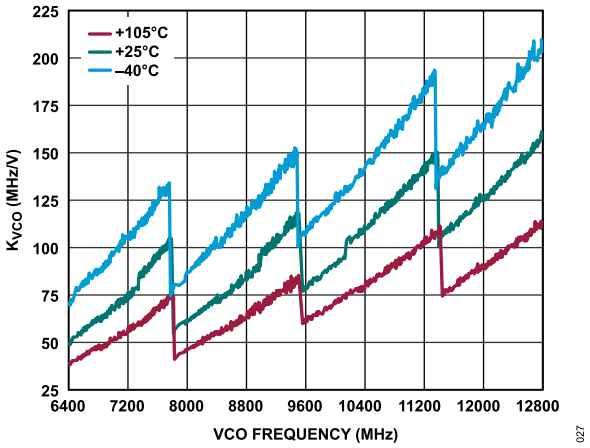

Figure 27. K_{VCO} at Various Frequencies and Temperatures

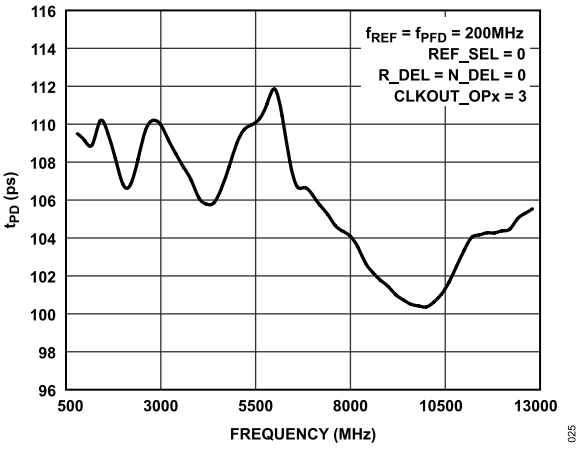

Figure 25. t_{PD} vs. Frequency

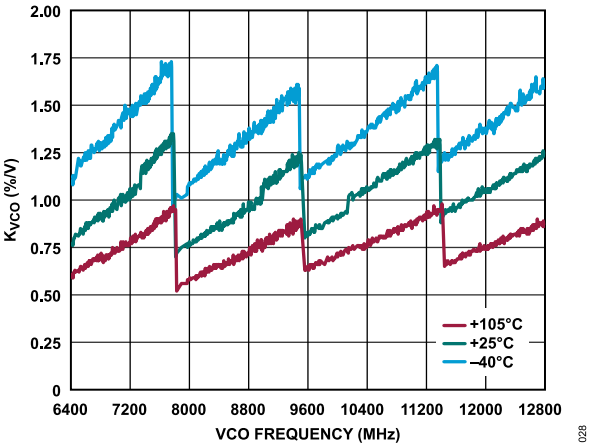

Figure 28. K_{VCO} Percentage at Various Frequencies and Temperatures

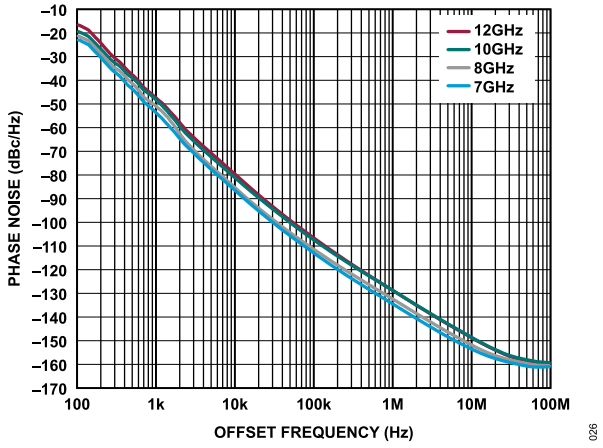

Figure 26. Open Loop VCO Phase Noise at Various Frequencies

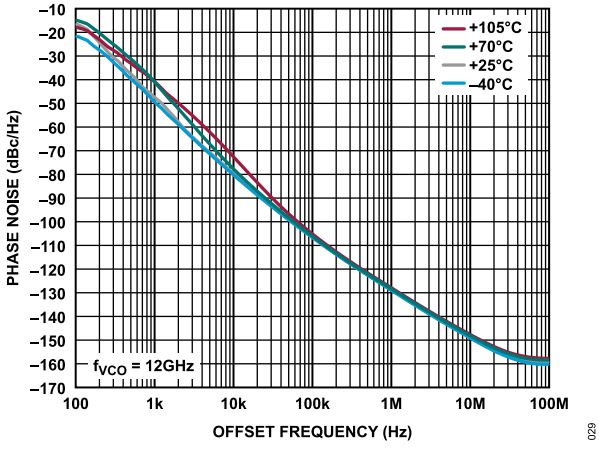

Figure 29. Open Loop VCO Phase Noise at Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

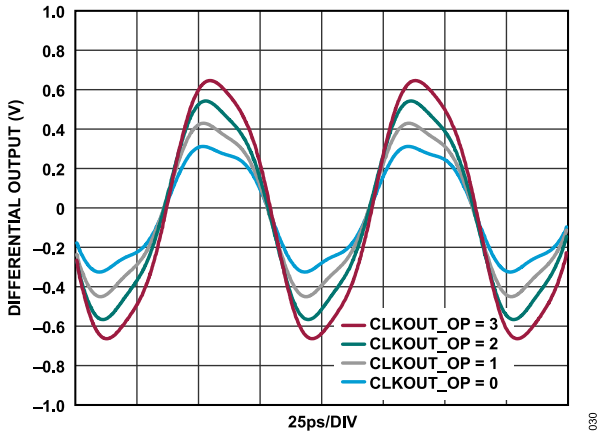

Figure 30. Differential Output at 12 GHz

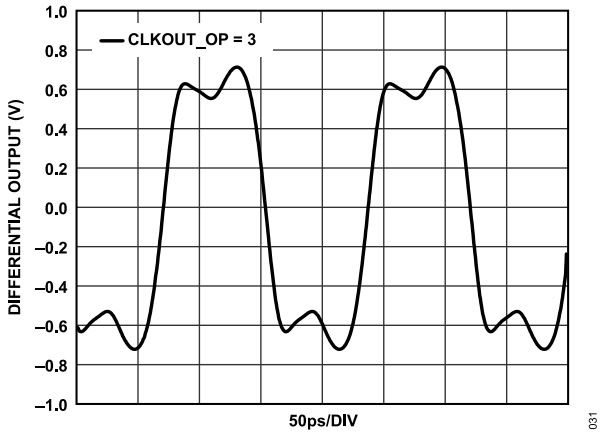

Figure 31. Differential Output at 6 GHz

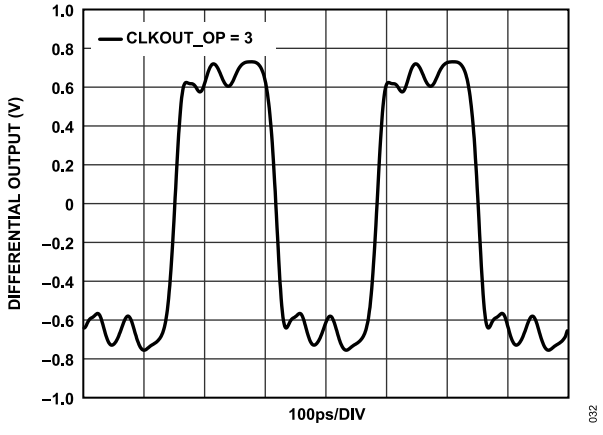

Figure 32. Differential Output at 3 GHz

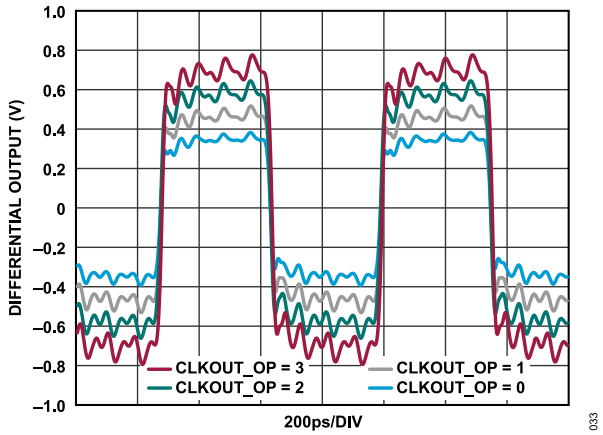

Figure 33. Differential Output at 1.5 GHz

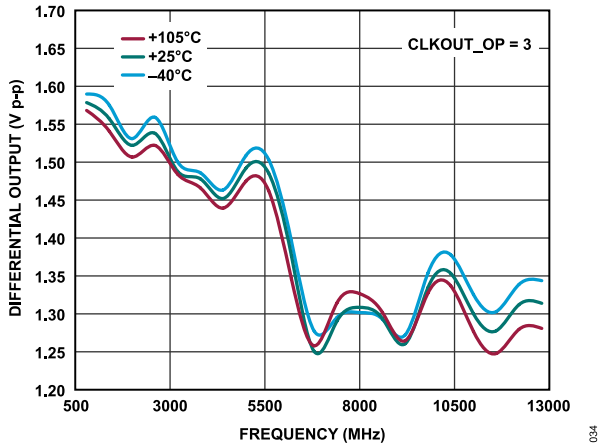

Figure 34. Differential Output vs. Frequency, Temperature

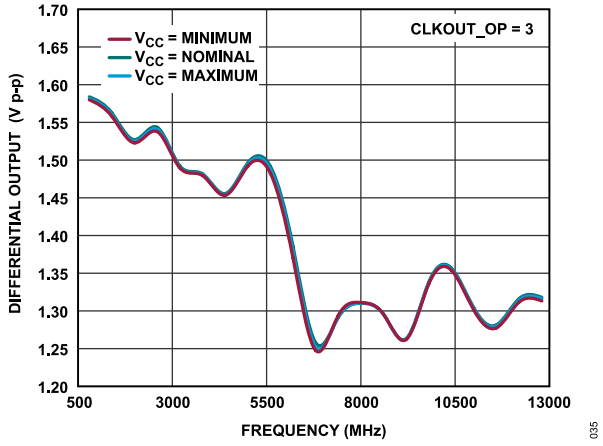

Figure 35. Differential Output vs. Frequency, Power Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

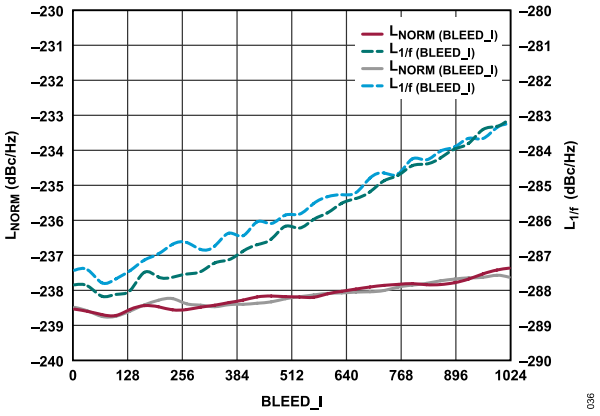

Figure 36. L_{NORM} and $L_{1/f}$ vs. BLEED_I

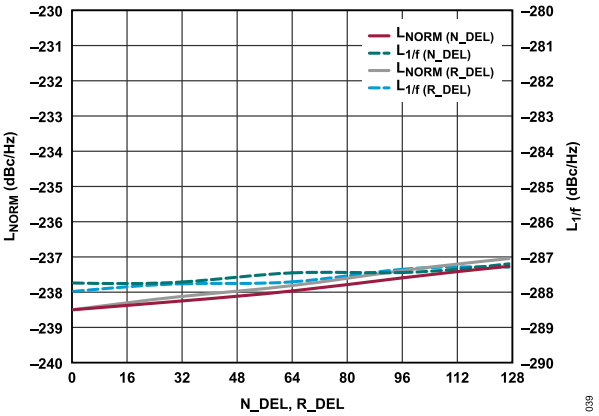

Figure 39. L_{NORM} and $L_{1/f}$ vs. N_DEL, R_DEL

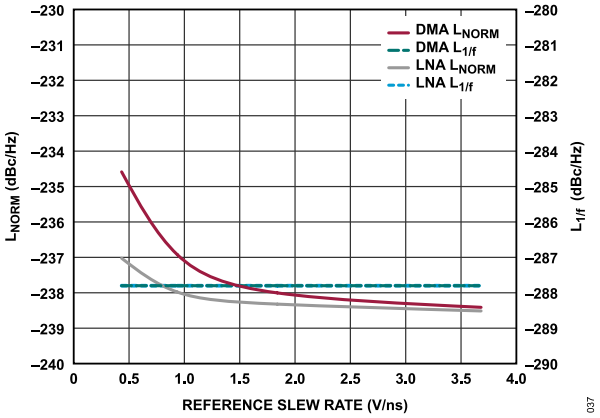

Figure 37. L_{NORM} and $L_{1/f}$ vs. Reference Slew Rate, Reference Amplifier

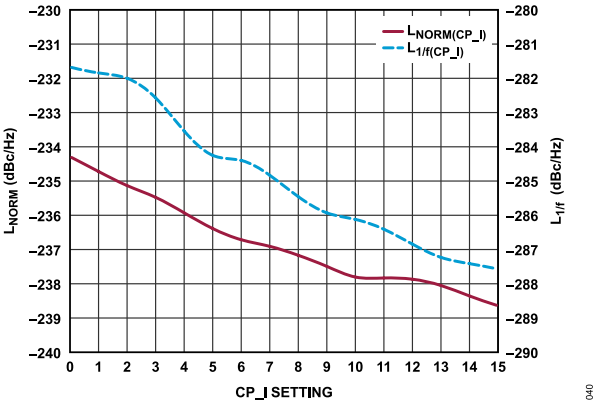

Figure 40. L_{NORM} and $L_{1/f}$ vs. CP_I Setting

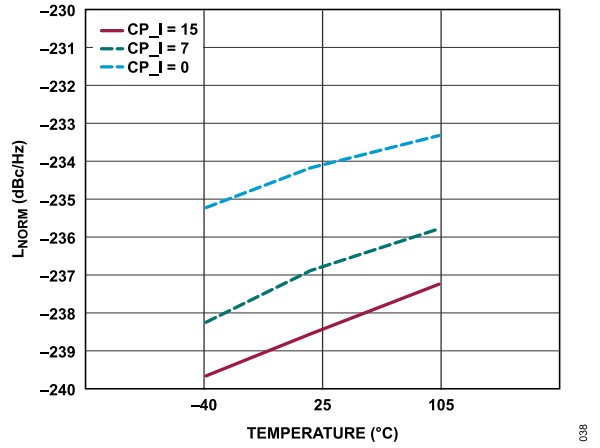

Figure 38. L_{NORM} vs. Temperature, Charge Pump Current

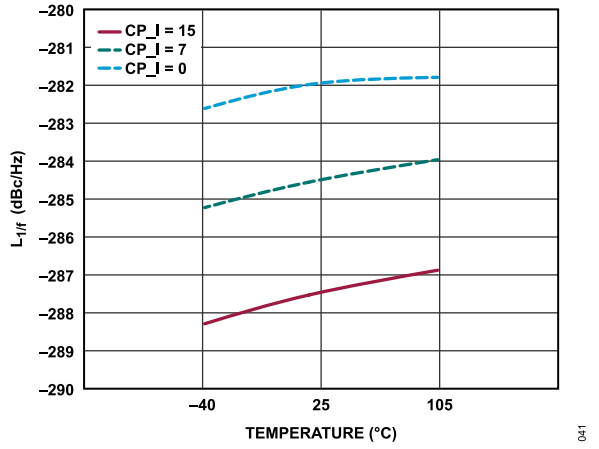

Figure 41. $L_{1/f}$ vs. Temperature, Charge Pump Current

TYPICAL PERFORMANCE CHARACTERISTICS

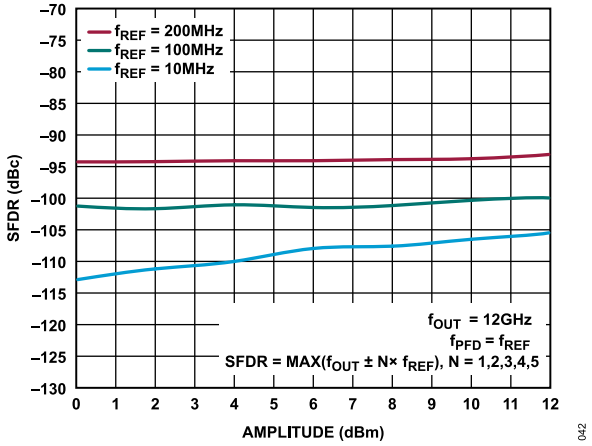

Figure 42. Reference and PFD Spurious Level at Various Reference Frequencies and Reference Amplitudes, EN_RDBLR = 0

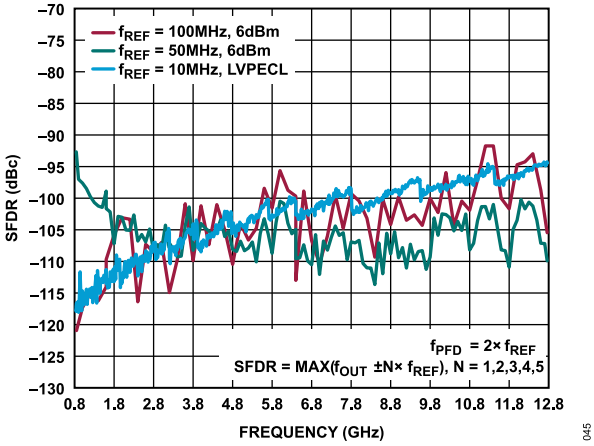

Figure 45. Reference and PFD Spurious Level at Various Reference Frequencies and Output Frequencies, EN_RDBLR = 1

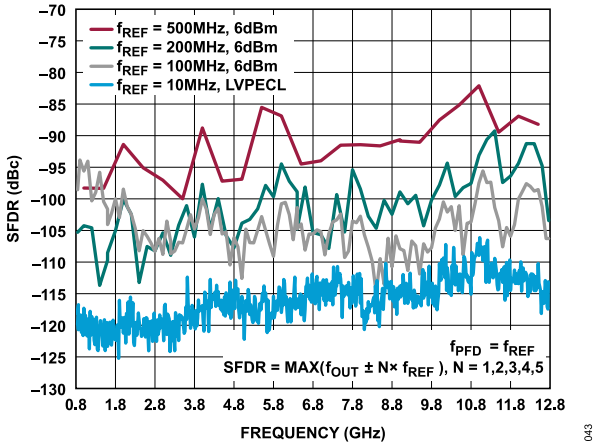

Figure 43. Reference and PFD Spurious Level at Various Reference Frequencies and Output Frequencies, EN_RDBLR = 0

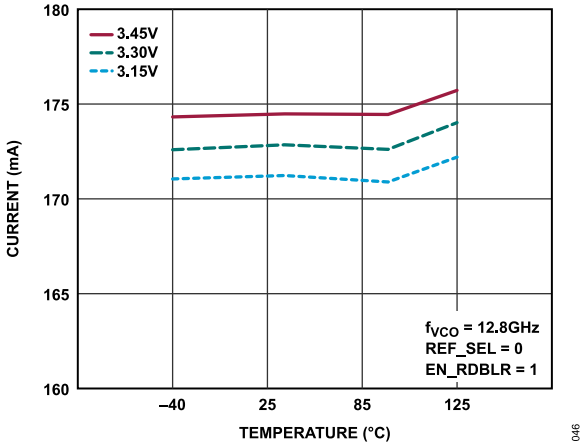

Figure 46. 3.3 V Supply Group 1 Current at Various Junction Temperatures and Power Supply Voltages

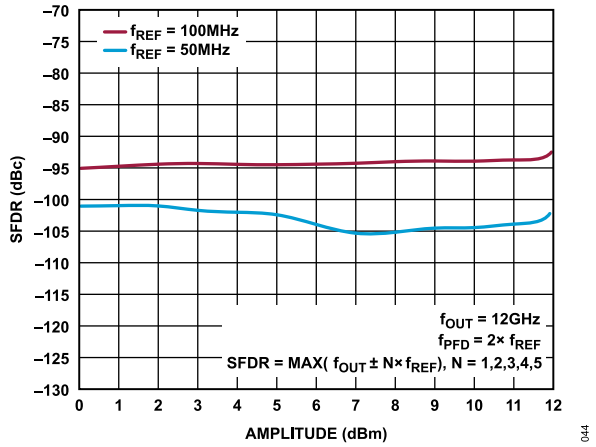

Figure 44. Reference and PFD Spurious Level at Various Reference Frequencies and Reference Amplitudes, EN_RDBLR = 1

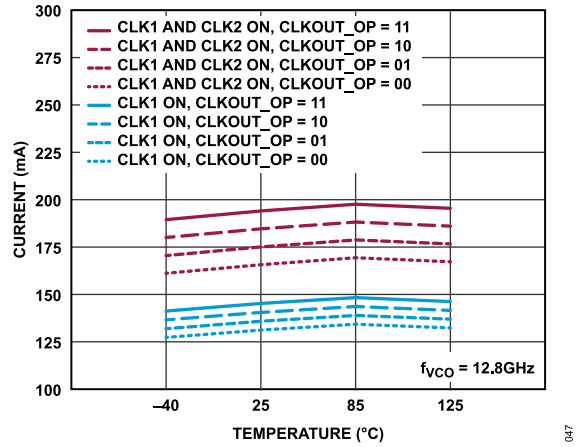

Figure 47. 3.3 V Supply Group 2 Current at Various Junction Temperatures and Output Settings

TYPICAL PERFORMANCE CHARACTERISTICS

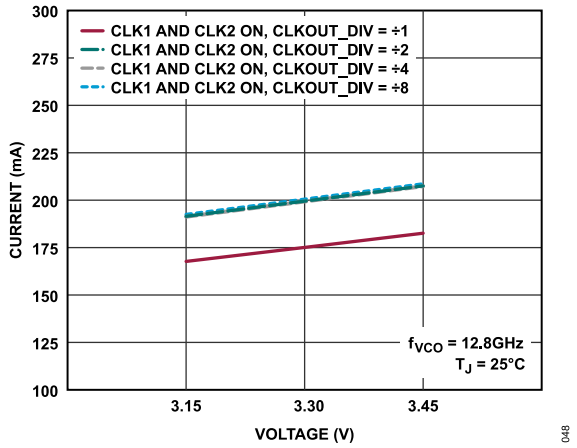

Figure 48. 3.3 V Supply Group 2 Current at Various Power Supply Voltages and CLKOUT_DIV Settings

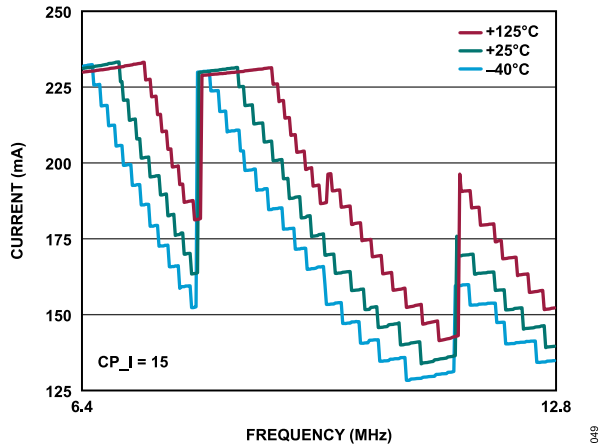

Figure 49. 5 V Supply Current at Various Output Frequencies and Junction Temperatures

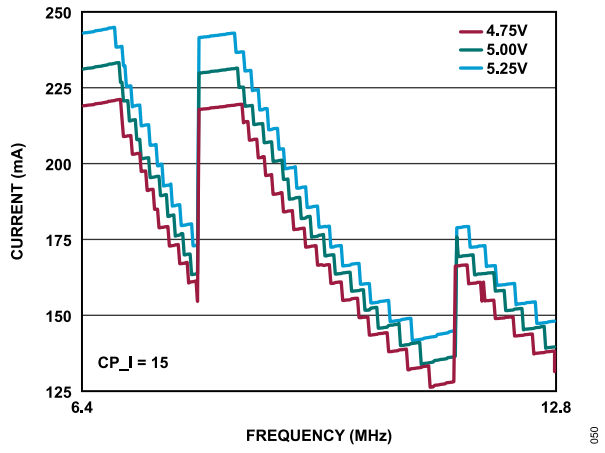

Figure 50. 5 V Supply Current at Various Output Frequencies and Power Supply Voltages

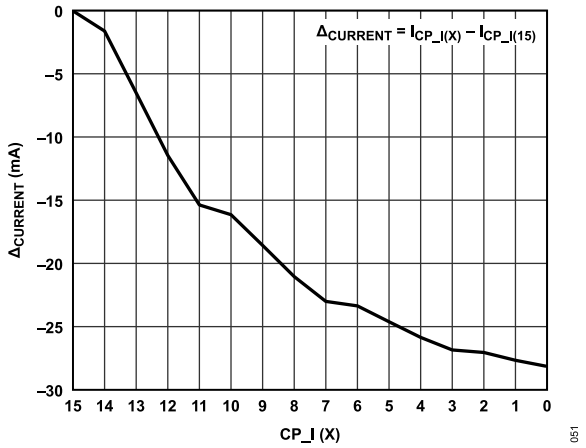

Figure 51. 5 V Delta Supply Current ($\Delta_{CURRENT}$) at Various CP_I Settings

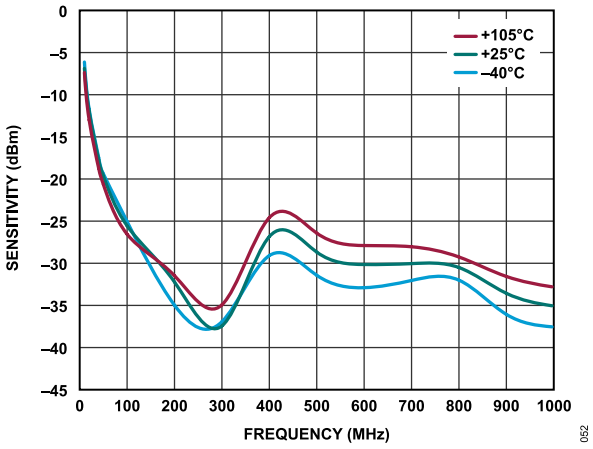

Figure 52. DMA Reference Input Sensitivity at Various Reference Frequencies and Temperatures

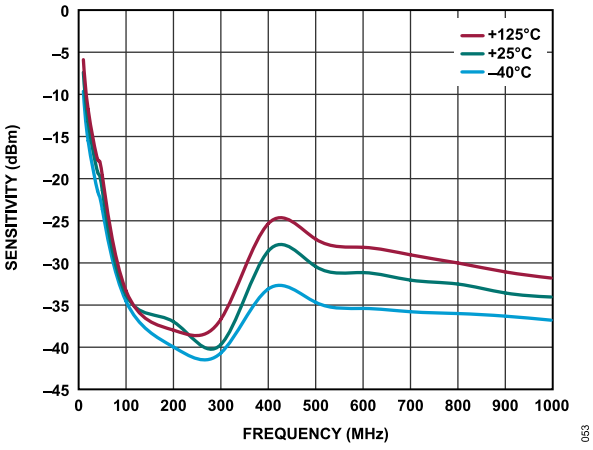

Figure 53. LNA Reference Input Sensitivity at Various Reference Frequencies and Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

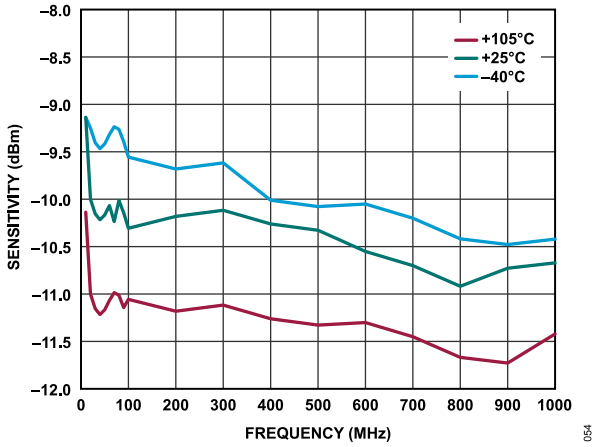

Figure 54. Reference Input Signal Detected at Various Reference Frequencies and Temperatures

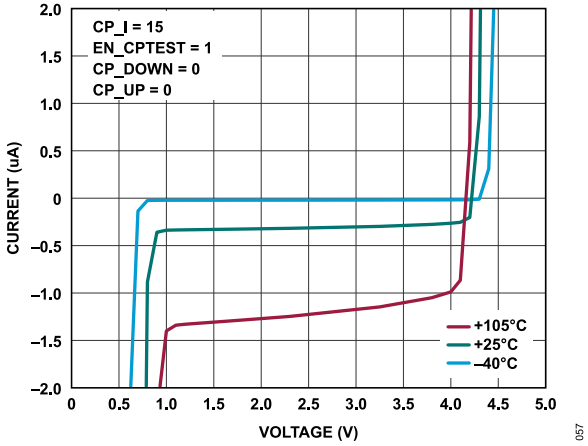

Figure 57. Charge Pump High-Z Current at Various Charge Pump Voltages and Temperatures

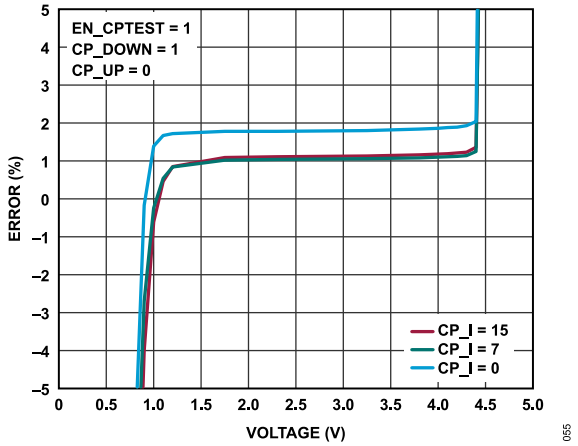

Figure 55. Charge Pump Sink Current Error at Various Charge Pump Voltages and CP_I Settings

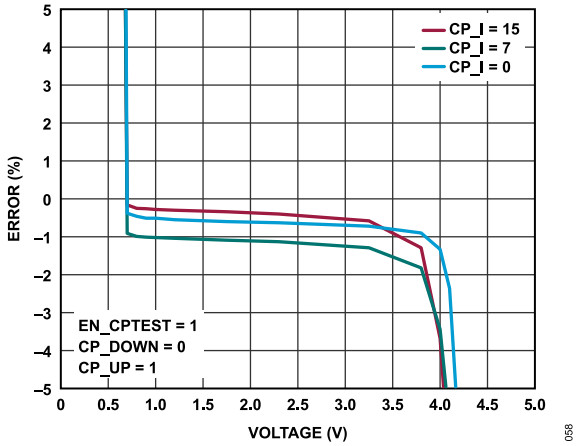

Figure 58. Charge Pump Source Current Error at Various Charge Pump Voltages and CP_I Settings

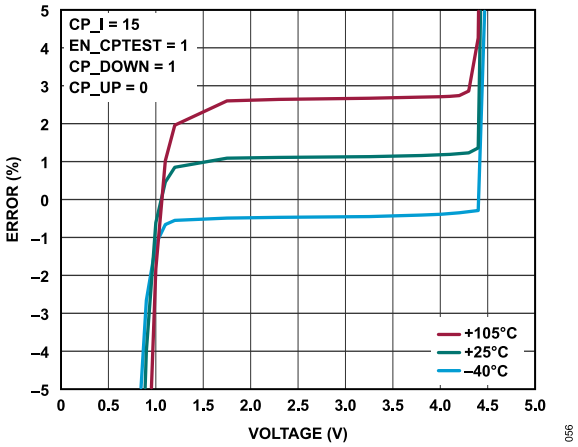

Figure 56. Charge Pump Sink Current Error at Various Charge Pump Voltages and Temperatures

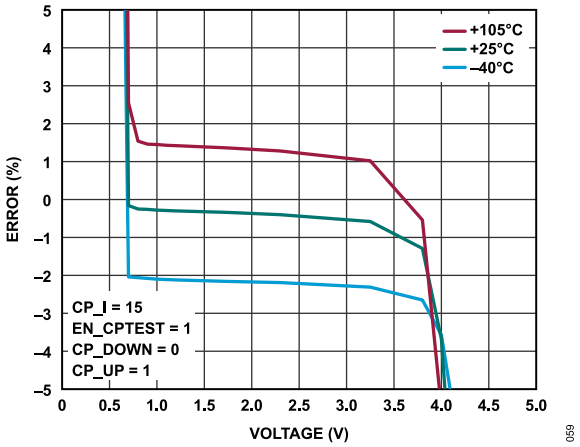

Figure 59. Charge Pump Source Current Error at Various Charge Pump Voltages and Temperatures

THEORY OF OPERATION

INTRODUCTION

A PLL is a complex feedback system that may conceptually be considered a frequency multiplier. The system multiplies the reference input frequency (f_{REF}) and produces a higher frequency on the clock output pins (f_{OUT}). The PFD, charge pump, output divider, feedback divider, VCO, and external loop filter forms a feedback loop to accurately control the output frequency (see Figure 60). The reference divider or reference doubler is used to set the frequency resolution.

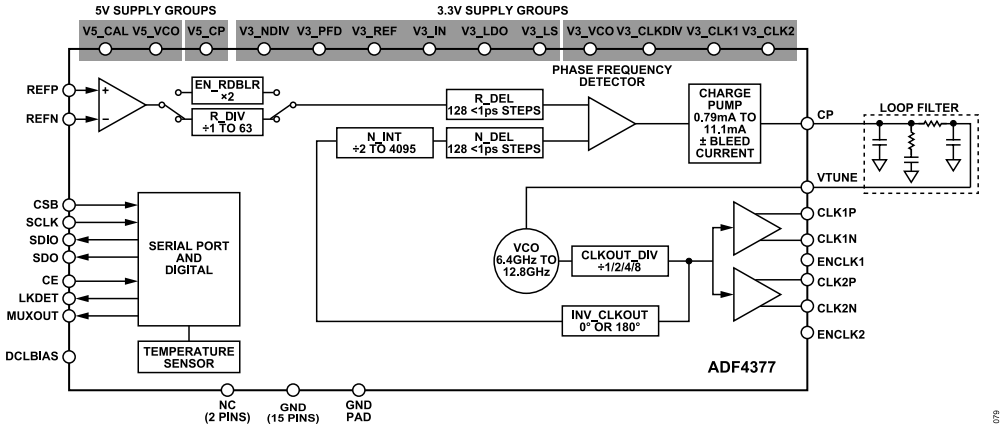

Figure 60. PLL Loop Diagram

THEORY OF OPERATION

OUTPUT FREQUENCY

When EN_RDBLR = 0

When the loop is locked, the frequency (f_{VCO}) (in Hz) produced at the output of the VCO is determined by the reference frequency (f_{REF}) and the O, R, and N values given by Equation 1. Refer to Table 11 and Table 18 for more information.

$$f_{VCO} = f_{REF} \times \frac{N \times O}{R} \quad (1)$$

In the following equation, the PFD frequency (f_{PFD}) produced is given by Equation 2.

$$f_{PFD} = \frac{f_{REF}}{R} \quad (2)$$

f_{VCO} may be alternatively expressed as

$$f_{VCO} = f_{PFD} \times N \times O \quad (3)$$

The output frequency (f_{OUT}) produced at the output of the output divider is given by Equation 4.

$$f_{OUT} = \frac{f_{VCO}}{O} \quad (4)$$

The output frequency resolution (f_{STEP}) produced by a unit change in N is given by Equation 5.

$$f_{STEP} = f_{PFD} \quad (5)$$

When EN_RDBLR = 1

When the loop is locked, the frequency (f_{VCO}) (in Hz) produced at the output of the VCO is determined by the reference frequency (f_{REF}) and the O, D, and N values given by Equation 6.

$$f_{VCO} = f_{REF} \times D \times N \times O \quad (6)$$

When EN_RDBLR = 1, the PFD frequency (f_{PFD}) produced is given by Equation 7.

$$f_{PFD} = f_{REF} \times D \quad (7)$$

Equation 3, Equation 4, and Equation 5 for f_{VCO}, f_{OUT}, and f_{STEP} remain the same when EN_RDBLR = 1.

CIRCUIT DESCRIPTION

Reference Input Buffer

The reference frequency of the PLL is applied differentially on the REFP pin and REFN pin. These high impedance inputs are self-biased and must be ac-coupled with 1 µF capacitors (see Figure 61 for a simplified schematic). Alternatively, the differential inputs may be configured as a single ended input by applying the reference frequency at REFP and bypassing REFN to GND with a 1 µF capacitor (see Figure 80).

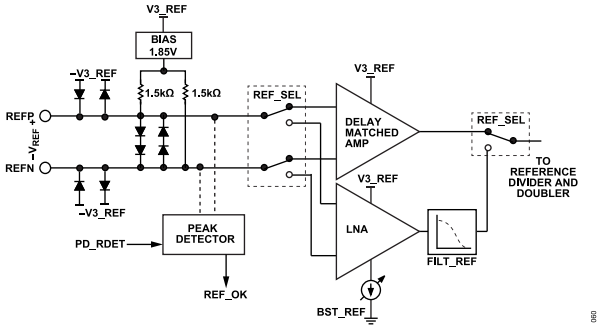

Figure 61. Reference Input Stage

A high quality signal must be applied to the REFP and REFN inputs because they provide the frequency reference to the entire PLL. To achieve the in-band phase noise performance of the PLL, apply a continuous waveform signal or a square wave with a slew rate of at least 1000 V/µs. See the Reference Source Considerations section for more information on reference input signal requirements and interfacing.

When the REF_SEL bit is set to 0, the DMA buffer is selected. The DMA is optimized for high slew rate signals, such as square waves or higher frequency and higher amplitude sine waves. The DMA has a controlled propagation delay from the reference input to clock output, which eases time zero and over temperature multichip clock alignment.

When the REF_SEL bit is set to 1, the LNA is selected. The LNA is optimized for low slew rate signals, such as lower frequency or lower amplitude sine waves.

The REF_SEL bit must be set correctly to optimize the in-band phase noise performance and propagation delay. See Table 7, Figure 37, and Equation 8 for recommended settings.

Table 7. REF_SEL Programming

REF_SEL	Sine Wave Slew Rate (V/µs)	Square Wave	Optimized t_{PD}
0	≥1500	Preferred	Yes
1	<1500	Not applicable	Not applicable

To calculate the slew rate of sine wave,

$$Slew\ \ Rate\ \ = 2 \times \pi \times f \times V \quad (8)$$

where:

f = sine wave frequency

V = sine wave amplitude (in V_{PK})

The FILT_REF bit controls the low-pass filter of the reference input LNA and must be set for sine wave signals based on f_{REF} to limit the wideband noise of the input reference signal. The FILT_REF bit must be set correctly to reach the L_{NORM} normalized in-band phase noise floor. See Table 8 for recommended settings. Square wave inputs must have FILT_REF set to 0.

THEORY OF OPERATION

Table 8. FILT_REF Programming

FILT_REF	Sine Wave f_{REF}	Square Wave f_{REF}
0	≥20 MHz	All f_{REF}
1	< 20 MHz	Not applicable

The BST_REF bit must be set based on the input signal level to prevent the LNA reference input buffer from saturating. The BST_REF programming is the same whether the input is a sine wave or a square wave. See Table 9 for recommended settings and the Applications Information section for programming examples.

Table 9. BST_REF Programming

BST_REF	Sine Wave V_{REF}
0	≥ 1.6 V p-p
1	< 1.6 V p-p

Reference Peak Detector

A reference input peak detection circuit is provided on the REFP and REFN inputs to detect the presence of a reference signal and provides the REF_OK status flag available through serial port register REG0049. The circuit has hysteresis to prevent the REF_OK flag from chattering at the detection threshold.

The peak detector approximates an rms detector. Therefore, sine and square wave inputs give different detection thresholds by a factor of 4/π. See Table 10 for REF_OK detection values.

Table 10. REF_OK Status Output vs. Reference Input

REF_OK	Sine Wave V_{REF}	Square Wave V_{REF}
1	≥200 mV p-p	≥155 mV p-p
0	<160 mV p-p	<125 mV p-p

Reference Divider (R) and Doubler (D)

When the EN_RDBLR bit is set to 1, a frequency multiplier is used to double the frequency seen at the PFD. When the EN_RDBLR bit is set to 0, a 6-bit divider, R_DIV, is used to reduce the frequency seen at the PFD. The reference divide ratio, R, may be set to any integer from 1 to 63, inclusive of all the integer divide values. Use the R_DIV bits found in REG0012 to directly program the R divide ratio (see Figure 62 and Table 11). See the Output Frequency section for the relationship between R, D, and the f_{REF}, f_{PFD}, f_{VCO}, and f_{OUT} frequencies. The state of the DCLK_MODE bit is determined by Table 17.

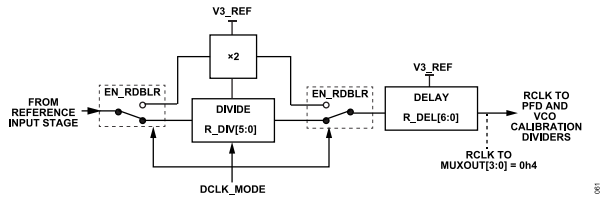

Figure 62. Reference Divider and Doubler

Table 11. EN_RDBLR and R_DIV Programming

EN_RDBLR	R_DIV	R	D
1	Not applicable	Not applicable	2
0	0	1	Not applicable
0	1	1	Not applicable
0	…	…	Not applicable
0	63	63	Not applicable

Reference Delay

A 7-bit delay, R_DEL, is used to increase the propagation delay from the reference input pins to the clock outputs pins. Use the R_DEL bits to directly program the reference delay (t_{RDEL}) which typically ranges from 0 ps to 127 ps in 1 ps steps (see Figure 63).

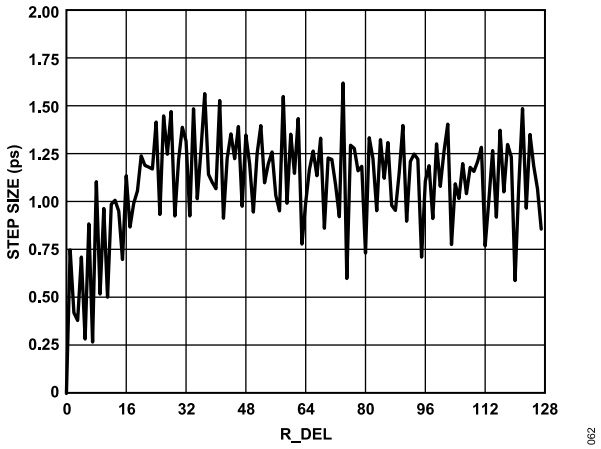

Figure 63. Typical Reference Delay Step Size vs. R_DEL Register Setting

INV_CLKOUT, N_DEL, and R_DEL can be used in conjunction to align the multichip output to output skew to within ±0.5 ps. Figure 39 shows that the largest R_DEL settings may increase L_{NORM} by 1 dB. INV_CLKOUT does not degrade performance and must be used to adjust for multichip output to output skews greater than a quarter of the $1/f_{OUT}$ period, in lieu of a large N_DEL or R_DEL value. As a result, the maximum t_{RDEL} adjustment never has to be more than a quarter of the $1/f_{OUT}$ period. See the Aligning Multiple ADF4377 Output Phases section for the relationship between R_DEL, N_DEL, INV_CLKOUT, BLEED_I bit fields, Bits[9:0], and BLEED_POL.

Phase/Frequency Detector (PFD)

The PFD, in conjunction with the charge pump, produces source and sink current pulses proportional to the phase difference between the outputs of the reference divider or reference doubler and feedback divider. This action provides the necessary feedback to phase-lock the loop, forcing a phase alignment at the inputs of the PFD. See Figure 64 for a simplified schematic of the PFD.

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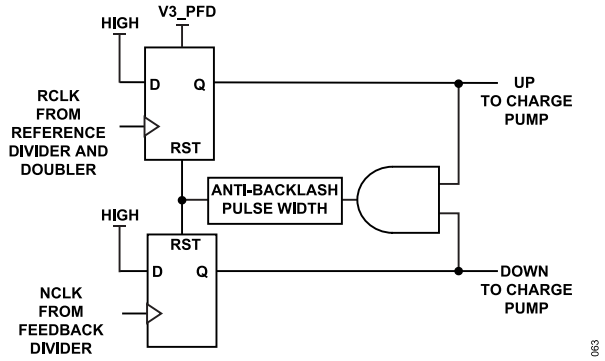

Figure 64. Simplified PFD Schematic

Charge Pump

The charge pump, controlled by the PFD, forces sink (down) or source (up) current pulses onto the CP pin, which must be connected to an appropriate loop filter. See Figure 65 for a simplified schematic of the charge pump.

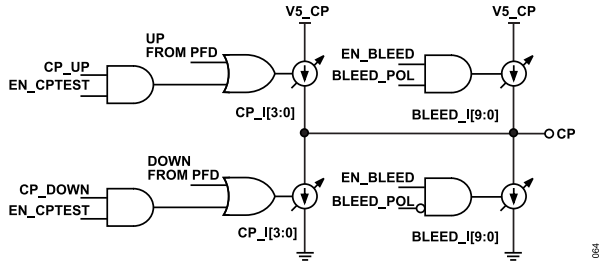

Figure 65. Simplified Charge Pump Schematic

The output current magnitude (I_{CP}) may be set from 0.79 mA to 11.1 mA using the CP_I bits. A larger I_{CP} can result in lower in-band noise (L_{NORM}) due to the lower impedance of the loop filter components. A smaller I_{CP} can result in better spurious performance. See Table 12 for programming specifics and the Applications Information section for information on designing a loop filter.

Table 12. CP Programming

CP_I	I_{CP}
0	0.79 mA
1	0.99 mA
2	1.19 mA
3	1.38 mA
4	1.59 mA
5	1.98 mA
6	2.39 mA
7	2.79 mA
8	3.18 mA
9	3.97 mA
10	4.77 mA
11	5.57 mA
12	6.33 mA
13	7.91 mA

Table 12. CP Programming

CP_I	I_{CP}
14	9.51 mA
15	11.1 mA

Charge Pump Test Mode

When the EN_CPTEST bit is set to 1, the CP_UP bit and CP_DOWN bit can be programmed to force a constant I_{CP} source or sink current, respectively, on the CP pin. These bits are commonly used as an aid to debug PLL related issues during the hardware and software development phase of a project. For normal operation, set EN_CPTEST, CP_UP, and CP_DOWN to 0. Refer to Figure 65 and Table 13.

Table 13. Charge Pump Debug Functions

EN_CPTEST	CP_UP	CP_DOWN	CP Pin State	Debug Test
1	0	0	High-Z	VCO open loop
1	1	0	~V_{V5_CP}	Charge pump output voltage verification
1	0	1	~GND	
0	0	0	Normal operation	Not applicable

Charge Pump Bleed Current

A small programmable constant charge pump current, known as bleed current, can be used to either increase or decrease the propagation delay from the reference input pins to the clock output pins.

To enable the bleed current, set the EN_BLEED bit to 1. When the BLEED_POL bit is set to 1, a small constant source current is forced onto the CP pin. When the BLEED_POL bit is set to 0, a small constant sink current is forced onto the CP pin. Refer to Figure 65.

The bleed current LSB step size is 536 nA. The bleed current delay step size ($t_{IDEL-STEP}$) is a function of the bleed current step size (I_{CP}) and f_{PFD}, as shown in Equation 9. Figure 66 provides a quick reference of $t_{IDEL-STEP}$ vs. several common I_{CP} and f_{PFD} values.

$$t_{IDEL-STEP} = \frac{536\ nA}{I_{CP} \times f_{PFD}} \quad (9)$$

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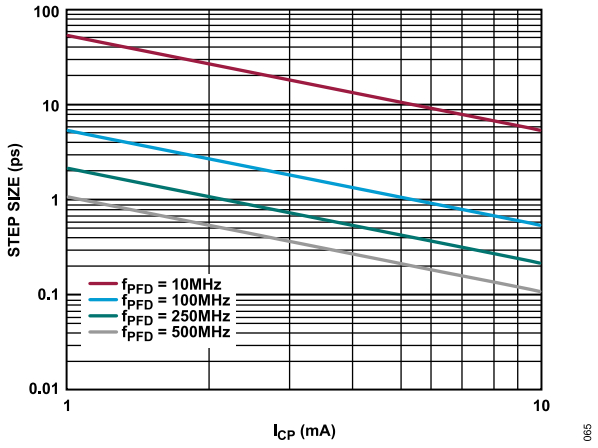

Figure 66. Bleed Current Delay Step Size

Bleed current delay (t_{IDEL}) is determined by $t_{IDEL-STEP}$, the BLEED_POL bit, and BLEED_I bit fields, Bits[9:0]. Refer to Equation 10 and Equation 11.

If BLEED_POL = 0, the propagation delay from the REFP and REFN input pins to the CLKxP and CLKxN output pins increases. Refer to Figure 19.

$$t_{IDEL} = t_{IDEL-STEP} \times BLD\_I \quad (10)$$

where BLD_I represents the decimal value of the BLEED_I bit field, Bits[9:0].

If BLEED_POL = 1, the propagation delay from the REFP and REFN input pins to the CLKxP and CLKxN output pins decreases. Refer to Figure 22

$$t_{IDEL} = -t_{IDEL-STEP} \times BLD\_I \quad (11)$$

The maximum t_{IDEL} for proper lock detector functionality is based on the LDWIN_PW setting, as shown in Table 16.

INV_CLKOUT, BLEED_I bit fields, Bits[9:0], and BLEED_POL can be used in conjunction to align the multichip output to output skew to as small as ±0.05 ps (see Equation 9). The largest BLEED_I bit fields, Bits[9:0] settings may increase L_{NORM} by 1 dB and $L_{1/f}$ by 4 dB, as shown in Figure 36. INV_CLKOUT does not degrade performance and must be used to adjust for multichip output to output skews greater than a quarter of the $1/f_{OUT}$ period, in lieu of a large BLEED_I bit fields, Bits[9:0] value. As a result, the maximum t_{IDEL} adjustment never needs to be more than a quarter of the $1/f_{OUT}$ period. See the Applications Information section for the relationship between R_DEL, N_DEL, INV_CLKOUT, BLEED_I bit fields, Bits[9:0], and BLEED_POL.

Lock Detector

The lock detector uses internal signals from the PFD to measure phase coincidence between the output signal of the reference divider and doubler (RCLK) in Figure 62 and the output signal of the feedback divider (NCLK) in Figure 72. It is enabled by setting both the EN_LOL bit and the EN_LDWIN bit to 1 and presents the lock detector output on the LKDET pin and the LOCKED bit. The lock detector output can also be presented on the MUXOUT pin by programming the MUXOUT bits (see Figure 75). The CMOS_OV bit determines if the logic high level for the MUXOUT, LKDET, SDO, and SDIO output pins is 3.3 V or 1.8 V.

The PFD phase difference must be less than the phase difference lock window time (t_{LDWIN}) for a set number of PFD cycles before the lock detector output indicates that the PLL has locked. The desired number of PFD cycles varies if a designer prioritizes lock detect accuracy or speed. Five loop filter time constants can be used as an initial estimate of the desired number of PFD cycles, as shown in Equation 12. The desired number of PFD cycles is set by the LD_COUNT bits, as shown in Table 14. Refer to Figure 67 and Table 15 for more details.

$$PFD\ \ Cycles = \frac{5 \times f_{PFD}}{2 \times \pi \times \mathrm{LPBW}} \quad (12)$$

where LPBW = loop filter bandwidth.

Table 14. LD_COUNT Programming

LD_COUNT	PFD Cycles
0	23
1	32
2	47
3	66
4	95
5	134
6	191
7	270
8	383
9	542
10	767
11	1085
12	1535
13	2171
14	3071
15	4343
16	6143
17	8687
18	12287
19	17376
20	24575
21	34754
22	49151
23	69510
24	98303
25	139021
26	196607
27	278044
28	393215
29	556090

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Table 14. LD_COUNT Programming

LD_COUNT	PFD Cycles
30	786431
31	1112181

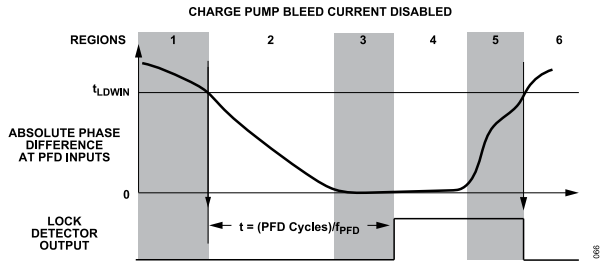

Figure 67. Lock Detector Timing, Bleed Current Disabled

Table 15. Lock Detector Timing, Bleed Current Disabled

Region	Absolute Phase Difference at PFD	Lock Detector State
1	> t_{LDWIN}	Low
2	< t_{LDWIN}	Low, counts PFD cycles
3	~0	
4	~0	High, ≥ desired PFD cycle count
5	< t_{LDWIN}	High
6	> t_{LDWIN}	Low (immediately)

When the charge pump bleed current is enabled, a phase offset is applied to the PFD inputs. This phase offset (t_{IDEL}) is proportional to the amount of bleed current programmed in Equation 10 and Equation 11. Region 3 and Region 4 in Figure 67 and Figure 68 highlight the PFD phase difference that the PLL settles to when the charge pump bleed current is disabled or enabled, respectively.

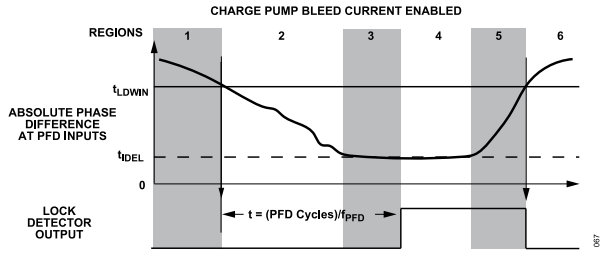

Figure 68. Lock Detector Timing, Bleed Current Enabled

For proper operation of the lock detector, the absolute value of t_{IDEL} must be less than t_{LDWIN}. The user sets the phase difference lock window time (t_{LDWIN}) for a valid lock condition with the LDWIN_PW bit. In most cases, LDWIN_PW must be set to 0. Refer to Table 16 to understand the relationship between the LDWIN_PW bit and maximum allowable t_{IDEL}.

Table 16. Maximum t_{IDEL}

LDWIN_PW	$t_{IDEL(MAX)}$
0	±150 ps
1	±250 ps

VCO

The VCO core consists of 4 separate VCOs, each of which uses 256 overlapping bands, which allows the device to cover a wide frequency range without large VCO sensitivity (K_{VCO}). The output frequency can be further extended by utilizing the output divider.

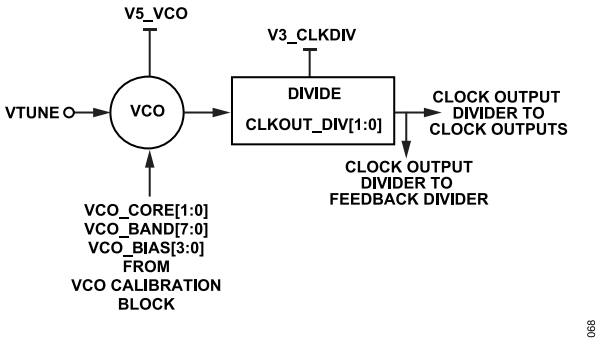

Figure 69. VCO and Clock Output Divider

The correct register values for the VCO_CORE, VCO_BAND, and VCO_BIAS settings are determined by performing a VCO calibration. See the VCO Calibration section for more information. After a VCO calibration is performed for a specific device and frequency, the VCO_CORE, VCO_BAND, and VCO_BIAS values can be recorded. These recorded values may be programmed manually on subsequent power ups when the same device and frequency are used, thereby avoiding the VCO calibration time.

VCO Calibration

A VCO calibration is required to select the correct VCO core, band, and bias settings for a specific VCO frequency. This procedure assumes that the device is powered up, the desired reference frequency is present on the REFP and REFN pins, and all other registers are programmed correctly. Figure 70 and Figure 71 are provided as visual aids for this procedure.

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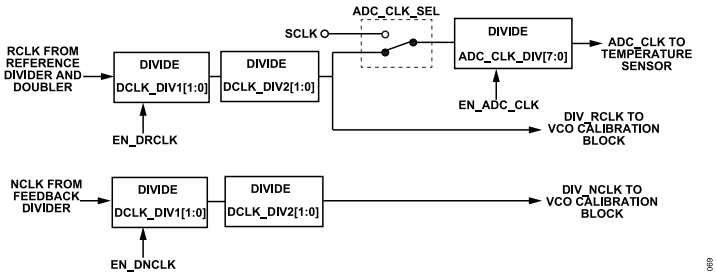

Figure 70. VCO Calibration Dividers

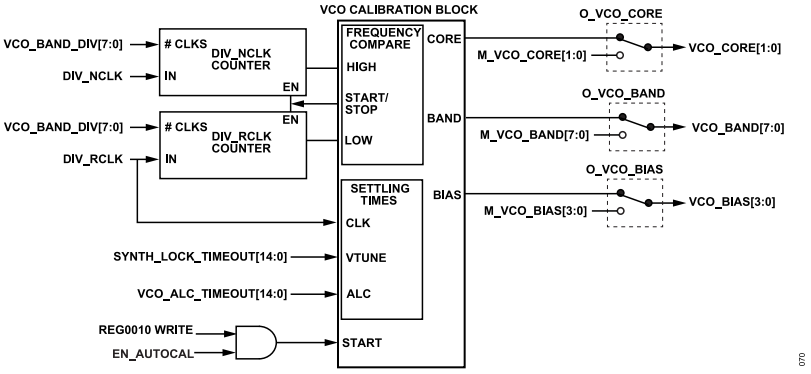

Figure 71. VCO Calibration Block

To perform a VCO calibration, set up several registers as outlined in the following procedure:

1. Set register bits based on the RCLK column in Table 22.
2. Set DCLK_DIV1 = 1. Set CAL_CT_SEL, DCLK_DIV2, and DCLK_MODE to the values in Table 17. Record f_{DIV_RCLK} for later use.
3. Calculate and set the minimum values for the SYNTH_LOCK_TIMEOUT bit fields, Bits[14:0], the VCO_ALC_TIMEOUT bit fields, Bits[14:0], and the VCO_BAND_DIV bits. Typical automatic VCO calibration times are 3 ms to 9 ms when minimum values are chosen for these parameters. Larger values produce longer VCO calibration times.

$$SYNTH\_LOCK\_TIMEOUT \geq Ceiling(200\ \mu s \times f_{DIV\_RCLK}) \quad (13)$$

$$VCO\_ALC\_TIMEOUT \geq Ceiling(50\ \mu s \times f_{DIV\_RCLK}) \quad (14)$$

$$VCO\_BAND\_DIV \geq Ceiling\left(\frac{15\ \mu s \times f_{DIV\_RCLK}}{16 \times 2^{DCLK\_MODE}}\right) \quad (15)$$

4. Ensure that the ADC_CLK_DIV bits are set so that the desired ADC clock frequency is <400 kHz.

$$ADC\_CLK\_DIV > Ceiling\left(\frac{\left(\frac{f_{DIV\_RCLK}}{400\ kHz} - 2\right)}{4}\right) \quad (16)$$

5. Set the N_INT bit fields, Bits[11:0], CLKOUT_DIV bits, R_DIV bits, and EN_RDBLR bits by programming REG0010 last. Any write to REG0010 starts the VCO automatic calibration.
6. This is an optional step. Monitor the register bits, ADC_BUSY and FSM_BUSY. The calibration is finished when ADC_BUSY transitions from high to low, followed by FSM_BUSY transitioning from high to low.
7. After the VCO calibration is complete, disable calibration clocks to limit unwanted spurious content by setting EN_DRCLK = EN_DNCLK = EN_ADC_CLK = 0.
8. This is an optional step. Read back the VCO_CORE, VCO_BAND, and VCO_BIAS bits, and then record the readback values. These values can be used to bypass calibration and manually program the M_VCO_CORE, M_VCO_BAND, and M_VCO_BIAS bits for a given device and frequency, as described in the Fast Power-Up and Initialization, Manually Programmed VCO Calibration Settings (Optional) section.

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Table 17. CAL_CT_SEL, DCLK_DIV2, and DCLK_MODE Setup

f_{PFD} (MHz)	CAL_CT_SEL	DCLK_DIV2	DCLK_MODE	f_{DIV_RCLK} (MHz)
≤160	1	0	0	$f_{PFD}/2$
>160 and ≤250	1	0	1	$f_{PFD}/2$
>250 and ≤320	0	1	0	$f_{PFD}/4$
>320 and ≤500	0	1	1	$f_{PFD}/4$

Clock Output Divider

A 2-bit divider, CLKOUT_DIV, in Figure 69 is used to reduce the frequency seen at the output buffer and feedback divider. The clock output divide value (O) may be set to 1, 2, 4, or 8. Use the CLKOUT_DIV bit to directly program the divide ratio. CLKOUT_DIV is located inside the PLL loop. Therefore, any change to CLKOUT_DIV requires a change to the N_INT bit fields, Bits[11:0] to maintain the same f_{PFD} and results in the PLL losing lock for a few loop time constants. Refer to Table 18 for more information. See the Theory of Operation section for the relationship between the f_{REF}, f_{PFD}, f_{VCO}, and f_{OUT} frequencies.

Table 18. CLKOUT_DIV Programming

CLKOUT_DIV	O	Output Frequency Range (GHz)
0	1	$6.4 \geq f_{OUT} \leq 12.8$
1	2	$3.2 \geq f_{OUT} \leq 6.4$
2	4	$1.6 \geq f_{OUT} \leq 3.2$
3	8	$0.8 \geq f_{OUT} \leq 1.6$

Output Invert (INV_CLKOUT)

The output invert (INV_CLKOUT) is used to shift the output signal 180° with respect to the rising edge of the reference input signal, when f_{OUT} is an integer multiple of f_{REF}. Refer to Table 19 for more information. INV_CLKOUT is located inside the PLL loop, and any change to INV_CLKOUT results in the PLL losing lock for few a loop time constants. Use the INV_CLKOUT bit to directly program the output phase.

Table 19. INV_CLKOUT Programming

f_{OUT}/f_{REF}=	INV_CLKOUT	Each Reference Rising Edge Aligned to
Integer	0	CLKP rising edge
Integer	1	CLKP falling edge
Noninteger	x	Varies

INV_CLKOUT, N_DEL, R_DEL, BLEED_I bit fields, Bits[9:0], and BLEED_POL can be used in conjunction to align the multichip output to output skew to sub ps levels. INV_CLKOUT does not degrade performance and must be used to adjust for multichip output-output skews greater than a quarter of the $1/f_{OUT}$ period, in lieu of a large N_DEL, R_DEL, or BLEED_I bit fields, Bits[9:0] value. See the Aligning Multiple ADF4377 Output Phases section for the relationship between R_DEL, N_DEL, INV_CLKOUT, BLEED_I bit fields, Bits[9:0], and BLEED_POL.

Feedback Divider (N)

A 12-bit divider, the N_INT bit fields, Bits[11:0], in Figure 72, is used to reduce the frequency seen at the output of the clock output divider. The feedback divider closes the feedback loop from the VCO and clock output divider to the PFD.

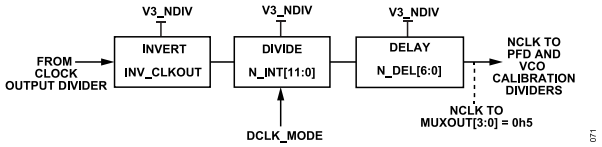

Figure 72. Feedback Divider

The feedback divider divide ratio (N) may be programmed to any integer from 2 to 4095. Use the N_INT bit fields, Bits[11:0] to directly program the N divide ratio (see Table 20). See the Output Frequency section for the relationship between N, O, and the f_{REF}, f_{PFD}, f_{VCO}, and f_{OUT} frequencies. The state of the DCLK_MODE bit is determined by Table 17.

Table 20. N_INT Programming

N_INT Bit Fields, Bits[11:0]	N
0	Not applicable
1	Not applicable
2	2
3	3
…	…
4095	4095

Feedback Delay

A 7-bit delay, N_DEL, is used to decrease the propagation delay from the REFP and REFN input pins to the CLKxP and CLKxN output pins. Use the N_DEL bits to directly program the feedback delay (t_{NDEL}), which typically ranges from 0 ps to 110 ps in 0.85 ps steps (see Figure 73).

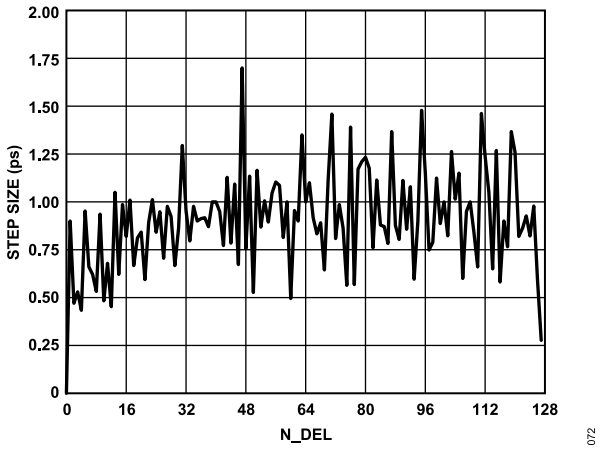

Figure 73. Step Size vs. N_DEL , Typical Feedback Delay

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INV_CLKOUT, N_DEL, and R_DEL can be used in conjunction to align the multichip output to output skew to within ±0.5 ps. Figure 39 shows that the largest N_DEL settings may increase L_{NORM} by 1 dB. INV_CLKOUT does not degrade performance and can be used to adjust for multichip output to output skews greater than a quarter of the $1/f_{OUT}$ period, in lieu of a large N_DEL or R_DEL value. As a result, the maximum t_{NDEL} adjustment never has to be more than a quarter of the $1/f_{OUT}$ period. See the Aligning Multiple ADF4377 Output Phases section for the relationship between R_DEL, N_DEL, INV_CLKOUT, BLEED_I bit fields, Bits[9:0], and BLEED_POL.

Clock Output Buffer

The low noise, differential output buffer in Figure 74 produces a differential output voltage. The output amplitude level and common mode voltage is settable with the CLKOUT1_OP bits and CLKOUT2_OP bits, according to Table 21. Each output can be either ac-coupled or dc-coupled and terminated with 100 Ω, differentially. If a single-ended output is desired, each side of the output must be individually ac-coupled and terminated with 50 Ω (see Figure 98).

Table 21. CLKOUT1_OP, CLKOUT2_OP Programming

CLKOUT1_OP, CLKOUT2_OP	Differential Amplitude (V_{OD})	Common-Mode Voltage
0	320 mV_{PEAK}	$V_{CLK} - 1.2 \times V_{OD}$
1	420 mV_{PEAK}	$V_{CLK} - 1.2 \times V_{OD}$
2	530 mV_{PEAK}	$V_{CLK} - 1.2 \times V_{OD}$
3	640 mV_{PEAK}	$V_{CLK} - 1.2 \times V_{OD}$

The outputs can be powered down individually by either setting the ENCLK1 pin and ENCLK2 pin low or programming the PD_CLKOUT1 and PD_CLKOUT2 bits to 1. The EN_CLK1 bit and EN_CLK2 bit report the state of the ENCLK1 pin and ENCLK2 pin. When powered down, the outputs source a common-mode voltage around 2 V.

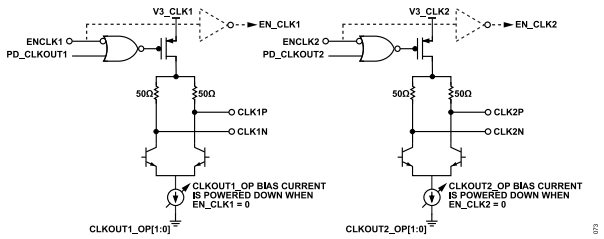

Figure 74. Simplified Clock Outputs

MUXOUT

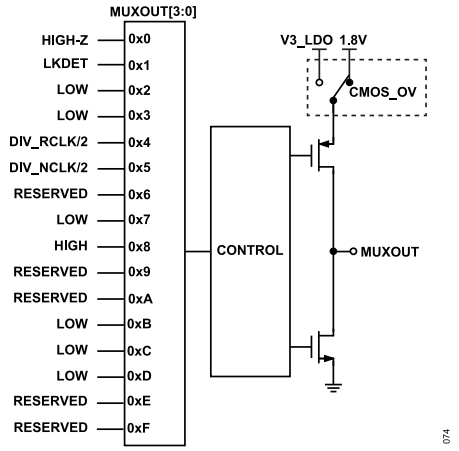

Figure 75. MUXOUT

The state of the MUXOUT pin is determined by the serial port interface (SPI) register bit field MUXOUT, which allows the user access to various internal nodes. The MUXOUT pin and MUXOUT bits are commonly used as an additional lock status output or to debug PLL related issues during the hardware and software development phase of a project. The CMOS_OV bit field determines if the logic high level for the MUXOUT pin, LKDET pin, SDO pin, and SDIO pin is 3.3 V or 1.8 V.

Temperature Sensor

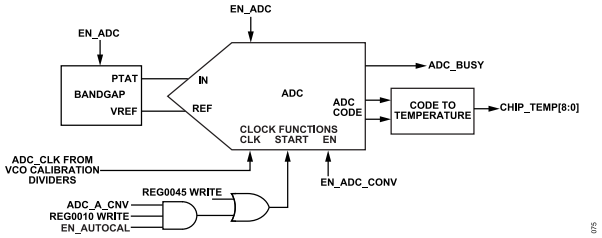

Figure 76. Temperature Sensor

The temperature sensor is composed of an 8-bit ADC, which measures the proportional to absolute temperature (PTAT) voltage with respect to the reference (VREF) voltage of a bandgap. The purpose of the temperature sensor is to measure changes in die temperature, not the absolute junction temperature.

The maximum ADC clock frequency is 400 kHz. Equation 16 calculates the correct ADC_CLK_DIV value. The ADC clock may be generated from either the SPI clock or the RCLK (see Figure 70). Before an ADC measurement can occur, program the registers of the ADF4377 as shown in Table 22.

Table 22. ADC Register Setup for SPI Clock and RCLK

Bits	RCLK[1]	SPI Clock
ADC_CLK_SEL	0	1
EN_DRCLK, EN_DNCLK	1	Not applicable

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Table 22. ADC Register Setup for SPI Clock and RCLK

Bits	RCLK[1]	SPI Clock
ADC_A_CONV, EN_AUTOCAL	1[1]	Not applicable
EN_ADC_CNV, EN_ADC, EN_ADC_CLK	1	
PD_ADC	0	

[1] Required when writing to REG0010 to start the ADC conversion and VCO calibration.

After the bits in Table 22 are programmed, start an ADC conversion with either, a register write to REG0045 or a register write to REG0010 (RCLK only). With a REG0010 write, a VCO calibration (see the VCO Calibration section) begins immediately after the ADC conversion is complete. An ADC conversion requires 17 clock cycles to complete. In serial port register REG0049, the ADC_BUSY bit monitors the conversion status. During a conversion, ADC_BUSY is set to 1 and on conversion completion, ADC_BUSY is set to 0.

Measurements are recorded in the CHIP_TEMP bit fields, Bits[8:0], in REG004C and REG004D (see Figure 76).

If an ambient temperature measurement is desired, program the ADF4377 to a low power state, as shown in Table 23. For ambient temperature measurements, the SPI clock is the only available clock option.

Table 23. Ambient Temperature Full Power Down Register Setup

Bit Fields	State
ADC_CLK_SEL	1
PD_ADC	0
PD_CLK, PD_RDET, PD_CALDAC, PD_NDIV, PD_VCO, PD_LD, PD_PFDCP, PD_CLKOUT1, PD_CLKOUT2, PD_RDIV	1

Double Buffering

Double buffering refers to a main/subordinate configuration for the bit fields shown in Table 24. Only the subordinate bit fields control the actual state of the ADF4377. When double buffering is enabled for a bit field, the serial interface only writes to the main bit field. The subordinate bit field retains its previous value until a register write is sent to REG0010. After writing to REG0010, all main bit fields are automatically loaded to their respective subordinate bit field. Writing to REG0010 also starts the autocalibration of the VCO (see the VCO Calibration section). This allows the user to update several bit fields that change the output frequency of the ADF4377 and start a new VCO calibration on the same register write. When double buffering is disabled, the serial interface writes directly to the subordinate bit field.

It is possible to read back the state of either the main or subordinate bit fields by enabling or disabling the MAIN_READBACK_CONTROL bit.

Table 24. Double Buffer Enable Bits and Bit Fields

Double Buffer Enable Bits	Double Buffered Bit Fields
Not applicable, always enabled	N_INT bits, Bits[11:0], R_DIV, EN_RDBLR, CP_I
CLKODIV_DB	CLKOUT_DIV
DCLK_DIV_DB	DCLK_DIV1, DCLK_DIV2
O_VCO_DB	M_VCO_CORE, M_VCO_BAND, M_VCO_BIAS
DEL_CTRL_DB	INV_CLKOUT, BLEED_I bits, Bits[9:0], BLEED_POL, N_DEL, R_DEL

Serial Port

The SPI-compatible serial port provides control and monitoring functionality. The CMOS_OV bit determines if the logic high level for the SDO and SDIO SPI output pins is 3.3 V or 1.8 V. CMOS_OV also sets the output level for MUXOUT and LKDET.

The serial port can be programmed to support several different configurations in REG0000 and REG0001.

The SDO_ACTIVE bit determines if the serial port is configured as a 3-wire or 4-wire serial interface (see the timing diagrams in Figure 2, Figure 3, and Figure 4).

As shown in Figure 77 and Figure 78, the instruction cycle is composed of 16 bits. The fifteen LSB bits determine the register address, and the MSB determines if data is written to or read from the serial interface during the data transfer cycle. The LSB_FIRST bit determines the data orientation of the instruction cycle and data transfer cycle of the serial interface.

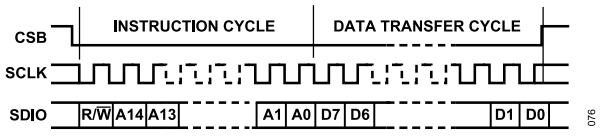

Figure 77. Serial Interface, MSB First (LSB_FIRST = 0)

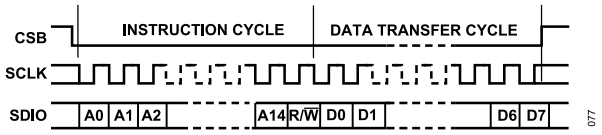

Figure 78. Serial Interface, LSB First (LSB_FIRST = 1)

The SPI register map can be programmed with single instructions, as shown in Figure 77 and Figure 78, or in streaming mode, as shown in Figure 79. Streaming mode allows for efficient data transfer read or write cycles to multiple registers. Streaming mode allows the user to program a bit stream composed of one register address in the instruction header and data for that register address, which is then followed by data in subsequent register addresses. The ADDRESS_ASCENSION bit determines if the subsequent register addresses are incremented or decremented. It is recommended to decrement the register addresses in streaming mode (ADDRESS_ASCENSION = 0). The reason for this recommendation is

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because REG0010 triggers the VCO calibration and loading of all double buffers and, therefore, must be the last SPI register written to. The SINGLE_INSTRUCTION bit disables streaming mode when it is set to 1. When SINGLE_INSTRUCTION is set to 0, streaming mode is enabled.

Block Power Down Control

The power down control bits of the ADF4377 reside in REG0019 and REG001A. The PD_ALL, PD_RDET, PD_CLKOUT1, and PD_CLKOUT2 bits may be programmed independently.

The PD_CLK, PD_CALDAC, PD_RDIV, PD_NDIV, PD_VCO, PD_LD, and PD_PFDCP bits must be set to the same state at all times. The only time this group is allowed to be set to 1 is when a full power-down ambient temperature measurement is performed (see Table 23). In all other cases, this bit grouping must be set to 0.

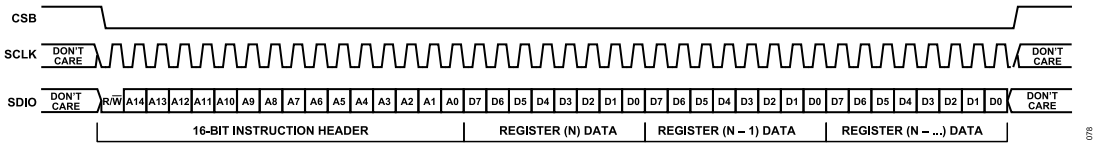

Figure 79. Serial Interface, Recommended Streaming Mode (SINGLE_INSTRUCTION = 0) with Decrementing Registers (ADDRESS_ASCENCION = 0)

APPLICATIONS INFORMATION

LOOP FILTER DESIGN

A stable loop filter design requires care in selecting the loop filter components of the ADF4377. It is recommended to download and install ADIsimPLL™ for loop filter design and simulation. ADIsimPLL has an integrated tutorial for first time users and a help manual for more complex topics. There are also several ADIsimPLL training videos available on www.analog.com. After a loop filter has been designed and simulated, it is recommended to verify the new loop filter using the ADF4377 evaluation hardware.

A full loop filter design tutorial is beyond the scope of this data sheet. However, some best practices are shown in the following lists. ADIsimPLL aids in defining and simulating these parameters. Any significant change to these items requires a new loop filter design.

A stable loop filter must meet the following criteria:

- Loop filter phase margin > 45°
- Loop filter bandwidth < $f_{PFD} \div 10$

The desired loop filter bandwidth is determined by the following features of the ADF4377:

- I_{CP}
- K_{VCO}
- PFD frequency
- Reference input phase noise (see the Reference Phase Noise section).
- Trade-off between minimizing jitter or settling time (see the Output Phase Noise Characteristics section and Equation 12, respectively).

The VTUNE pin has an internal 30 pf capacitor to GND that must be included in the loop filter design. ADIsimPLL takes this internal capacitance into account automatically.

REFERENCE SOURCE CONSIDERATIONS

Reference Input Network

The reference input buffer of the ADF4377, shown in Figure 61, provides a flexible interface to either differential or single-ended frequency sources. Figure 80 to Figure 85 show recommended interfaces for different reference signal types. All Z_O signal traces are 50 Ω transmission lines in Figure 80, Figure 81, Figure 82, Figure 83, Figure 84, and Figure 85.

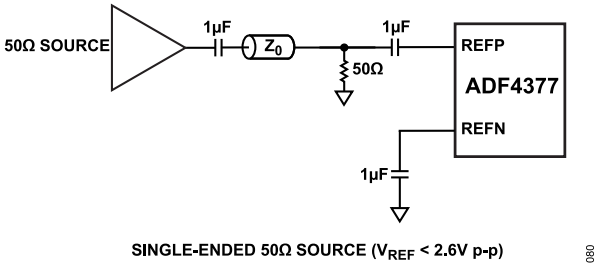

Figure 80. Single-Ended 50 Ω Source (V_{REF} < 2.6 V p-p)

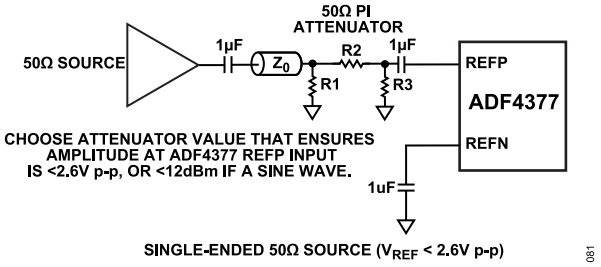

Figure 81. Single-Ended 50 Ω Source (V_{REF} > 2.6 V p-p)

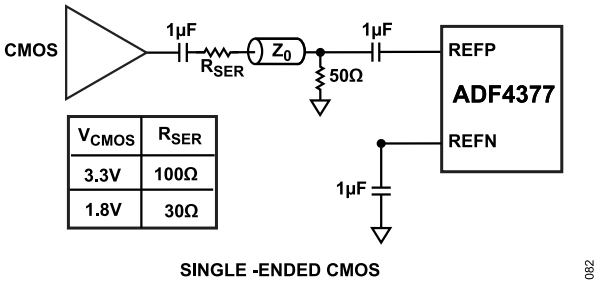

Figure 82. Single-Ended CMOS

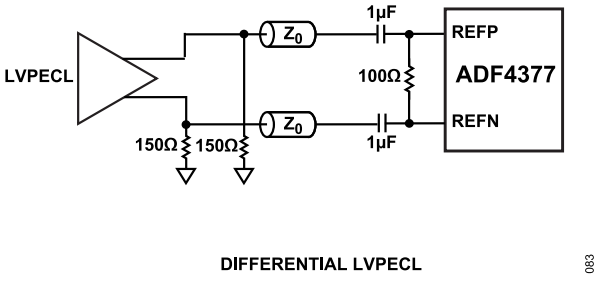

Figure 83. Differential LVPECL

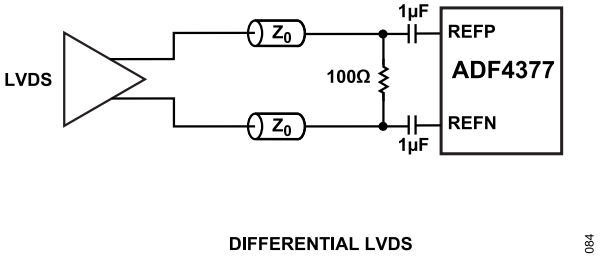

Figure 84. Differential LVDS

APPLICATIONS INFORMATION

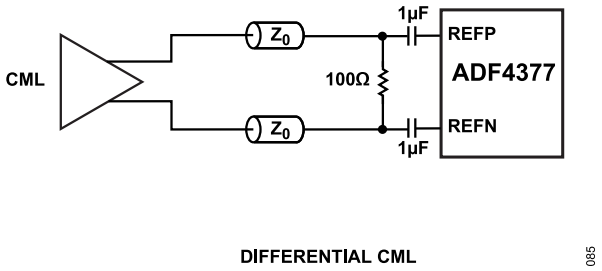

Figure 85. Differential CML

Reference Phase Noise

The ADF4377 achieves an in-band normalized phase noise floor of L_{NORM} = −239 dBc/Hz typical. To calculate the equivalent input phase noise floor (L_{IN}), use the following Equation 17. Equation 17 is plotted in Figure 86.

$$L_{IN} = L_{NORM} + 10 \times \log_{10}(f_{REF}) \quad (17)$$

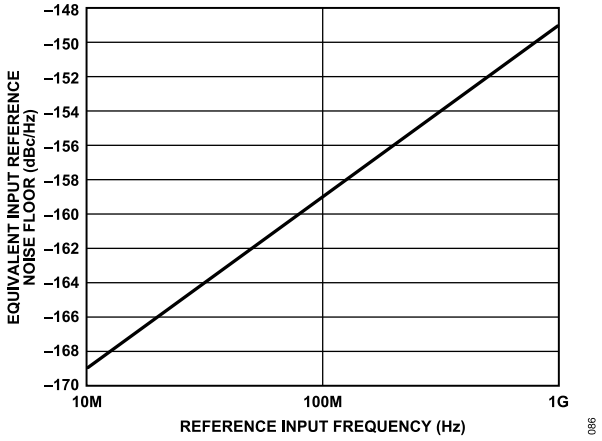

Figure 86. Equivalent Input Reference Noise Floor vs. Reference Input Frequency

For example, a 100 MHz reference input frequency gives an L_{IN} of −159 dBc/Hz. The phase noise of the reference frequency source must be at least 6 dB less than L_{IN} to avoid impacting and increasing the overall system phase noise.

To maintain typical L_{NORM} performance, Table 7 provides criteria for selecting the optimal REF_SEL setting based on the input reference signal type and amplitude.

OUTPUT PHASE NOISE CHARACTERISTICS

In-Band Output Phase Noise

The in-band phase noise floor (L_{OUT}) produced at f_{OUT} may be calculated by Equation 18 and Equation 19.

$$L_{OUT} = L_{NORM} + 10 \times \log_{10}(f_{PFD}) + 20 \times \log_{10}\left(\frac{f_{OUT}}{f_{PFD}}\right) \quad (18)$$

or

$$L_{OUT} = L_{NORM} + 10 \times \log_{10}(f_{PFD}) + 20 \times \log_{10}\left(\frac{N}{O}\right) \quad (19)$$

where L_{NORM} = −239 dBc/Hz. See Figure 36 to Figure 41, which show L_{NORM} variation vs. I_{CP}, N_DEL, R_DEL, BLEED_I bit fields, Bits[9:0], and reference slew rate.

As shown from Equation 18 and Equation 19 for a given PFD frequency (f_{PFD}), the output in-band phase noise increases at a 20 dB per decade rate with the N divider count. Therefore, for a given output frequency (f_{OUT}), f_{PFD} must be as large as possible (or N must be as small as possible) while still satisfying the frequency step size requirements of the application.

Output Phase Noise Due to 1/f Noise

In-band phase noise at very low offset frequencies may be influenced by the 1/f noise of the ADF4377, depending on f_{PFD}. Use the normalized in-band 1/f noise ($L_{1/f}$) of −287 dBc/Hz with Equation 20 to approximate the output 1/f phase noise at a given frequency offset (f_{OFFSET}).

$$L_{OUT(1/f)} = L_{1/f} + 20 \times \log_{10}(f_{OUT}) - 10 \times \log_{10}(f_{OFFSET}) \quad (20)$$

Often $L_{1/f}$ is normalized to a 1 GHz signal at a 10 kHz offset, as shown in Equation 21.

$$L_{1/f\_1G\_10k} = L_{1/f} + 20 \times \log_{10}(1 \quad GHz) - 10 \times \log_{10}(10 \quad kHz) = L_{1/f} + 140 \quad dB \quad (21)$$

Unlike the in-band noise floor (L_{OUT}), the 1/f noise ($L_{OUT(1/f)}$) does not change with f_{PFD} and is not constant over offset frequency. See Figure 87 for an example of in-band phase noise for f_{PFD} equal to 100 MHz and 500 MHz. The total phase noise is the summation of L_{OUT} and $L_{OUT(1/f)}$, calculated by Equation 22.

$$L_{OUT(TOTAL)}(f_{OFFSET}) = 10 \times \log_{10}\left(10^{L_{OUT}/10} + 10^{L_{OUT(1/f)}(f_{OFFSET})/10}\right) \quad (22)$$

APPLICATIONS INFORMATION

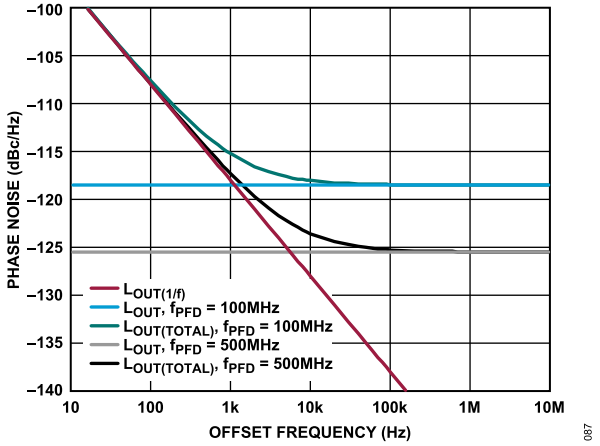

Figure 87. Theoretical In-Band Phase Noise, f_{OUT} = 10 GHz

POWER-UP AND INITIALIZATION SEQUENCE

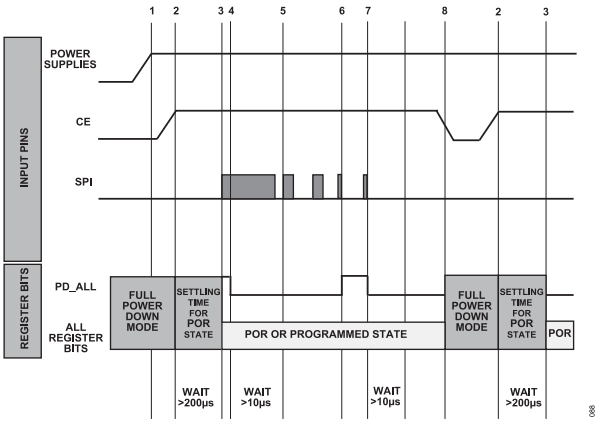

Figure 88. Power-Up and Initialization Sequence

The following steps describe the recommended power-up and initialization sequence of the ADF4377:

1. Apply specified voltages to the V_{5V}, $V_{3.3V\_1}$, and $V_{3.3V\_2}$ power supply groups. The ADF4377 is in full power-down mode at this point and SPI programming is not possible.
2. Set the CE pin to a logic high. It is acceptable to connect the CE pin to the V3_LDO pin via a pull-up resistor, therefore performing Step 1 and Step 2 coincidentally.
3. After waiting ≥200 µs for all SPI register bits to settle to their power-on reset state (POR), begin programming the SPI to configure the ADF4377 to a desired state. The following is the recommended SPI programming:
    a. Set the SDO_ACTIVE and CMOS_OV bits to a desired state for future readback operations.
    b. Program all register addresses in descending order, REG0045 to REG0010. There are several required reserved register field settings provided in Table 42 that are required for proper device operation.
4. The ADF4377 remains in power-down mode until the PD_ALL bit is programmed to 0. After PD_ALL is disabled, wait at least 10 µs for the VCO calibration circuitry and other circuit blocks to settle before starting a VCO calibration.
5. A write to REG0010 starts a VCO autocalibration. At this point, the device is fully operational and new frequencies can be programmed as often as desired.
6. Setting PD_ALL to 1 powers down the ADF4377, retaining the latest programmed SPI settings and full SPI programming capability.
7. If only the state of PD_ALL was modified in Step 6, setting PD_ALL to 0 returns the ADF4377 to the frequency programmed in Step 5. After a 10 µs wait, all circuit blocks are completely powered up internally. This 10 µs wait does not include the frequency settling time associated with the loop filter bandwidth.
8. Toggling the CE pin level causes the ADF4377 to return to full power-down mode and return the SPI registers to the POR state (see Step 2 and Step 3).

POWER SUPPLY AND BYPASSING

The ADF4377 is a high performance, low noise device. Phase noise and spurious performance may be degraded by noisy power supplies. To achieve maximum performance and ensure that power supply noise does not degrade the performance of the ADF4377, it is recommended to use the Analog Devices low noise, high power supply rejection ratio (PSRR) regulators. Preferred regulators include the LT3045, ADM7150, and the ADM7151.

The ADF4377 eliminates the need for on-board supply bypass capacitors, by integrating all necessary local power supply bypass capacitors on the ADF4377 package laminate. As shown in Figure 89, by removing the requirement for local power supply bypass capacitors, the ADF4377 consumes 40% less effective PCB area and reduces the number of board layout design challenges.

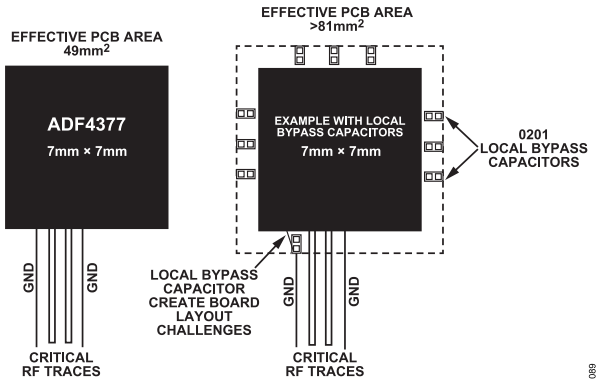

Figure 89. Layout Advantages with Integrated Power Supply Decoupling Capacitors

APPLICATIONS INFORMATION

DESIGN AND PROGRAMMING EXAMPLE 1: SINGLE ADF4377

A single ADF4377 clocks a single ADC. The purpose of this example is to provide a method to determine the correct inputs required to design a loop filter in ADIsimPLL, provide a method to manually generate all ADF4377 register settings, and provide the method to perform a VCO autocalibration on initial power-up and bypass or override the VCO autocalibration on all future device power-ups. In practice, the ADF4377 evaluation board graphical user interface (GUI) register automates the register generation process and can replace and/or verify the manual register generation method.

For this design example, assume the following design goals:

- Reference input, 125 MHz, single-ended 7 dBm sine wave, 50 Ω environment
- Output of 12 GHz
- SPI requirements of 1.8 V, 4 wire SPI, optimize SPI write sequence
- Prioritize designing for the lowest jitter performance over other design criteria

Design Procedure

The following design procedure aids in schematic design and SPI register generation:

1. Select the settings for reference and loop filter design (see the Reference and Loop Filter Design section)
2. Select the output, frequency, and amplitude (see the Output Selection, Frequency and Amplitude section)
3. Select the settings for the reference to output propagation delay (see the Reference to Output Propagation Delay Settings section)
4. Select the lock detector settings (see the Lock Detector Settings section)
5. Select the VCO automatic calibration settings (see the VCO Automatic Calibration Settings section)
6. Select the double buffer and manual VCO calibration settings (see the Double Buffer and Manual VCO Calibration Settings section)
7. Select the SPI protocol settings (see the SPI Protocol Settings section)
8. Select the remaining register settings (see the Remaining Register Settings section)

Reference and Loop Filter Design

To design a loop filter in ADIsimPLL, the user must determine the desired reference input settings, charge pump settings, and PFD frequency. The design goals provided in the Design and Programming Example 1: Single ADF4377 section state to prioritize the lowest jitter performance over other design criteria. To design the lowest jitter loop filter, determine the register settings that minimize the output phase noise characteristics as described in the Output Phase Noise Characteristics section.

The In-Band Output Phase Noise section states the maximum f_{PFD} minimizes L_{OUT}. The maximum f_{PFD} is obtained with the reference doubler enabled and the reference divider bypassed (see the Reference Divider (R) and Doubler (D) section). To enable the reference doubler, set EN_RDBLR = 1. The reference divider is bypassed and can remain at its power on reset state (R_DIV = 1). Solve Equation 7 for the maximum f_{PFD}.

$$f_{PFD} = D \times f_{REF} = 2 \times 125 \quad MHz = 250 \quad MHz$$

The Charge Pump section states that larger I_{CP} results in lower L_{NORM}, as shown in Figure 40. Set CP_I = 15 to minimize L_{NORM}.

Selecting the optimal reference input buffer amplifier (see the Reference Input Buffer section) based on the reference input slew rate also minimizes L_{NORM} (see Figure 37). Solve Equation 23 and Equation 8 for the reference input slew rate.

$$V_{PK} = \sqrt{2} \times \sqrt{10^{((P_{dBm}/10) \times 50\ \Omega/1000\ mW)}} \tag{23}$$

$$V_{PK} = \sqrt{2} \times \sqrt{10^{((7\ dBm/10) \times 50\ \Omega/1000\ mW)}} = 0.707$$
$$V_{PK}$$

$$Slew \quad Rate \quad = 2 \times \pi \times f_{REF} \times V_{PK} = 2 \times \pi \times 125$$
$$\text{MHz} \times 0.707 = 556 \quad \text{V}/\upsilon\text{s}$$

Based on Table 7 and Figure 37, a reference input slew rate of 556 V/µs minimizes L_{NORM} when the LNA reference amplifier is selected by setting REF_SEL = 1. When the LNA reference amplifier is selected, Table 8 requires FILT_REF = 0 when f_{REF} = 125 MHz, and Table 9 requires BST_REF = 1 when V_{REF} = 2 × 0.707 V_{PK} = 1.414 V p-p.

The reference peak detector (see the Reference Peak Detector section) consumes minimal power, ~10 mW, and does not degrade performance. As a result, PD_RDET can be set to 0 or 1 to meet the design goals. The reference and loop filter design was created with PD_RDET = 0 to allow for the option to monitor the reference signal with the REF_OK bit.

Table 25. SPI Summary, Reference and Loop Filter Design

Bit Field	Value
EN_RDBLR	0x1
R_DIV	0x1
CP_I	0xF
REF_SEL	0x1
FILT_REF	0x0
BST_REF	0x1
PD_RDET	0x0

For the recommended reference input network, refer to Figure 80, single-ended 50 Ω source (V_{REFIN} < 2.6 V p-p).

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For ADIsimPLL loop filter design, note that the selected LNA reference amplifier has a higher gain than the DMA reference amplifier. As a result, the LNA generates larger reference spurious content, which requires a 5th order loop filter design to achieve the stated typical spurious performance of −100 dBc. However, the DMA has less reference spurious content and can use a simpler 4th order loop filter design for the same spurious result. For the purposes of the reference and loop filter design, assume ADIsimPLL created a loop filter with a 460 kHz loop bandwidth. The loop filter bandwidth is used to determine the LD_COUNT setting in the Lock Detector Settings section.

Output Selection, Frequency and Amplitude

The Design and Programming Example 1: Single ADF4377 section design goals require f_{OUT} = 12 GHz. Table 18 sets CLKOUT_DIV = 0 and O = 1 when f_{OUT} = 12 GHz. The PLL feedback divider bit fields, N_INT, Bits[11:0], can be determined from Equation 4, Equation 6, and Table 20.

$$f_{OUT} = f_{VCO}/O = f_{VCO}$$
$$f_{VCO} = f_{REF} \times D \times N \times O, \text{ solving for } N \text{ produces}$$
$$N = f_{VCO}/(f_{REF} \times D \times O) = 12\,GHz/(125\,MHz \times 2 \times 1)$$
$$= 48, N\_INT \text{ setting}$$

The clock output buffer amplitude (see the Clock Output Buffer section) does not have a noticeable effect on jitter performance, see Figure 9. However, Figure 47 indicates that lower amplitudes decrease the supply current. Therefore, choose the lowest amplitude setting the ADC clock input accepts. For the frequency and amplitude output selection, choose the CLK1P and CLK1N clock output buffer amplitude by setting CLKOUT1_OP = 1 (see Figure 30 and Table 21).

Enable the output of CLK1P and CLK1N by setting the ENCLK1 pin to logic high and setting PD_CLKOUT1 = 0. Because this example clocks a single ADC, the output of CLK2P and CLK2N is powered down. Power down CLK2P and CLK2N either by setting the ENCLK2 pin to a logic low and/or setting the PD_CLKOUT2 bit = 1. Because CLK2P and CLK2N is powered down, the CLKOUT2_OP amplitude setting can remain at its power on reset state of 0.

Common ADF4377 clock output networks are shown in Figure 98.

Table 26. SPI Summary, Output Selection, Frequency and Amplitude

Bit Field	Value
CLKOUT_DIV	0x0
N_INT, Bits[11:0]	0x30
CKLOUT1_OP	0x1
CLKOUT2_OP	0x0
PD_CLKOUT1	0x0
PD_CLKOUT2	0x1

Reference to Output Propagation Delay Settings

Reference to output propagation delay was not mentioned in the Design and Programming Example 1: Single ADF4377 section. In the Design and Programming Example 1: Single ADF4377 section, it was stated to prioritize to the lowest jitter performance. Setting the reference to output delay controls to their minimum setting achieves the lowest jitter by minimizing L_{NORM} and $L_{1/f}$ (see Figure 12, Figure 15, Figure 36, and Figure 39). As shown in Figure 14, the INV_CLKOUT setting does not affect jitter performance and can remain at its power on reset state of 0.

Table 27. SPI Summary, Propagation Delay

Bit Field	Value
EN_BLEED	0x0
BLEED_I bit fields, Bits[9:0]	0x0
BLEED_POL	0x0
R_DEL	0x0
N_DEL	0x0
INV_CLKOUT	0x0

Lock Detector Settings

To enable the lock detector (see the Lock Detector section), set the EN_LOL and EN_LDWIN bits to 1. The LD_COUNT bit field is determined by Equation 12. As mentioned in the Reference and Loop Filter Design section, a 460 kHz loop bandwidth (LPBW) was assumed.

$$PFD \quad Cycles = f_{PFD} \times 5/(2 \times \pi \times \text{LPBW}) = 250$$
$$\text{MHz} \times 5/(2 \times \pi \times 460 \quad \text{kHz}) = 432$$

The calculated minimum PFD cycle count of 432 is then compared to the PFD cycle column in Table 14, which results in 542 PFD cycles and LD_COUNT = 9.

To determine the LDWIN_PW setting from Table 16, calculate t_{IDEL} from Equation 10 or Equation 11. Because the BLEED_I bit fields, Bits[9:0], is set to 0 in the Reference to Output Propagation Delay Settings section, t_{IDEL} = 0. Based on Table 16, when t_{IDEL} = 0, LDWIN_PW is set to 0. The RST_LD bit is related to the lock detector and is set to 0 in normal use cases.

Table 28. SPI Summary, Lock Detector

Bit Field	Value
EN_LOL	0x1
EN_LDWIN	0x1
LD_COUNT	0x9
LDWIN_PW	0x0
RST_LD	0x0

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VCO Automatic Calibration Settings

The procedure to determine the SPI registers for an automatic VCO calibration is outlined in the VCO Calibration section.

The VCO calibration Step 1 enables the automatic calibration bit, EN_AUTOCAL, along with enabling several VCO calibration dividers, clocks, and the temperature sensor.

Table 29. SPI Summary, VCO Automatic Calibration, Step 1

Bit Field	Value
EN_DNCLK	0x1
EN_DRCLK	0x1
ADC_CLK_SEL	0x0
ADC_A_CONV	0x1
EN_AUTOCAL	0x1
EN_ADC_CNV	0x1
EN_ADC	0x1
EN_ADC_CLK	0x1
PD_ADC	0x0

In VCO calibration Step 2, Table 17 determines the state of CAL_CT_SEL, DCLK_DIV2, and DCLK_MODE based off the 250 MHz PFD frequency. DCLK_DIV1 must always be set to 1 regardless of PFD frequency. Table 17 provides an equation to calculate f_{DIV_RCLK}

$$f_{DIV\_RCLK} = f_{PFD}/2 \quad = 250 \quad MHz/2 \quad = \quad 125 \quad MHz$$

Table 30. SPI Summary, VCO Automatic Calibration, Step 2

Bit Field	Value
CAL_CT_SEL	0x1
DCLK_DIV2	0x0
DCLK_MODE	0x1
DCLK_DIV1	0x1

In the VCO calibration Step 3 and Step 4, Equation 13, Equation 14, Equation 15, and Equation 16 are provided to calculate the SYNTH_LOCK_TIMEOUT bit fields, Bits[14:0], VCO_ALC_TIMEOUT bit fields, Bits[14:0], VCO_BAND_DIV bits, and ADC_CLK_DIV bits from f_{DIV_RCLK}.

$$SYNTH\_LOCK\_TIMEOUT \geq Ceiling (200 \quad \mu s \times 125 \quad MHz) = 25000$$

$$VCO\_ALC\_TIMEOUT \geq Ceiling(50 \quad \mu s \times 125 \quad MHz) = 6250$$

$$VCO\_BAND\_DIV \geq Ceiling\left(\frac{15 \quad \mu s \times 125 \quad MHz}{16 \times 2^1}\right) = Ceiling(58.59375) = 59$$

$$ADC\_CLK\_DIV > Ceiling\left(\frac{\frac{125 \quad MHz}{400 \quad kHz} - \quad 2}{4}\right) = Ceiling (77.625) = 78$$

Table 31. SPI Summary, VCO Automatic Calibration, Step 3 and Step 4

Bit Field	Value
SYNTH_LOCK_TIMEOUT	0x61A8
VCO_ALC_TIMEOUT	0x186A
VCO_BAND_DIV	0x3B
ADC_CLK_DIV	0x4E

Double Buffer and Manual VCO Calibration Settings

If multiple frequency settings are desired, double buffering (see the Double Buffering section) and manual programming of the VCO settings can improve frequency switching times. In a single fixed frequency application, such as this design procedure, these modes are rarely required. Therefore, related bits can remain in their power-up default state.

Table 32. SPI Summary, Double Buffer and Manual VCO Calibration Settings

Bit Field	Value
M_VCO_CORE	0x0
M_VCO_BAND	0x0
M_VCO_BIAS	0x0
O_VCO_CORE	0x0
O_VCO_BAND	0x0
O_VCO_BIAS	0x0
CLKO_DIV_DB	0x0
DCLK_DIV_DB	0x0
O_VCO_DB	0x0
DEL_CTRL_DB	0x0

SPI Protocol Settings

The design goals stated for the SPI protocol (see the Serial Port section) are 1.8 V logic, 4-wire SPI, and optimize SPI write sequence. REG0000, REG0001, and REG0018 have the SPI related register bits, which are shown in Table 33 with the desired state based on the design goals. The power-on default state is assumed if the bit function is not listed as a design goal.

Table 33. SPI Summary - SPI Protocol

Bit Field	Value
CMOS_OV	0x0
SDO_ACTIVE, SDO_ACTIVE_R	0x1
ADDRESS_ASCENSION, ADDRESS_ASCENSION_R	0x0
SINGLE_INSTRUCTION	0x0
LSB_FIRST, LSB_FIRST_R	0x0

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Table 33. SPI Summary - SPI Protocol

Bit Field	Value
MAIN_READBACK_CONTROL	0x0

Remaining Register Settings

The Charge Pump Test Mode section,MUXOUT section, and Block Power Down Control section list several bit fields that are recommended for special purposes, such as debug or ambient die temperature measurements. For this normal use case, these bit fields must be set to their POR state (see Table 34). SOFT_RESET, SOFT_RESET_R, RST_SYS, and ADC_ST_CNV are the only remaining RW bit fields not mentioned yet, and must also be set to their POR state (see Table 34).

The bit columns in Table 42 have several cells without a name. These unnamed, reserved cells must be programmed to the state provided in Table 42 for proper operation.

Table 34. SPI Summary, Remaining Registers

Bit Field	Value
EN_CPTEST	0x0
CP_UP	0x0
CP_DOWN	0x0
MUXOUT	0x0
PD_CLK	0x0
PD_CALDAC	0x0
PD_ALL	0x0
PD_RDIV	0x0
PD_NDIV	0x0
PD_VCO	0x0
PD_LD	0x0
PD_PFDCP	0x0
SOFT_RESET, SOFT_RESET_R	0x0
RESET_SYS	0x0
ADC_ST_CNV	0x0

Programming Procedure

There are two different methods to power up the ADF4377. The most commonly used method provided in the Standard Power-Up and Initialization Sequence, Automatic VCO Calibration section is mandatory on the initial device power-up.

The method provided in the Fast Power-Up and Initialization, Manually Programmed VCO Calibration Settings (Optional) section is an optional power-up procedure after the initial power-up.

Standard Power-Up and Initialization Sequence, Automatic VCO Calibration

The following standard power-up and initialization sequence is the recommended procedure to power up and program the ADF4377:

1. Follow Step 1 through Step 5 in the Power-Up and Initialization Sequence section, using the register settings provided in the Design Procedure section.
2. It is optional to monitor the status of the VCO calibration bit fields, ADC_BUSY and FSM_BUSY. A VCO calibration is completed when ADC_BUSY transitions from high to low, followed by FSM_BUSY transitioning from high to low. Typical automatic VCO calibration times range from 3 ms to 9 ms.
3. After the VCO calibration is complete, disable the VCO calibration clocks by setting EN_DRCLK = EN_DNCLK = EN_ADC_CLK = 0. Disabling the VCO calibration clocks reduces the $V_{3.3V\_1}$ current by roughly 15 mA and reduces unwanted spurious content.
4. PLL is locked when the lock detector sets the LKDET pin and the LOCKED bit high.

Fast Power-Up and Initialization, Manually Programmed VCO Calibration Settings (Optional)

The purpose of the fast power-up and initialization method is to avoid the automatic VCO calibration time, which is typically 3 ms to 9 ms. For fixed clock frequency converter applications, such as this design and programming Example 1, automatic VCO calibration times are typically acceptable. The following list provides the steps to record the VCO calibration results on the initial power-up and manually program VCO Calibration settings on subsequent power ups:

1. On initial power, follow the procedure in the Standard Power-Up and Initialization Sequence, Automatic VCO Calibration section.
2. Record calibration results from the VCO_CORE, VCO_BAND, and VCO_BIAS bit fields and store the recorded results in memory. Note that each unique device and frequency combination generates different VCO_CORE, VCO_BAND, and VCO_BIAS values.
3. Subsequent power-up and initialization sequences (see the Power-Up and Initialization Sequence section) can bypass the automatic VCO calibration procedure by programming the override (O_VCO_CORE, O_VCO_BAND, and O_VCO_BIAS) and manual (M_VCO_CORE, M_VCO_BAND, and M_VCO_BIAS) VCO register bits with the register settings provided in Table 35. All other bit fields from the Design Procedure section remain the same.

Table 35. Manually Programmed VCO Calibration Settings

Bit Fields	Value
EN_AUTOCAL	0x0
EN_DRCLK	0x0
EN_DNCLK	0x0
EN_ADC_CLK	0x0
O_VCO_CORE	0x1
O_VCO_BAND	0x1
O_VCO_BIAS	0x1

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Table 35. Manually Programmed VCO Calibration Settings

Bit Fields	Value
M_VCO_CORE M_VCO_BAND M_VCO_BIAS	Program M_VCO_CORE, M_VCO_BAND, and M_VCO_BIAS with recorded VCO_CORE, VCO_BAND, and VCO_BIAS values, respectively, from the Standard Power-Up and Initialization Sequence, Automatic VCO Calibration section

ALIGNING MULTIPLE ADF4377 OUTPUT PHASES

Aligning multiple ADF4377 output phases can be broken into two steps. The first step ensures that the reference dividers, reference doubler, and clock output divider of the multiple devices are setup correctly to ensure phase alignment. The second step minimizes output to output skew between multiple ADF4377 devices.

Step 1: Phase Alignment

The ADF4377 architecture includes the clock output divider and the output invert inside the integer PLL feedback loop (see Figure 1), which allows the locked PLL to align the clock output divider phase to the reference input phase. Therefore, to align multiple ADF4377 output phases, ensure that the reference phases are aligned at all the reference input pins of the ADF4377.

Because the reference divider and reference doubler are outside of the PLL loop, refer to Table 36 to ensure that phase alignment between multiple ADF4377 devices is guaranteed.

Table 36. Reference Settings to Align Multiple ADF4377 Devices

Reference Divider and Doubler State	Guaranteed Reference to Output Phase Alignment
EN_RDBLR = 1	Yes
R_DIV = 1	Yes
R_DIV > 1	When f_{OUT}/f_{REF} = integer, and $f_{REF} \leq f_{OUT}$

Step 2: Output to Output Skew Adjustment

Any variation in reference input to output propagation delay (t_{PD}) between multiple ADF4377 devices presents itself as output skew between multiple ADF4377 devices.

To minimize t_{PD} across process and temperature, select the DMA of the reference input buffer by setting REF_SEL = 0. When the DMA is selected, the typical t_{PD} standard deviation due to process variation is 3 ps with a temperature coefficient ($t_{PD\text{-}TC}$) of 0.03 ps/°C, as shown in Figure 24 and Figure 20, respectively.

Due to the controlled t_{PD} of the ADF4377 devices, it is reasonable to expect that a significant portion of the total system skew (t_{SKEW_SYSTEM}) is due to propagation delay mismatches in traces or cables (t_{SKEW_B}, t_{SKEW_D}), and skew in other components (t_{SKEW_A}) or instruments (t_{MEAS_ERROR}, t_{CHAN1}, and t_{CHAN2}). Figure 90 and Equation 24 provide several sources of possible output skew error in a typical system. The *Analog Dialogue* article, "Clock Skew in Large Multi-GHz Clock Trees" (Volume 53, January 2019), outlines the skew trade-offs in component selection, board design, and end-user cost requirements in large clock trees.

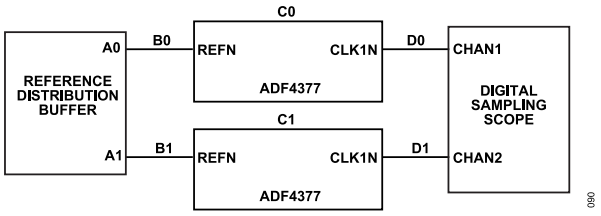

Figure 90. Total System Skew

$$t_{SKEW\_SYSTEM} = t_{SKEW\_A} + t_{SKEW\_B} + t_{SKEW\_C} + t_{SKEW\_D} + t_{MEAS\_ERROR} \quad (24)$$

where:

$t_{SKEW\_A} = t_{A1} - t_{A0}$

$t_{SKEW\_B} = t_{PD\_B1} - t_{PD\_B0}$

$t_{SKEW\_C} = t_{PD\_C1} - t_{PD\_C0}$

$t_{SKEW\_D} = t_{PD\_D1} - t_{PD\_D0}$

$t_{MEAS\_ERROR} = t_{CHAN1} - t_{CHAN2}$

To further minimize clock skew between multiple clocks, the ADF4377 devices provide SPI programmable adjustments to increase or decrease the t_{PD} in sub-ps steps. Table 37 and Table 38 provide a comparison of the multiple reference to output delay controls. In large clock trees, these t_{PD} adjustments can alleviate output to output skew trade-offs in component selection, board design, and end-user cost requirements.

Table 37. ADF4377 Reference to Output Delay Control Comparison

Parameters	Reference Delay	Feedback Delay	Charge Pump Bleed Current	Output Invert
Register Bits	R_DEL	N_DEL	EN_BLEED, BLEED_I bit fields, Bits[9:0], BLEED_POL	INV_CLKOUT
t_{PD}	Increases	Decreases	BLEED_POL = 0, increases BLEED_POL = 1, decreases	Inverts output, see Table 19
Number of Steps	127	127	1023	
Step Size	~1 ps	~1 ps	~0.01 ps to 65 ps, varies with CP_I and f_{PFD} Equation 9	$1/(2 \times f_{OUT})$

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Table 38. ADF4377 Reference to Output Typical Performance Impact

Parameters	Reference and Feedback Delay	Charge Pump Bleed Current	Output Invert
Temperature Coefficient	Minimal, Figure 18 and Figure 21	None, Figure 19 and Figure 22	None
L_{NORM}	< 1 dB, Figure 39	< 1 dB, Figure 36	None
$L_{1/f}$	< 1 dB, Figure 39	< 4 dB, Figure 36	None
Spurious	Minimal	f_{PFD} ≥ 50 MHz: minimal, f_{PFD} < 50 MHz, contact ADI	Minimal
Lock Detector	None	See the Lock Detector section	None

Figure 39 and Figure 37 show a general trend that an increasing magnitude of R_DEL, N_DEL, or BLEED_I bit fields, Bits[9:0] causes a small increase in L_{NORM} and $L_{1/f}$. Increases in L_{NORM} and $L_{1/f}$ result in clock jitter (see Figure 12 and Figure 15). Therefore, in the most performance sensitive applications, identifying ways to minimize the magnitude of the R_DEL, N_DEL, or BLEED_I bit fields, Bits[9:0] values is desired. As an example, Figure 91 provides two skew adjustment methods to minimize the skew in Figure 90. Method 1 only adjusts one of the reference to output delay adjustments provided in Table 37. Method 1 results in an R_DEL, N_DEL, or BLEED_I bit fields, Bits[9:0] maximum adjustment equal to half an output cycle, or 1/(2 × f_{OUT}). Method 2 minimizes the magnitude of R_DEL, N_DEL, or BLEED_I bit fields, Bits[9:0] by utilizing the output invert along with either R_DEL, N_DEL, or BLEED_I bit fields, Bits[9:0] adjustments. When compared to Method 1, Method 2 results in a lower R_DEL, N_DEL, or BLEED_I bit fields, Bits[9:0] maximum adjustment of a quarter cycle output cycle, or 1/(4 × f_{OUT}). Method 2 is furthered described in Table 39.

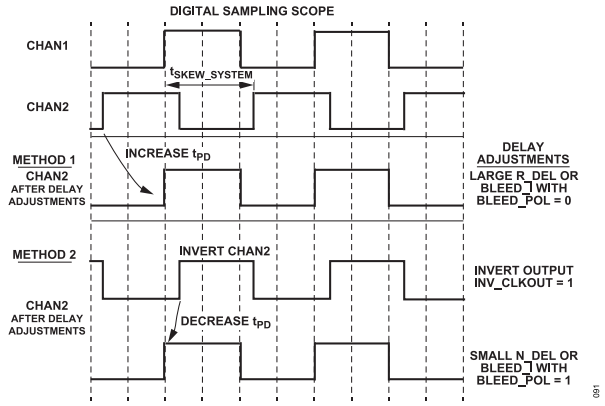

Figure 91. Skew Adjustment Methods

Table 39. Method 2: Skew Adjustment

t_{SKEW_SYSTEM}	Procedure
$0 < t_{SKEW\_SYSTEM} \leq 1/(4 \times f_{OUT})$	INV_CLKOUT = 0 and decrease t_{PD}
$1/(4 \times f_{OUT}) < t_{SKEW\_SYSTEM} \leq 2/(4 \times f_{OUT})$	INV_CLKOUT = 1 and increase t_{PD}
$2/(4 \times f_{OUT}) < t_{SKEW\_SYSTEM} \leq 3/(4 \times f_{OUT})$	INV_CLKOUT = 1 and decrease t_{PD}
$3/(4 \times f_{OUT}) < t_{SKEW\_SYSTEM} \leq 1/f_{OUT}$	INV_CLKOUT = 0 and increase t_{PD}

DESIGN EXAMPLE 2: JESD204B/C MULTICHIP CLOCK AND SYSREF ALIGNMENT

This design Example 2 focuses on the system level approach of ADI to minimize clock skew between converters, such as the AD9213, that include a time to digital converter (TDC). For detailed ADF4377 loop filter and register map design, follow the procedure outlined in the Design and Programming Example 1: Single ADF4377 section. Device specific programming and programming details of the AD9213 and Stage 1 distribution IC are beyond the scope of this example.

For this design example, assume the following goals:

- Clock two AD9213 devices with two separate ADF4377 devices
- Minimize clock skew at time zero
- Provide procedure to measure and reduce clock skew errors

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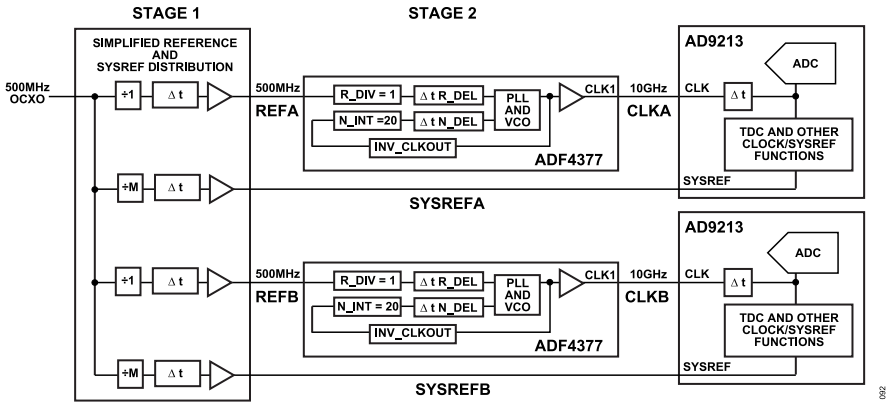

Figure 92. Design Example 2: JESD204B/C Multichip Clock and SYSREF Alignment

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Design Considerations

The Reference and SYSREF Distribution Selection section, Board Layout Considerations section, Skew Adjustment Options section, Skew Measurement, Adjustments and System Error section, and Power-Up, Programming, and Measurement Sequence section provide an overview of several design considerations when designing a low clock skew system with multiple ADF4377 devices and multiple JESD204B/C converters that include a TDC.

Reference and SYSREF Distribution Selection

In high performance applications that require minimum clock skew and drift, it is recommended to choose a reference distribution device whose additive noise floor meets the requirements described in the Reference Source Considerations section, and whose output slew rate allows for the DMA option of the ADF4377 reference input buffer (see Table 7). The DMA option minimizes $t_{PD\text{-}TC}$, as shown in Figure 20. Most reference distribution ICs output a square wave. The slew rate of a square wave is determined by Equation 25.

$$Slew\ Rate = \frac{V\ p\text{-}p \times (\%\ Upper\ t_{RISE}\ Threshold - \%\ Lower\ t_{RISE}\ Threshold)}{t_{RISE}} \quad (25)$$

The HMC7044, HMC7043, LTC6952, LTC6953, LTC6955, LTC6954, or LTC6957-1 are adequate reference distribution ICs for the noise floor and rise time requirements.

By using multiple outputs from a single reference and SYSREF distribution IC, the reference and SYSREF temperature delay drift match. See the LTC6952, LTC6953, and LTC6957-1 data sheets for more information on output skew variation over process per output to aid in SYSREF output selection. Choosing the outputs with the least skew for SYSREF outputs improves the skew adjustment errors, as described in the Skew Measurement, Adjustments and System Error section.

Selecting a JESD204B/C reference and SYSREF distribution IC requires knowledge of the AD9213 JESD204B serial lane rates and the clock and SYSREF requirements of the field programmable gate array (FPGA). Both these topics are beyond the scope of this data sheet. However, ADI has created several JESD204B/C development platforms that provide hardware and software examples that can aid further in the reference and SYSREF distribution IC selection. Several of these platforms are available on the Analog Devices website.

Board Layout Considerations

During hardware design, it is best to match the electrical lengths (ℓ) for the reference, clock, and SYSREF traces in Figure 92, as shown in Table 40.

Table 40. Trace Length Matching for Skew Optimization

If Skew Adjustments Performed	Skew Optimization	Skew Temperature Coefficient Optimization
No	$\ell_{REFA} = \ell_{REFB}$, $\ell_{CLKA} = \ell_{CLKB}$, and $\ell_{SYSREFA} = \ell_{SYSREFB}$	$\ell_{SYSREFx} = \ell_{REFx} + \ell_{CLKx}$
Yes	$\ell_{SYSREFA} = \ell_{SYSREFB}$	$\ell_{SYSREFx} = \ell_{REFx} + \ell_{CLKx}$

Refer to the *Analog Dialogue* article, "Clock Skew in Large Multi-GHz Clock Trees" (Volume 53, January 2019) for more information on PCB material selection, transmission line selection, cable selection, and several other concerns related to clock skew.

Signal attenuation is proportional to the length of the trace and signal frequency. Converter clock traces must be treated as RF traces because any unwanted spurious or noise that couples onto the clock signals can affect the performance of the converters. Therefore, it is recommended to minimize the ℓ_{CLKA} and ℓ_{CLKB} trace lengths to optimize performance and limit attenuation. Refer to the ADC Clock and Jitter Considerations section for additional information on clock performance concerns, routing, and recommended schematics.

In most cases, trace matching board layout errors can be corrected with the Δt functions in the reference and SYSREF distribution IC, the ADF4377 or the AD9213, shown in Figure 92.

Skew Adjustment Options

Figure 92 has skew adjustment (Δt) blocks in the Stage 1 IC, the ADF4377, and the AD9213. In most cases, the ADF4377 is the preferred skew adjustment option in terms of maximizing performance.

The ADF4377 Δt blocks are discussed in Table 37. For this design example, either R_DEL and N_DEL or BLEED_I bit fields, Bits[9:0] are valid options. However, in Figure 92, only R_DEL and N_DEL are shown.

The AD9213 also provides a Δt block capable of sub-ps step sizes. Like any Δt block, there is an opportunity for increased phase noise. The ADF4377 and AD9213 Δt blocks affect phase noise at different frequency offsets, as shown in Table 41.

Table 41. Clock Phase Noise Region Affected by ADF4377 and AD9213 Δt Blocks

	In-Band Phase Noise	Wideband Phase Noise
Δt Block	< ADF4377 Loop Filter Bandwidth	~10 MHz to f_{CLK}
ADF4377 Δt	Minimal additive noise, refer to Table 38	None
AD9213 Δt	None	Minimal additive noise

The reference and SYSREF distribution IC in Figure 92 has a Δt block for each output. The typical Stage 1 IC skew adjustment step size is in the 11 ps (LTC6952, LTC6953) to 25 ps (HMC7044, HMC7043) range. These Δt blocks typically increase the phase

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noise floor of the output, which then impacts the in-band performance of the ADF4377. As a result, the Stage 1 reference and SYSREF distribution IC Δt blocks are recommended for SYSREF signals only.

Skew Measurement, Adjustments and System Error

In Figure 92, a TDC is shown in the AD9213. The AD9213 TDC has the ability to measure the time delta between the rising edge of the AD9213 SYSREF input (t_{SYSREF}) and the rising edge of the AD9213 clock input (t_{CLK}) as shown in Equation 26.

$$\Delta t_{CLK\_SYSREF} = t_{CLK} - t_{SYSREF} \quad (26)$$

To determine the clock skew between the clock inputs of the first AD9213 device and the second AD9213 device, measure the Δt_{CLK_SYSREF} for both AD9213 devices.

$$\Delta t_{CLK\_SYSREFA} = t_{CLKA} - t_{SYSREFA}$$
$$\Delta t_{CLK\_SYSREFB} = t_{CLKB} - t_{SYSREFB}$$

By making the assumption that the SYSREFA and SYSREFB signals arrive at both AD9213 devices at the same moment in time, the clock to clock skew between both AD9213 devices can be calculated as shown in the following equation.

Assume, $t_{SYSREFA} - t_{ERROR} = t_{SYSREFB}$

$$t_{CLK\_SKEW} = \Delta t_{CLK\_SYSREFA} - \Delta t_{CLK\_SYSREFB}$$
$$t_{CLK\_SKEW} = (t_{CLKA} - t_{SYSREFA}) - (t_{CLKB} - t_{SYSREFB})$$
$$substituting, \quad t_{SYSREFA} - t_{ERROR} \quad for \quad t_{SYSREFB}$$
$$t_{CLK\_SKEW} = t_{CLKA} - t_{CLKB} + t_{ERROR}$$

If care is taken in the Board Layout Considerations section, t_{ERROR} limits the clock skew accuracy to roughly 5 ps to 10 ps. This error is due to the sum of errors from the SYSREF output skew from Stage 1, SYSREFA, and SYSREFB electrical trace matching, and the first AD9213 and the second AD9213 TDC measurement error. Contact ADI if less than 5 ps to 10 ps clock skew accuracy at the clock inputs of the AD9213 is required.

After t_{CLK_SKEW} is calculated, program the second ADF4377 skew adjustment using Method 2, as shown in Figure 91. After the skew adjustment is programmed, a t_{CLK_SKEW} measurement can be repeated as necessary to further fine tune the adjustment or average out measurement repeatability error.

Power-Up, Programming, and Measurement Sequence

The following list provides the recommended system level power-up, device programming, and skew measurement sequence:

1. Power up system
2. Program Stage 1 IC, ADF4377 devices, and AD9213 devices to their expected frequency plan
3. Allow temperature of the components to settle
4. Perform clock skew measurement
5. Program skew adjustments per Method 2, as shown in Figure 91
6. Perform JESD204B/C initialization

ADC CLOCK AND JITTER CONSIDERATIONS

Estimating ADC SNR and Clock Jitter Requirements

Adding noise directly to a clean signal reduces its signal-to-noise ratio (SNR). In data acquisition applications, digitizing a clean signal with a noisy clock signal also degrades the SNR. This issue is best explained in the time domain by using jitter instead of phase noise. For this discussion, assume that the jitter is white (flat with frequency) and of Gaussian distribution.

Figure 93 shows a sine wave signal entering a typical data acquisition circuit composed of an ADC, an input signal amplifier, and a sampling clock. Also shown in Figure 93 are three signal sampling scenarios for sampling the sine wave at its zero crossing.

In the first scenario, a perfect sine wave input is buffered by a noiseless amplifier to drive the ADC. Sampling is performed by a perfect, zero jitter clock. Without any added noise or sampling clock jitter, the digitized output value of the ADC is very clearly determined and perfectly repeatable from cycle to cycle.

In the second scenario, a perfect sine wave input is buffered by a noisy amplifier to drive the ADC. Sampling is performed by a perfect, zero jitter clock. The added noise results in an uncertainty in the digitized value, causing an error term that degrades the SNR. The degraded SNR in this scenario, from adding noise to the signal, is expected.

In the third scenario, a perfect sine wave input is buffered by a noiseless amplifier to drive the ADC. Sampling is performed by a clock signal with added jitter. Note that as the signal is slewing, the jitter of the clock signal leads to an uncertainty in the digitized value and an error term, like in the second scenario. Again, this error term degrades the SNR.

A real-world system has both additive amplifier noise and sample clock jitter. After the signal is digitized, determining the root cause of any SNR degradation, amplifier noise or sampling clock jitter, is essentially impossible.

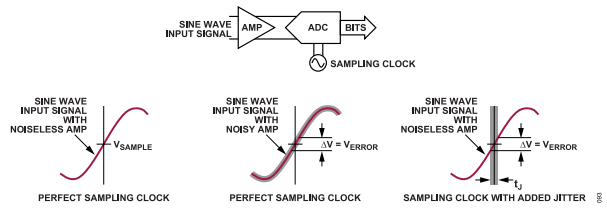

Figure 93. A Typical Data Acquisition Circuit Showing the Sampling Error Effects of a Noisy Amplifier and a Jittery Clock

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Degradation of the SNR due to sample clock jitter only occurs if the analog input signal is slewing. If the analog input signal is stationary (dc), it does not matter when in time the sampling occurs. Additionally, a faster slewing input signal yields a greater error (more noise) than a slower slewing input signal.

Figure 94 demonstrates this effect. Note how much larger the error term is with the fast slewing signal than with the slow slewing signal. To maintain the SNR performance of the data converter, digitization of high input frequency signals requires a clock with much less jitter than applications with lower frequency input signals.

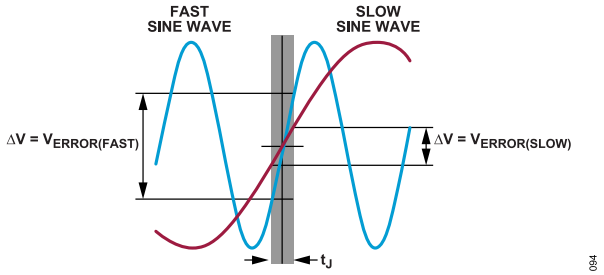

Figure 94. Fast and Slow Sine Wave Signals Sampled with a Jittery Clock

It is important to note that the frequency of the analog input signal determines the jitter requirement of the sample clock. The actual sample clock frequency does not matter. Many ADC applications that under sample high frequency signals have especially challenging sample clock jitter requirements.

This information is useful for gaining an intuitive feel for the SNR degradation due to sampling clock jitter. Quantitatively, the actual sample clock jitter requirement for a given application is calculated as follows:

$$t_{J(TOTAL)} = \frac{10^{-SNR_{dB}/20}}{2 \times \pi \times f_{SIG}} \quad (27)$$

where:

$t_{J(TOTAL)}$ is the total RMS jitter in seconds

SNR_{dB} is the SNR requirement in decibels

f_{SIG} is the highest frequency signal to be digitized, expressed in Hz

The total jitter is the rms sum of the aperture jitter of the ADC and the sample clock jitter, calculated as follows:

$$t_{J(TOTAL)} = \sqrt{t_{J(CLK)}^2 + t_{J(ADC)}^2} \quad (28)$$

Alternatively, for a given total jitter, the attainable SNR is calculated as follows:

$$SNR_{dB} = -20 \times \log\left(2 \times \pi \times f_{SIG} \times t_{J(TOTAL)}\right) \quad (29)$$

These calculations assume a full-scale sine wave input signal. If the input signal is a complex, modulated signal with a moderate crest factor, the peak slew rate of the signal may be lower and the sample clock jitter requirement may be relaxed.

These calculations are also theoretical. They assume a noiseless ADC with infinite resolution. All realistic ADCs have both added noise and a resolution limit. The limitations of the ADC must be accounted for to prevent overspecifying the sampling clock.

Figure 95 plots the previous equations and provides a way to estimate the sampling clock jitter requirement for a given input signal or the expected SNR performance for a given sample clock jitter.

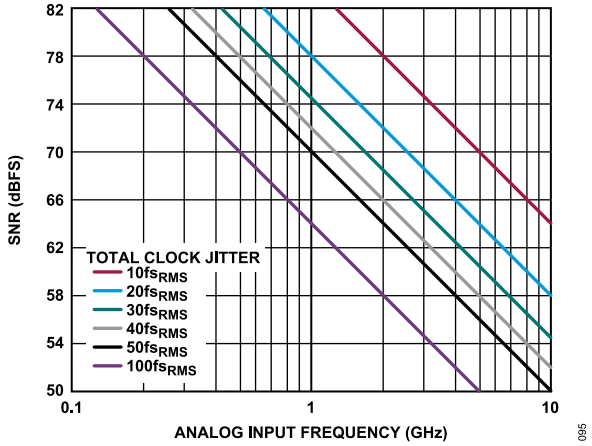

Figure 95. SNR vs. Analog Input Frequency with Various Levels of Clock Jitter

Measuring Clock Jitter Indirectly Using ADC SNR

For some applications, integrating the phase noise of a clock generator within a defined offset frequency range (for example, 12 kHz to 20 MHz) is sufficient to calculate the impact of the clock on the overall system performance. In these situations, the rms jitter can be calculated from a phase noise measurement.

However, other applications require knowledge of the phase noise of the clock at frequency offsets that exceed the capabilities of phase noise analyzers. This limitation makes it difficult to calculate jitter from a phase noise measurement.

The rms jitter of an ADC clock source can be indirectly measured by comparing a jitter dominated SNR measurement to a non-jitter dominated SNR measurement. A jitter dominated SNR measurement (SNR_{JITTER}) is created by applying a low jitter, high frequency full-scale sine wave to the ADC analog input. A non-jitter dominated SNR measurement (SNR_{BASE}) is created by applying a very low amplitude (or low frequency) sine wave to the ADC analog input. The total clock jitter ($t_{J(TOTAL)}$) can be calculated using Equation 30.

$$t_{J(TOTAL)} = \frac{10^{1/2} \times \log_{10}\left(10^{-SNR_{JITTER}/10} - 10^{-SNR_{BASE}/10}\right)}{2 \times \pi \times f_{SIG}} \quad (30)$$

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Assuming the inherent aperture jitter of the ADC ($t_{J(ADC)}$) is known, the jitter of the clock generator ($t_{J(CLK)}$) is obtained using Equation 28.

ADC Sample Clock Input Drive Requirements

Modern high speed, high resolution ADCs have a high dynamic range and are sensitive to any unwanted noise or spurious source. Noise or interfering signals on the analog signal input, the voltage reference, or the sampling clock input can easily appear in the digitized data. To deliver the full performance of any ADC, the sampling clock input must be driven with a clean, low jitter signal.

Figure 96 shows a simplified version of a typical ADC sample clock input. In Figure 96, the input pins may be labeled ENC± for encode or CLK± for clock in different ADCs. The input is composed of a differential limiting amplifier stage followed by a buffer that directly controls the track and hold stage of the ADC.

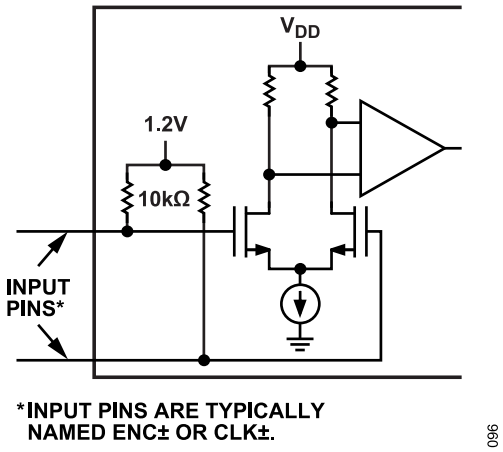

Figure 96. Simplified Sample Clock Input Circuit

The sample clock input amplifier also benefits from a fast slewing input signal because the amplifier has noise of its own. By slewing through the crossover region quickly, the amplifier noise creates less jitter than if the transition were slow. As shown in Figure 96, the sample clock input of the ADC is typically differential, with a differential sampling clock delivering the best performance. Figure 96 also shows the sample clock input with a different common-mode input voltage than the outputs of the ADF4377. Most ADC applications require ac coupling to convert between the two common-mode voltages.

Transmission Lines and Termination

Interconnection of high speed signaling with fast rise and fall times requires the use of transmission lines with properly matched termination. The transmission lines may be stripline, microstrip or any other design topology. A detailed discussion of transmission line design is beyond the scope of this data sheet. Any mismatch between the characteristic impedance of the transmission line and the terminating impedance results in a portion of the signal reflecting back toward the other end of the transmission line. In the extreme case of an open or short-circuit termination, all of the signal is reflected back. This signal reflection leads to overshoot and ringing on the waveform. Figure 97 shows the preferred method of far-end termination of the transmission line.

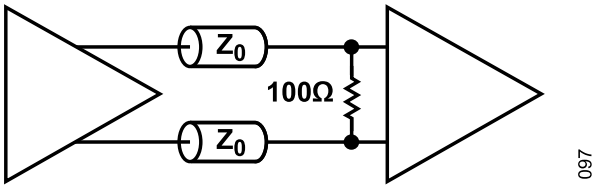

Figure 97. Far-End Transmission Line Termination (Z_O = 50 Ω)

ADF4377 Output Networks

The differential outputs of the ADF4377 are designed to interface with most differential signal devices while driving transmission lines with far-end termination. Figure 98, Figure 99, and Figure 100 shows ac-coupled output configurations. Note that some receiver devices have the 100 Ω termination resistor internal to the device, in which case the external 100 Ω resistor is unnecessary. The ADF4377 also interfaces with single-ended 50 Ω end terminations. In this case, the unused output requires an ac-coupled 50 Ω termination. For the single-ended example in Figure 100, the CLKxP and CLKxN pins may be swapped.

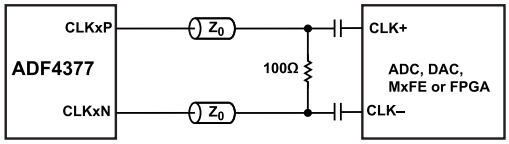

Figure 98. Common Clock Interface: Differential Clock with On Board End Termination (Z_O = 50 Ω)

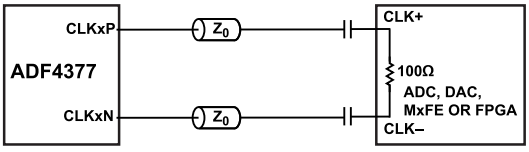

Figure 99. Common Clock Interface: Differential Clock with On-Chip End Termination (Z_O = 50 Ω)

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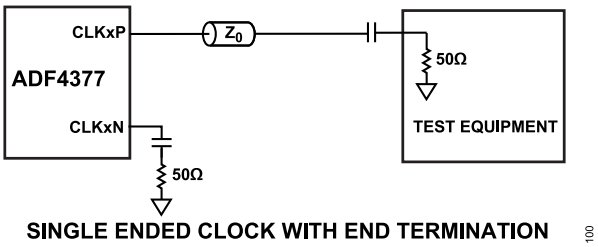

Figure 100. Common Clock Interface: Single Ended Clock with End Termination (Z_O = 50 Ω)

MEASURING DIFFERENTIAL SPURS WITH A SINGLE-ENDED TEST INSTRUMENT

Using a spectrum analyzer to measure spurious signals on the single-ended output of a clock generation chip gives pessimistic results, particularly for outputs that approximate square waves. There are two reasons for this.

First, because the spurious energy is often an ac signal superimposed on the power supply, a differential output rejects the spurs to within the matching of the positive and negative outputs. Observing only one side of the differential output provides no rejection.

Second, and most importantly, the spectrum analyzer displays all of the energy at its input, including amplitude modulation that occurs at the top and bottom pedestal voltage of the square wave. However, only amplitude modulation near a zero crossing affects the clock.

The best way to remove this measurement error is to drive the clock generator output differentially into a limiting buffer on a separate clean power supply. One of the differential outputs of the limiting buffer can then connect to a spectrum analyzer to correctly measure the spurious energy. An example of this technique using the ADF4377 as the clock generator and an HMC940 as the limiter is shown in Figure 101.

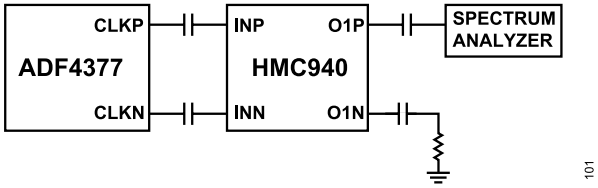

Figure 101. Example of Spurious Measurement Techniques

APPLICATION CIRCUITS

Parallel ADF4377 Devices, 13 fs RMS Jitter

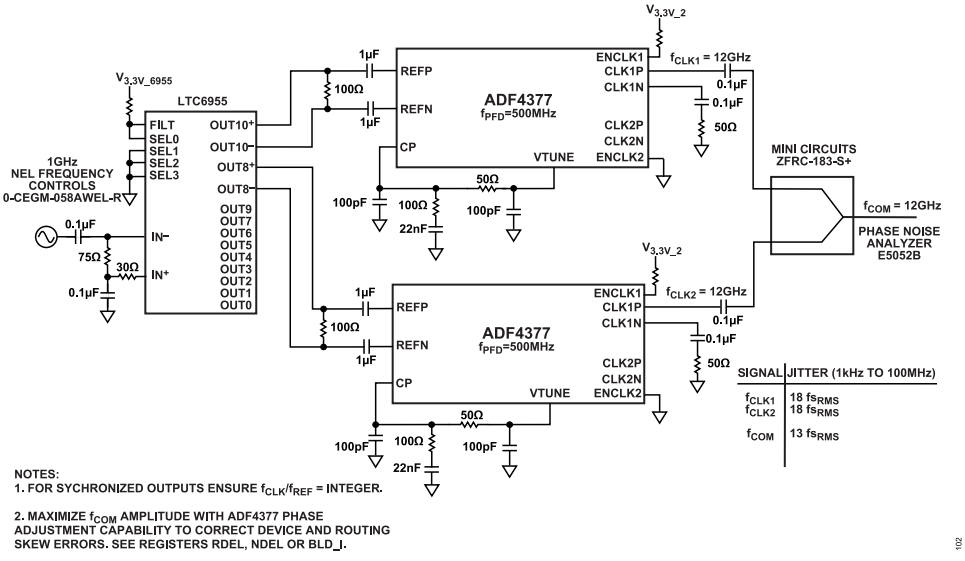

Figure 102. Block Diagram of Parallel ADF4377 Devices

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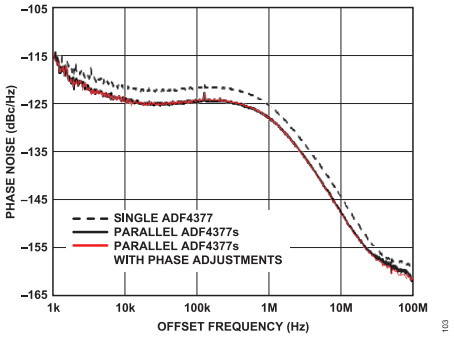

Figure 103. 12 GHz Parallel ADF4377s, 13 fs_{rms} Jitter

AD9082 Error Vector Magnitude (EVM) with ADF4377 as Clock

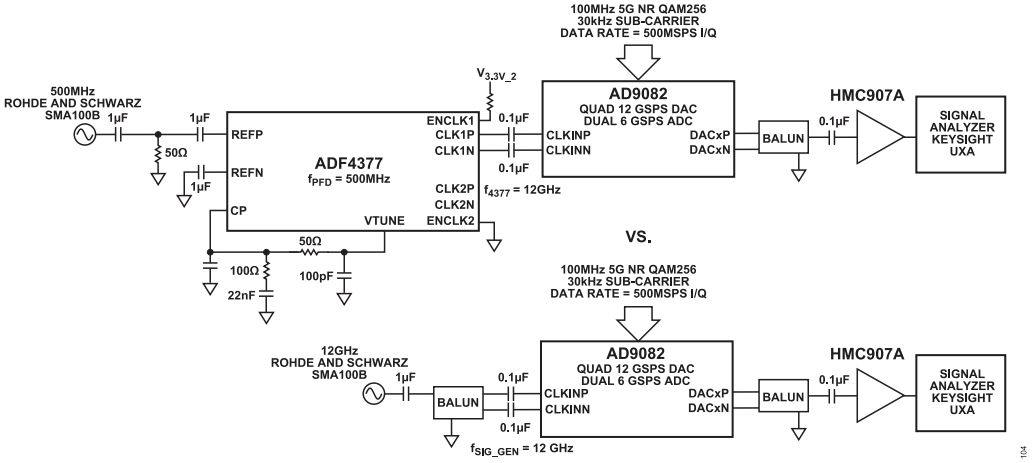

Figure 104. AD9082 and ADF4377 Measurement Schematic

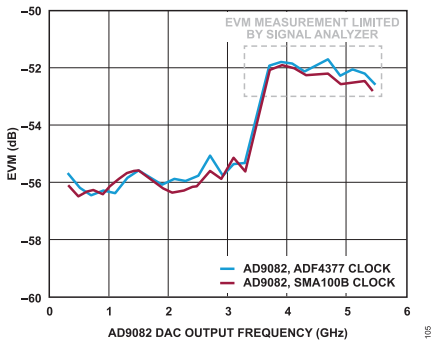

Figure 105. AD9082 EVM with ADF4377 as 12 GHz Clock

REGISTER MAP

Table 42. ADF4377 Register Map

Reg	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	SOFT_RESET_R	LSB_FIRST_R	ADDRESS_ASCENSION_R	SDO_ACTIVE_R	SDO_ACTIVE	ADDRESS_ASCENSION	LSB_FIRST	SOFT_RESET	0x00	R/W
0x01	SINGLE_INSTRUCTION	0	MAIN_READBACK_CONTROL	0	0	0	0	0	0x00	R/W
0x02	RESERVED				R002_RSV1				0x00	R
0x03	RESERVED				CHIP_TYPE				0x00	R
0x04	PRODUCT_ID[7:0]								0x00	R
0x05	PRODUCT_ID[15:8]								0x00	R
0x06	R006_RSV2				R006_RSV1				0x00	R
0x0A	SCRATCHPAD								0x00	R/W
0x0B	SPI_REVISION								0x00	R
0x0C	VENDOR_ID[7:0]								0x56	R
0x0D	VENDOR_ID[15:8]								0x04	R
0x0F	0	0	0	0	0	0	0	0	0x00	R/W
0x10	N_INT[7:0]								0x80	R/W
0x11	EN_AUTOCAL	EN_RDBLR	DCLK_DIV2		N_INT[11:8]				0x00	R/W
0x12	CLKOUT_DIV		R_DIV						0x01	R/W
0x13	0	0	M_VCO_CORE		M_VCO_BIAS				0x00	R/W
0x14	M_VCO_BAND								0x00	R/W
0x15	BLEED_I[1:0]		BLEED_POL	EN_BLEED	CP_I				0x00	R/W
0x16	BLEED_I[9:2]								0x00	R/W
0x17	INV_CLKOUT	N_DEL							0x00	R/W
0x18	CMOS_OV	R_DEL							0x00	R/W
0x19	CLKOUT2_OP		CLKOUT1_OP		PD_CLK	PD_RDET	PD_ADC	PD_CALDAC	0x04	R/W
0x1A	PD_ALL	PD_RDIV	PD_NDIV	PD_VCO	PD_LD	PD_PFDCP	PD_CLKOUT1	PD_CLKOUT2	0x83	R/W
0x1B	EN_LOL	LDWIN_PW	EN_LDWIN	LD_COUNT					0x00	R/W
0x1C	EN_DNCLK	EN_DRCLK	0	0	0	RST_LD	0	1	0x00	R/W
0x1D	MUXOUT				0	EN_CPTEST	CP_DOWN	CP_UP	0x00	R/W
0x1E	0	0	0	0	0	0	0	0	0x00	R/W
0x1F	BST_REF	FILT_REF	REF_SEL	0	0	1	1	1	0x00	R/W
0x20	0	0	0	RST_SYS	EN_ADC_CLK	0	0	1	0x00	R/W
0x21	1	1	0	1	0	0	1	1	0x00	R/W
0x22	0	0	1	1	0	0	1	0	0x00	R/W
0x23	CAL_CT_SEL	0	0	1	1	0	0	0	0x00	R/W
0x24	0	0	0	0	0	DCLK_MODE	0	0	0x00	R/W
0x25	CLKODIV_DB	DCLK_DIV_DB	0	1	0	1	1	0	0x00	R/W
0x26	VCO_BAND_DIV								0x00	R/W
0x27	SYNTH_LOCK_TIMEOUT[7:0]								0x00	R/W
0x28	O_VCO_DB	SYNTH_LOCK_TIMEOUT[14:8]							0x00	R/W
0x29	VCO_ALC_TIMEOUT[7:0]								0x00	R/W
0x2A	DEL_CTRL_DB	VCO_ALC_TIMEOUT[14:8]							0x00	R/W
0x2B	0	0	0	0	0	0	0	0	0x00	R/W
0x2C	1	1	0	0	0	0	0	0	0x00	R/W
0x2D	ADC_CLK_DIV								0x00	R/W
0x2E	EN_ADC_CNV	0	0	0	0	0	EN_ADC	ADC_A_CONV	0x00	R/W
0x2F	0	0	0	0	0	0	DCLK_DIV1		0x00	R/W

REGISTER MAP

Table 42. ADF4377 Register Map

Reg	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x30	0	0	0	0	0	0	0	0	0x00	R/W
0x31	0	0	0	0	1	0	0	1	0x00	R/W
0x32	0	ADC_CLK_SEL	0	0	1	0	0	1	0x00	R/W
0x33	0	0	0	1	1	0	0	0	0x00	R/W
0x34	0	0	0	0	1	0	0	0	0x00	R/W
0x35	0	0	0	0	0	0	0	0	0x00	R/W
0x36	0	0	0	0	0	0	0	0	0x00	R/W
0x37	0	0	0	0	0	0	0	0	0x00	R/W
0x38	R038_RSV1								0x00	R
0x39	0	0	0	0	0	0	0	0	0x00	R/W
0x3A	0	1	0	1	1	1	0	1	0x00	R/W
0x3B	0	0	1	0	1	0	1	1	0x00	R/W
0x3C	0	0	0	0	0	0	0	0	0x00	R/W
0x3D	0	0	0	0	O_VCO_BAND	O_VCO_CORE	O_VCO_BIAS	0	0x00	R/W
0x3E	0	0	0	0	0	0	0	0	0x00	R/W
0x3F	0	0	0	0	0	0	0	0	0x00	R/W
0x40	0	0	0	0	0	0	0	0	0x00	R/W
0x41	0	0	0	0	0	0	0	0	0x00	R/W
0x42	0	0	0	0	0	1	0	1	0x00	R/W
0x43	0	0	0	0	0	0	0	0	0x00	R/W
0x44	0	0	0	0	0	0	0	0	0x00	R/W
0x45	0	0	0	0	0	0	0	ADC_ST_CNV	0x00	R/W
0x46	R046_RSV1[7:0]								0x00	R
0x47	R046_RSV1[15:8]								0x00	R
0x48	R046_RSV1[23:16]								0x00	R
0x49	EN_CLK2	EN_CLK1	R049_RSV2	R049_RSV1	REF_OK	ADC_BUSY	FSM_BUSY	LOCKED	0x00	R
0x4A	R04A_RSV1								0x00	R
0x4B	RESERVED						VCO_CORE		0x00	R
0x4C	CHIP_TEMP[7:0]								0x00	R
0x4D	RESERVED							CHIP_TEMP[8]	0x00	R
0x4E	R04E_RSV1								0x00	R
0x4F	VCO_BAND								0x00	R
0x50	R050_RSV1								0x00	R
0x51	RESERVED				VCO_BIAS				0x00	R
0x52	RESERVED				R052_RSV1				0x00	R
0x53	RESERVED					R053_RSV2		R053_RSV1	0x00	R
0x54	VERSION								0x00	R

REGISTER DETAILS

Address: 0x00, Reset: 0x00, Name: REG0000

REGISTER MAP

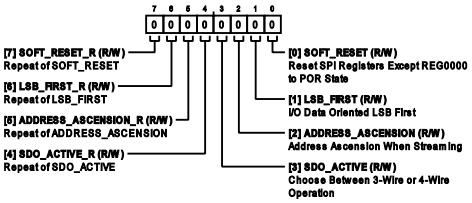

Figure 106.

Table 43. Bit Descriptions for REG0000

Bits	Bit Name	Description	Reset	Access
7	SOFT_RESET_R	Repeat of SOFT_RESET.	0x0	R/W
6	LSB_FIRST_R	Repeat of LSB_FIRST.	0x0	R/W
5	ADDRESS_ASCENSION_R	Repeat of ADDRESS_ASCENSION.	0x0	R/W
4	SDO_ACTIVE_R	Repeat of SDO_ACTIVE.	0x0	R/W
3	SDO_ACTIVE	Choose Between 3-Wire or 4-Wire Operation. 0: 3-wire. 1: 4-wire SPI (enables SDO and SDIO becomes an input only).	0x0	R/W
2	ADDRESS_ASCENSION	Address Ascension When Streaming. 0: address auto-decrements when streaming. 1: address auto-increments when streaming.	0x0	R/W
1	LSB_FIRST	I/O Data Oriented LSB First. 0: MSB first. 1: LSB first.	0x0	R/W
0	SOFT_RESET	Reset SPI Registers Except REG0000 to POR State. Self-clearing reset. 0: Normal operation. 1: Soft reset.	0x0	R/W

Address: 0x01, Reset: 0x00, Name: REG0001

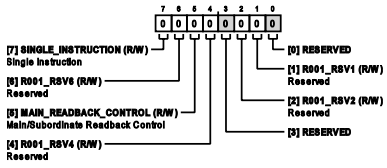

Figure 107.

Table 44. Bit Descriptions for REG0001

Bits	Bit Name	Description	Reset	Access
7	SINGLE_INSTRUCTION	Single Instruction. 0: SPI streaming enabled. 1: SPI streaming disabled.	0x0	R/W
6	R001_RSV6	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
5	MAIN_READBACK_CONTROL	Main/Subordinate Readback Control. 0: double buffering, readback subordinate register.	0x0	R/W

REGISTER MAP

Table 44. Bit Descriptions for REG0001

Bits	Bit Name	Description	Reset	Access
		1: double buffering, readback main register.		
4	R001_RSV4	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
3	RESERVED	Reserved.	0x0	R
2	R001_RSV2	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
1	R001_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
0	RESERVED	Reserved.	0x0	R

Address: 0x02, Reset: 0x00, Name: REG0002

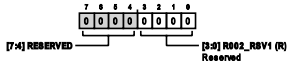

Figure 108.

Table 45. Bit Descriptions for REG0002

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	R002_RSV1	Reserved.	0x0	R

Address: 0x03, Reset: 0x00, Name: REG0003

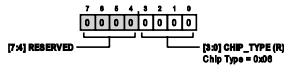

Figure 109.

Table 46. Bit Descriptions for REG0003

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CHIP_TYPE	Chip Type = 0x06.	0x0	R

Address: 0x04, Reset: 0x00, Name: REG0004

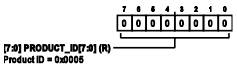

Figure 110.

Table 47. Bit Descriptions for REG0004

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]	Product ID = 0x0005.	0x0	R

Address: 0x05, Reset: 0x00, Name: REG0005

REGISTER MAP

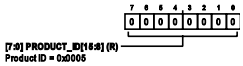

Figure 111.

Table 48. Bit Descriptions for REG0005

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]	Product ID = 0x0005.	0x0	R

Address: 0x06, Reset: 0x00, Name: REG0006

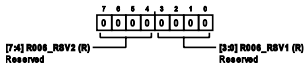

Figure 112.

Table 49. Bit Descriptions for REG0006

Bits	Bit Name	Description	Reset	Access
[7:4]	R006_RSV2	Reserved.	0x0	R
[3:0]	R006_RSV1	Reserved.	0x0	R

Address: 0x0A, Reset: 0x00, Name: REG000A

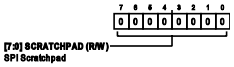

Figure 113.

Table 50. Bit Descriptions for REG000A

Bits	Bit Name	Description	Reset	Access
[7:0]	SCRATCHPAD	SPI Scratchpad.	0x0	R/W

Address: 0x0B, Reset: 0x00, Name: REG000B

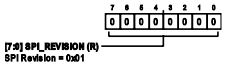

Figure 114.

Table 51. Bit Descriptions for REG000B

Bits	Bit Name	Description	Reset	Access
[7:0]	SPI_REVISION	SPI Revision = 0x01.	0x0	R

Address: 0x0C, Reset: 0x56, Name: REG000C

REGISTER MAP

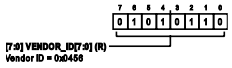

Figure 115.

Table 52. Bit Descriptions for REG000C

Bits	Bit Name	Description	Reset	Access
[7:0]	VENDOR_ID[7:0]	Vendor ID = 0x0456.	0x56	R

Address: 0x0D, Reset: 0x04, Name: REG000D

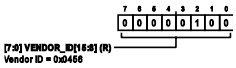

Figure 116.

Table 53. Bit Descriptions for REG000D

Bits	Bit Name	Description	Reset	Access
[7:0]	VENDOR_ID[15:8]	Vendor ID = 0x0456.	0x4	R

Address: 0x0F, Reset: 0x00, Name: REG000F

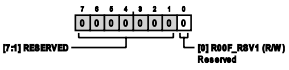

Figure 117.

Table 54. Bit Descriptions for REG000F

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	R00F_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x10, Reset: 0x80, Name: REG0010

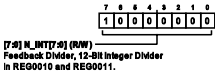

Figure 118.

Table 55. Bit Descriptions for REG0010

Bits	Bit Name	Description	Reset	Access
[7:0]	N_INT[7:0]	Feedback Divider, 12-Bit Integer Divider in REG0010 and REG0011. Set to any divide value from 2 to 4095, inclusive. Double buffering always enabled.	0x80	R/W

Address: 0x11, Reset: 0x00, Name: REG0011

REGISTER MAP

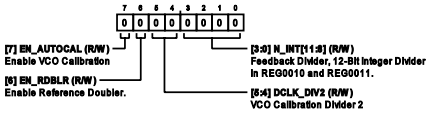

Figure 119.

Table 56. Bit Descriptions for REG0011

Bits	Bit Name	Description	Reset	Access
7	EN_AUTOCAL	Enable VCO Calibration. 0: disabled. 1: enabled.	0x0	R/W
6	EN_RDBLR	Enable Reference Doubler. 0: reference divider path selected. 1: reference doubler path selected.	0x0	R/W
[5:4]	DCLK_DIV2	VCO Calibration Divider 2. 00: divide by 1. 01: divide by 2. 10: divide by 4. 11: divide by 8.	0x0	R/W
[3:0]	N_INT[11:8]	Feedback Divider, 12-Bit Integer Divider in REG0010 and REG0011. Set to any divide value from 2 to 4095, inclusive. Double buffering always enabled.	0x0	R/W

Address: 0x12, Reset: 0x01, Name: REG0012

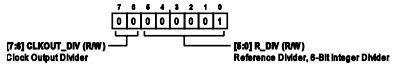

Figure 120.

Table 57. Bit Descriptions for REG0012

Bits	Bit Name	Description	Reset	Access
[7:6]	CLKOUT_DIV	Clock Output Divider. 00: divide by 1. 01: divide by 2. 10: divide by 4. 11: divide by 8.	0x0	R/W
[5:0]	R_DIV	Reference Divider, 6-Bit Integer Divider.	0x1	R/W

Address: 0x13, Reset: 0x00, Name: REG0013

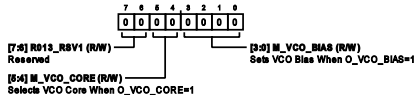

Figure 121.

REGISTER MAP

Table 58. Bit Descriptions for REG0013

Bits	Bit Name	Description	Reset	Access
[7:6]	R013_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[5:4]	M_VCO_CORE	Selects VCO Core When O_VCO_CORE = 1. 00: VCO 0 lowest frequency. 01: VCO 1. 10: VCO 2. 11: VCO 3 highest frequency.	0x0	R/W
[3:0]	M_VCO_BIAS	Sets VCO Bias When O_VCO_BIAS = 1. 0000: bias = 0. 0001: bias = 1. 0010: bias = 2. 0011: bias = 3. 0100: bias = 4. 0101: bias = 5. 0110: bias = 6. 0111: bias = 7. 1000: bias = 8. 1001: bias = 9. 1010: bias = 10. 1011: bias = 11. 1100: bias = 12. 1101: bias = 13. 1110: bias = 14. 1111: bias = 15.	0x0	R/W

Address: 0x14, Reset: 0x00, Name: REG0014

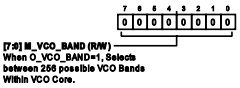

Figure 122.

Table 59. Bit Descriptions for REG0014

Bits	Bit Name	Description	Reset	Access
[7:0]	M_VCO_BAND	When O_VCO_BAND = 1, Selects Between 256 Possible VCO Bands Within VCO Core. 0: highest frequency VCO band 255: lowest frequency VCO band	0x0	R/W

Address: 0x15, Reset: 0x00, Name: REG0015

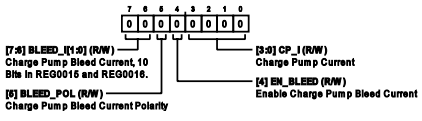

Figure 123.

REGISTER MAP

Table 60. Bit Descriptions for REG0015

Bits	Bit Name	Description	Reset	Access
[7:6]	BLEED_I[1:0]	Charge Pump Bleed Current, 10 Bits in REG0015 and REG0016. Refer to the Charge Pump Bleed Current section. Double buffering option.	0x0	R/W
5	BLEED_POL	Charge Pump Bleed Current Polarity. 0: sink current. Increases reference input to clock output propagation delay. 1: source current. Decreases reference input to clock output propagation delay.	0x0	R/W
4	EN_BLEED	Enable Charge Pump Bleed Current. 0: disabled. 1: enabled.	0x0	R/W
[3:0]	CP_I	Charge Pump Current. 0000: 0.79 mA. 0001: 0.99 mA. 0010: 1.19 mA. 0011: 1.38 mA. 0100: 1.59 mA. 0101: 1.98 mA. 0110: 2.39 mA. 0111: 2.79 mA. 1000: 3.18 mA. 1001: 3.97 mA. 1010: 4.77 mA. 1011: 5.57 mA. 1100: 6.33 mA. 1101: 7.91 mA. 1110: 9.51 mA. 1111: 11.1 mA.	0x0	R/W

Address: 0x16, Reset: 0x00, Name: REG0016

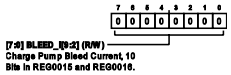

Figure 124.

Table 61. Bit Descriptions for REG0016

Bits	Bit Name	Description	Reset	Access
[7:0]	BLEED_I[9:2]	Charge Pump Bleed Current, 10 Bits in REG0015 and REG0016. Refer to the Charge Pump Bleed Current section. Double buffering option.	0x0	R/W

Address: 0x17, Reset: 0x00, Name: REG0017

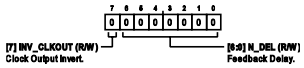

Figure 125.

Table 62. Bit Descriptions for REG0017

Bits	Bit Name	Description	Reset	Access
7	INV_CLKOUT	Clock Output Invert. Double buffering option.	0x0	R/W

REGISTER MAP

Table 62. Bit Descriptions for REG0017

Bits	Bit Name	Description	Reset	Access
		0: not inverted. 1: inverted.		
[6:0]	N_DEL	Feedback Delay. Decreases reference input to clock output propagation delay. Double buffering option.	0x0	R/W

Address: 0x18, Reset: 0x00, Name: REG0018

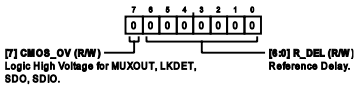

Figure 126.

Table 63. Bit Descriptions for REG0018

Bits	Bit Name	Description	Reset	Access
7	CMOS_OV	Logic High Voltage for MUXOUT, LKDET, SDO, SDIO. 0: 1.8 V logic. 1: 3.3 V logic.	0x0	R/W
[6:0]	R_DEL	Reference Delay. Increases reference input to clock output propagation delay. Double buffering option.	0x0	R/W

Address: 0x19, Reset: 0x04, Name: REG0019

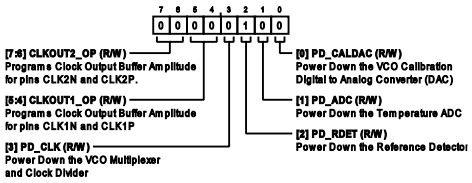

Figure 127.

Table 64. Bit Descriptions for REG0019

Bits	Bit Name	Description	Reset	Access
[7:6]	CLKOUT2_OP	Programs a Clock Output Buffer Amplitude for Pins CLK2N and CLK2P. 00: minimum amplitude, see the Specifications section. 01: see the Specifications section. 10: see the Specifications section. 11: maximum amplitude, see the Specifications section.	0x0	R/W
[5:4]	CLKOUT1_OP	Programs Clock Output Buffer Amplitude for Pins CLK1N and CLK1P. 00: minimum amplitude, see the Specifications section. 01: see the Specifications section. 10: see the Specifications section. 11: maximum amplitude, see the Specifications section.	0x0	R/W
3	PD_CLK	Power Down the VCO Multiplexer and Clock Divider. 0: active. Normal operation. 1: power-down. Refer to the Block Power Down Control section.	0x0	R/W
2	PD_RDET	Power Down the Reference Detector. 0: active. Normal operation.	0x1	R/W

REGISTER MAP

Table 64. Bit Descriptions for REG0019

Bits	Bit Name	Description	Reset	Access
		1: power-down.		
1	PD_ADC	Power Down the Temperature ADC. 0: active. Normal operation. 1: power-down.	0x0	R/W
0	PD_CALDAC	Power Down the VCO Calibration Digital to Analog Converter (DAC). 0: active. Normal operation. 1: power-down. Refer to the Block Power Down Control section.	0x0	R/W

Address: 0x1A, Reset: 0x83, Name: REG001A

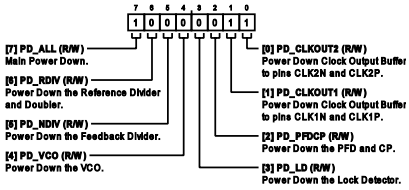

Figure 128.

Table 65. Bit Descriptions for REG001A

Bits	Bit Name	Description	Reset	Access
7	PD_ALL	Main Power Down. 0: active. 1: power-down. Does not reset SPI registers to POR state. Refer to the Power-Up and Initialization Sequence section.	0x1	R/W
6	PD_RDIV	Power Down the Reference Divider and Doubler. 0: active. Normal operation. 1: power-down. Refer to the Block Power Down Control section.	0x0	R/W
5	PD_NDIV	Power Down the Feedback Divider. 0: active. Normal operation. 1: power-down. Refer to the Block Power Down Control section.	0x0	R/W
4	PD_VCO	Power Down the VCO. 0: active. Normal operation. 1: power-down. Refer to the Block Power Down Control section.	0x0	R/W
3	PD_LD	Power Down the Lock Detector. 0: active. Normal operation. 1: power-down. Refer to the Block Power Down Control section.	0x0	R/W
2	PD_PFDCP	Power Down the PFD and CP. 0: active. Normal operation. 1: power-down. Refer to the Block Power Down Control section.	0x0	R/W
1	PD_CLKOUT1	Power Down Clock Output Buffer to Pins CLK1N and CLK1P. 0: active. Normal operation. 1: power-down.	0x1	R/W
0	PD_CLKOUT2	Power Down Clock Output Buffer to Pins CLK2N and CLK2P. 0: active. Normal operation. 1: power-down.	0x1	R/W

REGISTER MAP

Address: 0x1B, Reset: 0x00, Name: REG001B

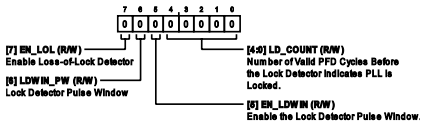

Figure 129.

Table 66. Bit Descriptions for REG001B

Bits	Bit Name	Description	Reset	Access
7	EN_LOL	Enable Loss-of-Lock Detector. 0: disabled. 1: enabled. Normal operation.	0x0	R/W
6	LDWIN_PW	Lock Detector Pulse Window. 0: narrow window. Normal operation. 1: wide window. Refer to the Lock Detector section.	0x0	R/W
5	EN_LDWIN	Enable the Lock Detector Pulse Window. 0: disabled. 1: enabled. Normal operation.	0x0	R/W
[4:0]	LD_COUNT	Number of Valid PFD Cycles Before the Lock Detector Indicates PLL is Locked. Refer to the Lock Detector section.	0x0	R/W

Address: 0x1C, Reset: 0x00, Name: REG001C

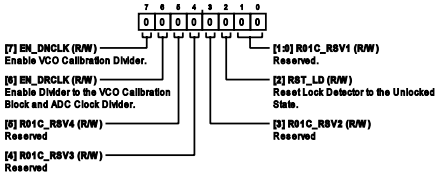

Figure 130.

Table 67. Bit Descriptions for REG001C

Bits	Bit Name	Description	Reset	Access
7	EN_DNCLK	Enable VCO Calibration Divider. See Figure 70. 0: disabled. Disable when not in use to reduce spurious content. 1: enabled. Enable before a VCO calibration begins.	0x0	R/W
6	EN_DRCLK	Enable Divider to the VCO Calibration Block and ADC Clock Divider. See Figure 70. 0: disabled. Disable when not in use to reduce spurious content. 1: enabled. Enable before a VCO calibration or temperature sensor measurement begins.	0x0	R/W
5	R01C_RSV4	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
4	R01C_RSV3	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
3	R01C_RSV2	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
2	RST_LD	Reset Lock Detector to the Unlocked State. This bit is not self-clearing. 0: reset inactive. Normal operation. 1: reset active.	0x0	R/W

REGISTER MAP

Table 67. Bit Descriptions for REG001C

Bits	Bit Name	Description	Reset	Access
[1:0]	R01C_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x1D, Reset: 0x00, Name: REG001D

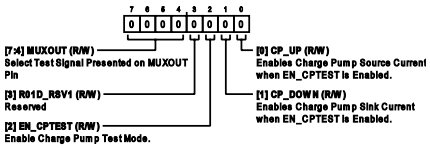

Figure 131.

Table 68. Bit Descriptions for REG001D

Bits	Bit Name	Description	Reset	Access
[7:4]	MUXOUT	Select Test Signal Presented on MUXOUT Pin. 0000: high-Z. 0001: LKDET. Lock detector output. 0010: low. 0011: low. 0100: $f_{DIV\_RCLK}/2$. 0101: $f_{DIV\_NCLK}/2$. 0110: reserved. 0111: low. 1000: high. 1001: reserved. 1010: reserved. 1011: low. 1100: low. 1101: low. 1110: reserved. 1111: reserved.	0x0	R/W
3	R01D_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
2	EN_CPTEST	Enable Charge Pump Test Mode. 0: disabled. Normal operation. 1: enabled.	0x0	R/W
1	CP_DOWN	Enables Charge Pump Sink Current when EN_CPTEST is Enabled. 0: disabled. 1: enabled.	0x0	R/W
0	CP_UP	Enables Charge Pump Source Current when EN_CPTEST is Enabled. 0: disabled. 1: enabled.	0x0	R/W

Address: 0x1E, Reset: 0x00, Name: REG001E

REGISTER MAP

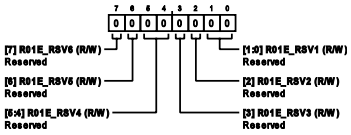

Figure 132.

Table 69. Bit Descriptions for REG001E

Bits	Bit Name	Description	Reset	Access
7	R01E_RSV6	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
6	R01E_RSV5	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[5:4]	R01E_RSV4	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
3	R01E_RSV3	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
2	R01E_RSV2	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[1:0]	R01E_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x1F, Reset: 0x00, Name: REG001F

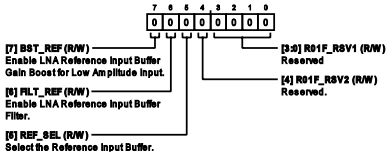

Figure 133.

Table 70. Bit Descriptions for REG001F

Bits	Bit Name	Description	Reset	Access
7	BST_REF	Enable LNA Reference Input Buffer Gain Boost for Low Amplitude Input. Refer to Table 9. 0: disabled. 1: enabled.	0x0	R/W
6	FILT_REF	Enable LNA Reference Input Buffer Filter. Refer to Table 8. 0: disabled. 1: enabled.	0x0	R/W
5	REF_SEL	Select the Reference Input Buffer. Refer to Table 7. 0: DMA for an improved reference input to clock output propagation delay temperature coefficient. 1: LNA for improved PLL in-band noise when a low slew rate signal is applied to the reference input.	0x0	R/W
4	R01F_RSV2	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[3:0]	R01F_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x20, Reset: 0x00, Name: REG0020

REGISTER MAP

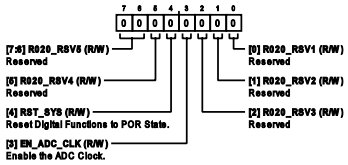

Figure 134.

Table 71. Bit Descriptions for REG0020

Bits	Bit Name	Description	Reset	Access
[7:6]	R020_RSV5	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
5	R020_RSV4	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
4	RST_SYS	Reset Digital Functions to POR State. Does not reset the SPI interface and SPI registers. This bit is not self-clearing. 0: reset inactive. Normal operation. 1: reset active.	0x0	R/W
3	EN_ADC_CLK	Enable the ADC Clock. See Figure 70. 0: disabled. 1: enabled. Normal operation.	0x0	R/W
2	R020_RSV3	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
1	R020_RSV2	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
0	R020_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x21, Reset: 0x00, Name: REG0021

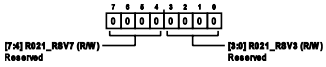

Figure 135.

Table 72. Bit Descriptions for REG0021

Bits	Bit Name	Description	Reset	Access
[7:4]	R021_RSV7	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[3:0]	R021_RSV3	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x22, Reset: 0x00, Name: REG0022

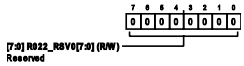

Figure 136.

Table 73. Bit Descriptions for REG0022

Bits	Bit Name	Description	Reset	Access
[7:0]	R022_RSV0[7:0]	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x23, Reset: 0x00, Name: REG0023

REGISTER MAP

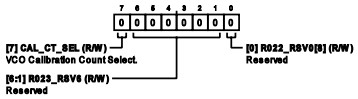

Figure 137.

Table 74. Bit Descriptions for REG0023

Bits	Bit Name	Description	Reset	Access
7	CAL_CT_SEL	VCO Calibration Count Select. Refer to Table 17.	0x0	R/W
[6:1]	R023_RSV6	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
0	R022_RSV0[8]	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x24, Reset: 0x00, Name: REG0024

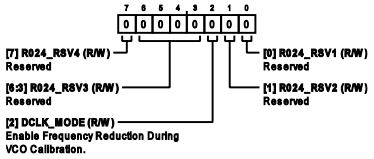

Figure 138.

Table 75. Bit Descriptions for REG0024

Bits	Bit Name	Description	Reset	Access
7	R024_RSV4	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[6:3]	R024_RSV3	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
2	DCLK_MODE	Enable Frequency Reduction During VCO Calibration. Divides f_{DIV_RCLK} and f_{DIV_NCLK} by 2 when enabled. Refer to Table 17. 0: disabled. 1: enabled.	0x0	R/W
1	R024_RSV2	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
0	R024_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x25, Reset: 0x00, Name: REG0025

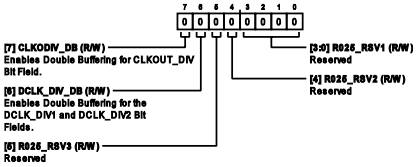

Figure 139.

Table 76. Bit Descriptions for REG0025

Bits	Bit Name	Description	Reset	Access
7	CLKODIV_DB	Enables Double Buffering for CLKOUT_DIV Bit Field.	0x0	R/W

REGISTER MAP

Table 76. Bit Descriptions for REG0025

Bits	Bit Name	Description	Reset	Access
		0: disabled. 1: enabled.		
6	DCLK_DIV_DB	Enables Double Buffering for the DCLK_DIV1 and DCLK_DIV2 Bit Fields. 0: disabled. 1: enabled.	0x0	R/W
5	R025_RSV3	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
4	R025_RSV2	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[3:0]	R025_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x26, Reset: 0x00, Name: REG0026

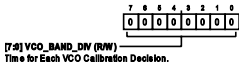

Figure 140.

Table 77. Bit Descriptions for REG0026

Bits	Bit Name	Description	Reset	Access
[7:0]	VCO_BAND_DIV	Time for Each VCO Calibration Decision. Determined by Equation 13 in the VCO Calibration section.	0x0	R/W

Address: 0x27, Reset: 0x00, Name: REG0027

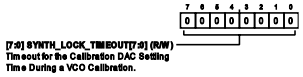

Figure 141.

Table 78. Bit Descriptions for REG0027

Bits	Bit Name	Description	Reset	Access
[7:0]	SYNTH_LOCK_TIMEOUT[7:0]	Timeout for the Calibration DAC Settling Time During a VCO Calibration. Determined by Equation 13 in the VCO Calibration section.	0x0	R/W

Address: 0x28, Reset: 0x00, Name: REG0028

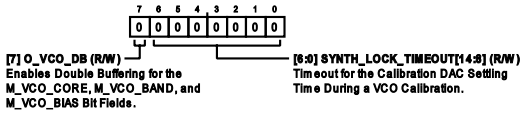

Figure 142.

Table 79. Bit Descriptions for REG0028

Bits	Bit Name	Description	Reset	Access
7	O_VCO_DB	Enables Double Buffering for the M_VCO_CORE, M_VCO_BAND, and M_VCO_BIAS Bit Fields. 0: disabled. 1: enabled.	0x0	R/W

REGISTER MAP

Table 79. Bit Descriptions for REG0028

Bits	Bit Name	Description	Reset	Access
[6:0]	SYNTH_LOCK_TIMEOUT[14:8]	Timeout for the Calibration DAC Settling Time During a VCO Calibration. Determined by Equation 13 in the VCO Calibration section.	0x0	R/W

Address: 0x29, Reset: 0x00, Name: REG0029

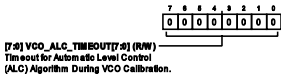

Figure 143.

Table 80. Bit Descriptions for REG0029

Bits	Bit Name	Description	Reset	Access
[7:0]	VCO_ALC_TIMEOUT[7:0]	Timeout for Automatic Level Control (ALC) Algorithm During VCO Calibration. Determined by Equation 13 in the VCO Calibration section.	0x0	R/W

Address: 0x2A, Reset: 0x00, Name: REG002A

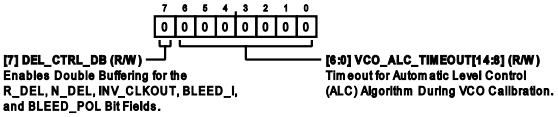

Figure 144.

Table 81. Bit Descriptions for REG002A

Bits	Bit Name	Description	Reset	Access
7	DEL_CTRL_DB	Enables Double Buffering for the R_DEL, N_DEL, INV_CLKOUT, BLEED_I, and BLEED_POL Bit Fields. 0: disabled. 1: enabled.	0x0	R/W
[6:0]	VCO_ALC_TIMEOUT[14:8]	Timeout for Automatic Level Control (ALC) Algorithm During VCO Calibration. Determined by Equation 13 in the VCO Calibration section.	0x0	R/W

Address: 0x2B, Reset: 0x00, Name: REG002B

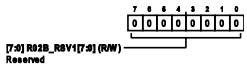

Figure 145.

Table 82. Bit Descriptions for REG002B

Bits	Bit Name	Description	Reset	Access
[7:0]	R02B_RSV1[7:0]	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x2C, Reset: 0x00, Name: REG002C

REGISTER MAP

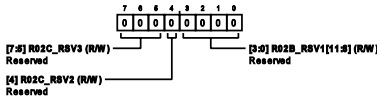

Figure 146.

Table 83. Bit Descriptions for REG002C

Bits	Bit Name	Description	Reset	Access
[7:5]	R02C_RSV3	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
4	R02C_RSV2	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[3:0]	R02B_RSV1[11:8]	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x2D, Reset: 0x00, Name: REG002D

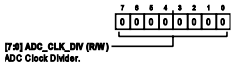

Figure 147.

Table 84. Bit Descriptions for REG002D

Bits	Bit Name	Description	Reset	Access
[7:0]	ADC_CLK_DIV	ADC Clock Divider. Determined by Equation 13 in the VCO Calibration section.	0x0	R/W

Address: 0x2E, Reset: 0x00, Name: REG002E

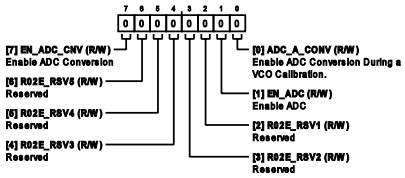

Figure 148.

Table 85. Bit Descriptions for REG002E

Bits	Bit Name	Description	Reset	Access
7	EN_ADC_CNV	Enable ADC Conversion. Refer to the Temperature Sensor section. 0: disabled. 1: enabled. Normal operation.	0x0	R/W
6	R02E_RSV5	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
5	R02E_RSV4	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
4	R02E_RSV3	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
3	R02E_RSV2	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
2	R02E_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
1	EN_ADC	Enable ADC. Refer to the Temperature Sensor section. 0: ADC conversion only possible with write to ADC_ST_CNV bit field. 1: enabled. Normal operation.	0x0	R/W

REGISTER MAP

Table 85. Bit Descriptions for REG002E

Bits	Bit Name	Description	Reset	Access
0	ADC_A_CONV	Enable ADC Conversion During a VCO Calibration. 0: ADC conversion only possible with write to ADC_ST_CNV bit field. 1: enabled. Normal operation. Automatically begins ADC conversion at the start of a VCO calibration or with write to ADC_ST_CNV bit field.	0x0	R/W

Address: 0x2F, Reset: 0x00, Name: REG002F

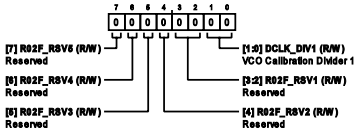

Figure 149.

Table 86. Bit Descriptions for REG002F

Bits	Bit Name	Description	Reset	Access
7	R02F_RSV5	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
6	R02F_RSV4	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
5	R02F_RSV3	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
4	R02F_RSV2	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[3:2]	R02F_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[1:0]	DCLK_DIV1	VCO Calibration Divider 1. 00: divide by 1. 01: divide by 2. 10: divide by 8. 11: divide by 32.	0x0	R/W

Address: 0x30, Reset: 0x00, Name: REG0030

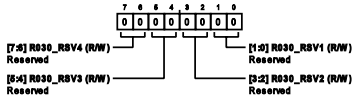

Figure 150.

Table 87. Bit Descriptions for REG0030

Bits	Bit Name	Description	Reset	Access
[7:6]	R030_RSV4	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[5:4]	R030_RSV3	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[3:2]	R030_RSV2	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[1:0]	R030_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x31, Reset: 0x00, Name: REG0031

REGISTER MAP

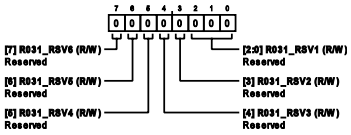

Figure 151.

Table 88. Bit Descriptions for REG0031

Bits	Bit Name	Description	Reset	Access
7	R031_RSV6	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
6	R031_RSV5	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
5	R031_RSV4	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
4	R031_RSV3	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
3	R031_RSV2	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[2:0]	R031_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x32, Reset: 0x00, Name: REG0032

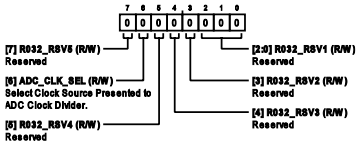

Figure 152.

Table 89. Bit Descriptions for REG0032

Bits	Bit Name	Description	Reset	Access
7	R032_RSV5	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
6	ADC_CLK_SEL	Select Clock Source Presented to ADC Clock Divider. See Figure 70. 0: select internal clock. Normal operation. Used during VCO calibrations and full power die temperature measurement. 1: select SCLK pin. Ambient die temperature measurements with the temperature sensor. See the Temperature Sensor section.	0x0	R/W
5	R032_RSV4	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
4	R032_RSV3	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
3	R032_RSV2	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[2:0]	R032_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x33, Reset: 0x00, Name: REG0033

REGISTER MAP

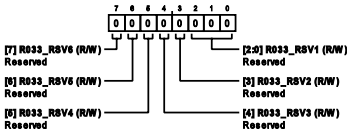

Figure 153.

Table 90. Bit Descriptions for REG0033

Bits	Bit Name	Description	Reset	Access
7	R033_RSV6	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
6	R033_RSV5	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
5	R033_RSV4	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
4	R033_RSV3	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
3	R033_RSV2	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[2:0]	R033_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x34, Reset: 0x00, Name: REG0034

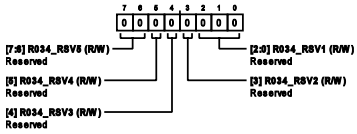

Figure 154.

Table 91. Bit Descriptions for REG0034

Bits	Bit Name	Description	Reset	Access
[7:6]	R034_RSV5	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
5	R034_RSV4	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
4	R034_RSV3	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
3	R034_RSV2	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[2:0]	R034_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x35, Reset: 0x00, Name: REG0035

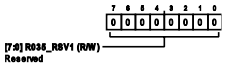

Figure 155.

Table 92. Bit Descriptions for REG0035

Bits	Bit Name	Description	Reset	Access
[7:0]	R035_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x36, Reset: 0x00, Name: REG0036

REGISTER MAP

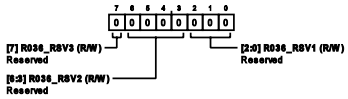

Figure 156.

Table 93. Bit Descriptions for REG0036

Bits	Bit Name	Description	Reset	Access
7	R036_RSV3	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[6:3]	R036_RSV2	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[2:0]	R036_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x37, Reset: 0x00, Name: REG0037

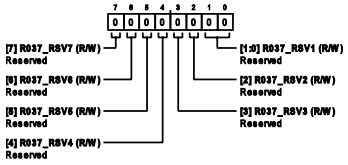

Figure 157.

Table 94. Bit Descriptions for REG0037

Bits	Bit Name	Description	Reset	Access
7	R037_RSV7	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
6	R037_RSV6	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
5	R037_RSV5	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
4	R037_RSV4	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
3	R037_RSV3	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
2	R037_RSV2	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[1:0]	R037_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x38, Reset: 0x00, Name: REG0038

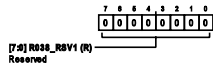

Figure 158.

Table 95. Bit Descriptions for REG0038

Bits	Bit Name	Description	Reset	Access
[7:0]	R038_RSV1	Reserved.	0x0	R

Address: 0x39, Reset: 0x00, Name: REG0039

REGISTER MAP

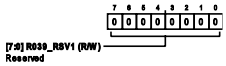

Figure 159.

Table 96. Bit Descriptions for REG0039

Bits	Bit Name	Description	Reset	Access
[7:0]	R039_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x3A, Reset: 0x00, Name: REG003A

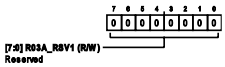

Figure 160.

Table 97. Bit Descriptions for REG003A

Bits	Bit Name	Description	Reset	Access
[7:0]	R03A_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x3B, Reset: 0x00, Name: REG003B

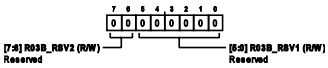

Figure 161.

Table 98. Bit Descriptions for REG003B

Bits	Bit Name	Description	Reset	Access
[7:6]	R03B_RSV2	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[5:0]	R03B_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x3C, Reset: 0x00, Name: REG003C

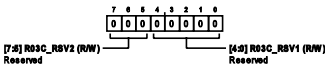

Figure 162.

Table 99. Bit Descriptions for REG003C

Bits	Bit Name	Description	Reset	Access
[7:5]	R03C_RSV2	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[4:0]	R03C_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x3D, Reset: 0x00, Name: REG003D

REGISTER MAP

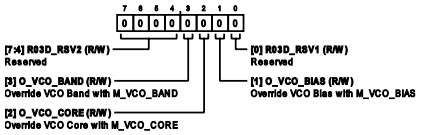

Figure 163.

Table 100. Bit Descriptions for REG003D

Bits	Bit Name	Description	Reset	Access
[7:4]	R03D_RSV2	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
3	O_VCO_BAND	Override VCO Band with M_VCO_BAND. 0: VCO band code from VCO calibration state machine. 1: VCO band code from M_VCO_BAND.	0x0	R/W
2	O_VCO_CORE	Override VCO Core with M_VCO_CORE. Refer to the VCO Calibration section. 0: VCO core set by the VCO calibration state machine. 1: VCO core set by M_VCO_CORE.	0x0	R/W
1	O_VCO_BIAS	Override VCO Bias with M_VCO_BIAS. Refer to the VCO Calibration section. 0: VCO bias set by the VCO calibration state machine. 1: VCO bias set by M_VCO_VBIAS.	0x0	R/W
0	R03D_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x3E, Reset: 0x00, Name: REG003E

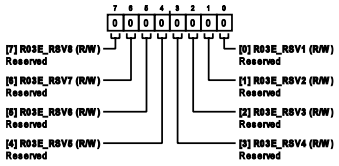

Figure 164.

Table 101. Bit Descriptions for REG003E

Bits	Bit Name	Description	Reset	Access
7	R03E_RSV8	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
6	R03E_RSV7	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
5	R03E_RSV6	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
4	R03E_RSV5	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
3	R03E_RSV4	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
2	R03E_RSV3	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
1	R03E_RSV2	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
0	R03E_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x3F, Reset: 0x00, Name: REG003F

REGISTER MAP

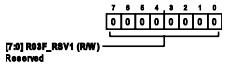

Figure 165.

Table 102. Bit Descriptions for REG003F

Bits	Bit Name	Description	Reset	Access
[7:0]	R03F_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x40, Reset: 0x00, Name: REG0040

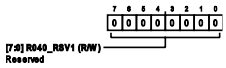

Figure 166.

Table 103. Bit Descriptions for REG0040

Bits	Bit Name	Description	Reset	Access
[7:0]	R040_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x41, Reset: 0x00, Name: REG0041

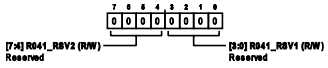

Figure 167.

Table 104. Bit Descriptions for REG0041

Bits	Bit Name	Description	Reset	Access
[7:4]	R041_RSV2	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[3:0]	R041_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x42, Reset: 0x00, Name: REG0042

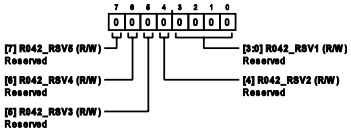

Figure 168.

Table 105. Bit Descriptions for REG0042

Bits	Bit Name	Description	Reset	Access
7	R042_RSV5	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
6	R042_RSV4	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
5	R042_RSV3	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
4	R042_RSV2	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

REGISTER MAP

Table 105. Bit Descriptions for REG0042

Bits	Bit Name	Description	Reset	Access
[3:0]	R042_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x43, Reset: 0x00, Name: REG0043

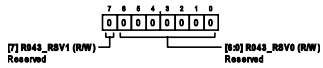

Figure 169.

Table 106. Bit Descriptions for REG0043

Bits	Bit Name	Description	Reset	Access
7	R043_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[6:0]	R043_RSV0	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x44, Reset: 0x00, Name: REG0044

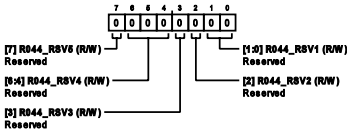

Figure 170.

Table 107. Bit Descriptions for REG0044

Bits	Bit Name	Description	Reset	Access
7	R044_RSV5	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[6:4]	R044_RSV4	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
3	R044_RSV3	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
2	R044_RSV2	Reserved. Table 42 provides required reserved register settings.	0x0	R/W
[1:0]	R044_RSV1	Reserved. Table 42 provides required reserved register settings.	0x0	R/W

Address: 0x45, Reset: 0x00, Name: REG0045

Refer to the Temperature Sensor section.

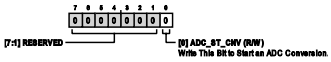

Figure 171.

Table 108. Bit Descriptions for REG0045

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	ADC_ST_CNV	Write This Bit to Start an ADC Conversion.	0x0	R/W

Address: 0x46, Reset: 0x00, Name: REG0046

REGISTER MAP

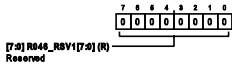

Figure 172.

Table 109. Bit Descriptions for REG0046

Bits	Bit Name	Description	Reset	Access
[7:0]	R046_RSV1[7:0]	Reserved.	0x0	R

Address: 0x47, Reset: 0x00, Name: REG0047

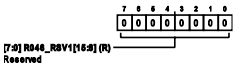

Figure 173.

Table 110. Bit Descriptions for REG0047

Bits	Bit Name	Description	Reset	Access
[7:0]	R046_RSV1[15:8]	Reserved.	0x0	R

Address: 0x48, Reset: 0x00, Name: REG0048

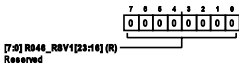

Figure 174.

Table 111. Bit Descriptions for REG0048

Bits	Bit Name	Description	Reset	Access
[7:0]	R046_RSV1[23:16]	Reserved.	0x0	R

Address: 0x49, Reset: 0x00, Name: REG0049

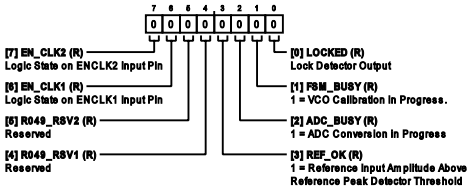

Figure 175.

Table 112. Bit Descriptions for REG0049

Bits	Bit Name	Description	Reset	Access
7	EN_CLK2	Logic State on ENCLK2 Input Pin. See Figure 74.	0x0	R
6	EN_CLK1	Logic State on ENCLK1 Input Pin. See Figure 74.	0x0	R
5	R049_RSV2	Reserved.	0x0	R

REGISTER MAP

Table 112. Bit Descriptions for REG0049

Bits	Bit Name	Description	Reset	Access
4	R049_RSV1	Reserved.	0x0	R
3	REF_OK	1 = Reference Input Amplitude Above Reference Peak Detector Threshold.	0x0	R
2	ADC_BUSY	1 = ADC Conversion in Progress. Refer to the VCO Calibration section and the Temperature Sensor section.	0x0	R
1	FSM_BUSY	1 = VCO Calibration in Progress.	0x0	R
0	LOCKED	Lock Detector Output.	0x0	R

Address: 0x4A, Reset: 0x00, Name: REG004A

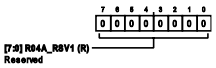

Figure 176.

Table 113. Bit Descriptions for REG004A

Bits	Bit Name	Description	Reset	Access
[7:0]	R04A_RSV1	Reserved.	0x0	R

Address: 0x4B, Reset: 0x00, Name: REG004B

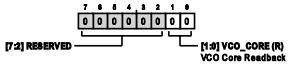

Figure 177.

Table 114. Bit Descriptions for REG004B

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	VCO_CORE	VCO Core Readback. See the VCO Calibration section.	0x0	R

Address: 0x4C, Reset: 0x00, Name: REG004C

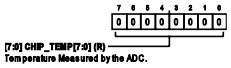

Figure 178.

Table 115. Bit Descriptions for REG004C

Bits	Bit Name	Description	Reset	Access
[7:0]	CHIP_TEMP[7:0]	Temperature Measured by the ADC. CHIP_TEMP[8] is the sign bit, where 0 = positive and 1 = negative. CHIP_TEMP[7:0] = magnitude.	0x0	R

Address: 0x4D, Reset: 0x00, Name: REG004D

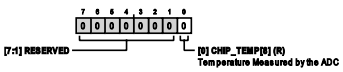

Figure 179.

REGISTER MAP

Table 116. Bit Descriptions for REG004D

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	CHIP_TEMP[8]	Temperature Measured by the ADC. CHIP_TEMP[8] is the sign bit, where 0 = positive and 1 = negative. CHIP_TEMP[7:0] = magnitude.	0x0	R

Address: 0x4E, Reset: 0x00, Name: REG004E

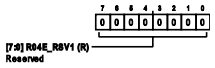

Figure 180.

Table 117. Bit Descriptions for REG004E

Bits	Bit Name	Description	Reset	Access
[7:0]	R04E_RSV1	Reserved.	0x0	R

Address: 0x4F, Reset: 0x00, Name: REG004F

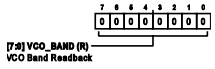

Figure 181.

Table 118. Bit Descriptions for REG004F

Bits	Bit Name	Description	Reset	Access
[7:0]	VCO_BAND	VCO Band Readback. See the VCO Calibration section.	0x0	R

Address: 0x50, Reset: 0x00, Name: REG0050

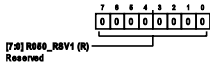

Figure 182.

Table 119. Bit Descriptions for REG0050

Bits	Bit Name	Description	Reset	Access
[7:0]	R050_RSV1	Reserved.	0x0	R

Address: 0x51, Reset: 0x00, Name: REG0051

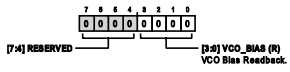

Figure 183.

Table 120. Bit Descriptions for REG0051

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R

REGISTER MAP

Table 120. Bit Descriptions for REG0051

Bits	Bit Name	Description	Reset	Access
[3:0]	VCO_BIAS	VCO Bias Readback. See the VCO Calibration section.	0x0	R

Address: 0x52, Reset: 0x00, Name: REG0052

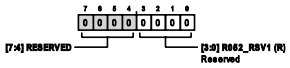

Figure 184.

Table 121. Bit Descriptions for REG0052

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	R052_RSV1	Reserved.	0x0	R

Address: 0x53, Reset: 0x00, Name: REG0053

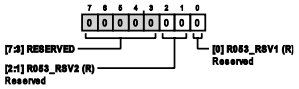

Figure 185.

Table 122. Bit Descriptions for REG0053

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:1]	R053_RSV2	Reserved.	0x0	R
0	R053_RSV1	Reserved.	0x0	R

Address: 0x54, Reset: 0x00, Name: REG0054

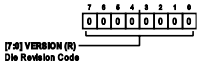

Figure 186.

Table 123. Bit Descriptions for REG0054

Bits	Bit Name	Description	Reset	Access
[7:0]	VERSION	Die Revision Code.	0x0	R

OUTLINE DIMENSIONS

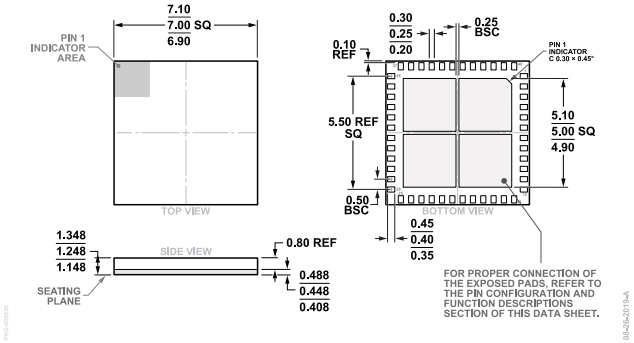

Figure 187. 48-Lead Land Grid Array Package [LGA] (CC-48-6) 7 mm × 7 mm Body, Dimensions shown in millimeters.

Updated: September 04, 2022

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADF4377BCCZ	-40°C to +105°C	LGA/CASON/CH ARRY SO NO LD		CC-48-6
ADF4377BCCZ-RL7	-40°C to +105°C	LGA/CASON/CH ARRY SO NO LD	Reel, 1500	CC-48-6

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EV-ADF4377SD1Z	ADF4377 LGA Evaluation Board

[1] Z = RoHS Compliant Part.

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